# Low－Voltage，Dual－SPDT（0．4 ${ }^{\text {）Analog Switch with }}$ Negative Swing Audio Capability 

## Features

－0．4 Typical On Resistance for +3.0 V Supply
－ $0.25 \Omega$ Maximum RoN Flatness for +3.0 V Supply
－－3db Bandwidth：＞50MHz
－Low Icct Current Over Expanded Control Input Range
－Packaged in 10－Lead UMLP
－Power－off Protection on Common Ports
－Broad $\mathrm{V}_{\mathrm{cc}}$ Operating Range： 1.65 to 4.3 V
－Noise Immunity Termination Resistors
－ESD JEDEC：JESD22－A114 Human Body Model：
－Power to GND：16KV
－I／O to GND：10kV
－All other Pins：7kV
－ESD JEDEC：JESD22－A101 Charged Device Model：
－CDM：2kV

## Applications

－Cell phone，PDA，Digital Camera，and Notebook
－LCD Monitor，TV，and Set－Top Box

## Description

The FSA2271T is a high－performance，dual－single pole double throw（SPDT）analog switch with negative swing audio capability．It features ultra－low Ron of $0.4 \Omega$ （typical）at 3．0V Vcc．The FSA2271T operates over a wide $\mathrm{V}_{\mathrm{cc}}$ range of 1.65 V to 4.3 V and is fabricated with sub－micron CMOS technology to achieve fast switching speeds．Designed for break－before－make operation，the FSA2271T select input is TTL level compatible．
The FSA2271T features very low quiescent current， even when the control voltage is lower than the $\mathrm{V}_{\mathrm{cc}}$ supply．This feature is optimized for the mobile handset applications，allowing direct interface with baseband processor general－purpose I／Os with minimal battery consumption．

The FSA2271T includes termination resistors that improve noise immunity during overshoot excursions， ＂pop－minimization，＂or off－isolation coupling．

## IMPORTANT NOTE：

For additional information，please contact analogswitch＠fairchildsemi．com．

## Ordering Information

| Part Number | Termination <br> Resistors | Operating <br> Temperature <br> Range | Eco Status | Package |
| :--- | :---: | :---: | :---: | :---: |
| FSA2271TUMX | Yes | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | Green | 10－Lead Quad Ultrathin Molded Leadless <br> Package（UMLP）， $1.4 \times 1.8 \mathrm{~mm}, 0.4 \mathrm{~mm}$ pitch |

For Fairchild＇s definition of Eco Status，please visit：http：／／www．fairchildsemi．com／company／green／rohs green．html．

## Analog Symbol



Figure 1. FSA2271T

## Pin Configuration



Figure 2. Pin Configuration

## Pin Definitions

| Pin\# | Name |  |
| :---: | :---: | :--- |
| 1,6 | S2, S1 | Switch Select Pins |
| 2,7 | $2 \mathrm{~A}, 1 \mathrm{~A}$ | Data Points |
| 3,8 | $2 \mathrm{~B} 0,1 \mathrm{B0}$ | Data Points |
| 4,9 | $2 \mathrm{~B} 1,1 \mathrm{~B} 1$ | Data Ports |
| 5 | GND | Ground |
| 10 | $V_{c c}$ | Supply Voltage Data Ports |

## Truth Table

| Control Input,Sn | Function |
| :---: | :---: |
| LOW Logic Level | nB0 connected to nA; nB1 terminated to GND |
| HIGH Logic Level | nB1 connected to nA; nB0 terminated to GND |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Conditions | Min. | Max. | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {cc }}$ | Supply Voltage |  | -0.5 | 5.5 | V |
| $V_{\text {sw }}$ | Switch Voltage ${ }^{(1)}$ | 1B0, 1B1, 2B0, 2B1, 1A, 2A Pins | $\mathrm{V}_{\mathrm{cc}}-4.3 \mathrm{~V}$ | $V_{C C}+0.3 V$ | V |
| $\mathrm{V}_{\text {CNTRL }}$ | Control Input Voltage ${ }^{(1)}$ | S1, S2 | -0.5 | $\mathrm{V}_{\mathrm{cc}}+0.3 \mathrm{~V}$ | V |
| $\mathrm{I}_{\mathrm{K}}$ | Input Clamp Diode Current |  |  | -50 | mA |
| Isw | Switch I/O Current | Continuous |  | 350 | mA |
| Iswpeak | Peak Switch Current | Pulsed at 1ms Duration, <10\% Duty Cycle |  | 500 | mA |
| TSTG | Storage Temperature Range |  | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Maximum Junction Temperature |  |  | +150 | ${ }^{\circ} \mathrm{C}$ |
| TL | Lead Temperature | Soldering 10 seconds |  | +260 | ${ }^{\circ} \mathrm{C}$ |
| ESD | Human Body Model, JEDEC: JESD22-A114 | I/O to GND | 10 |  | kV |
|  |  | All Other Pins | 7 |  |  |
|  |  | Power to GND | 16 |  |  |
|  | Charged Device Model, JEDEC-JESD-C101 |  | 2 |  |  |

## Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{Cc}}$ | Supply Voltage | 1.65 | 4.30 | V |
| $\mathrm{~V}_{\mathrm{S} 1, \mathrm{~S} 2}$ | Control Input Voltage | 0 | $\mathrm{~V}_{\mathrm{cc}}$ | V |
| $\mathrm{V}_{\mathrm{SW}}$ | Switch I/O Voltage | $\mathrm{V}_{\mathrm{Cc}}-4.3$ | $\mathrm{~V}_{\mathrm{Cc}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |

## DC Electrical Characteristics

All typical values are for $\mathrm{V}_{\mathrm{Cc}}=3.3 \mathrm{~V}$ at $25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $\mathrm{V}_{\mathrm{cc}}(\mathrm{V})$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=-40 \text { to } \\ +85^{\circ} \mathrm{C} \end{gathered}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. | Min. | Max. |  |
| $\mathrm{V}_{\text {IH }}$ | Input Voltage High |  | 3.60 to 4.30 |  |  |  | 1.7 |  |  |
|  |  |  | 2.70 to 3.60 |  |  |  | 1.5 |  | V |
|  |  |  | 2.30 to 2.70 |  |  |  | 1.4 |  |  |
|  |  |  | 1.65 to 1.95 |  |  |  | 0.9 |  |  |
| $\mathrm{V}_{\text {IL }}$ | Input Voltage Low |  | 3.60 to 4.30 |  |  |  |  | 0.7 | V |
|  |  |  | 2.70 to 3.60 |  |  |  |  | 0.5 | V |
|  |  |  | 2.30 to 2.70 |  |  |  |  | 0.4 |  |
|  |  |  | 1.65 to 1.95 |  |  |  |  | 0.4 |  |
| In | Control Input Leakage (S1,S2) | $\mathrm{V}_{\text {IN }}=0$ to $\mathrm{V}_{\mathrm{cc}}$ | 1.65 to 4.30 |  |  |  | -0.5 | 0.5 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{A}(\mathrm{ON})}$ | On Leakage Current of Port nA | $n A=0.3 V, V_{c c}-0.3 V$; nB0 or nB1 (on) =nA or Floating; nB0 or nB1 (off) $=0 \mathrm{~V}$ or floating Figure 5 | 1.95 to 4.30 |  |  |  | -1 | 1 | $\mu \mathrm{A}$ |
| loff | Power Off Leakage Current (Common Port Only 1A, 2A) | $\begin{aligned} & \text { Common Port }(1 \mathrm{~A}, 2 \mathrm{~A}) ; \\ & \mathrm{V}_{1 \mathrm{~N}}=0 \mathrm{~V} \text { to } 4.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{cc}}=0 \mathrm{~V} ; \mathrm{nB0}, \\ & \mathrm{nB} 1=0 \mathrm{~V} \text { or Floating } \\ & \hline \end{aligned}$ | 0 |  |  |  |  | $\pm 45$ | $\mu \mathrm{A}$ |
| Ron | Switch On Resistance ${ }^{(2)}$ | $\mathrm{I}_{\mathrm{on}}=100 \mathrm{~mA}, \mathrm{nB} 0 \text { or } \mathrm{nB} 1=0 \mathrm{~V} \text {, }$ <br> $0.7 \mathrm{~V}, 3.6 \mathrm{~V}, 4.3 \mathrm{~V}$ <br> Figure 3 | 4.30 |  | 0.3 |  |  |  | $\Omega$ |
|  |  | $\mathrm{IoN}_{\mathrm{N}}=100 \mathrm{~mA}, \mathrm{nB} 0 \text { or } \mathrm{nB} 1=0 \mathrm{~V} \text {, }$ $0.7 \mathrm{~V}, 2.3 \mathrm{~V}, 3.0 \mathrm{~V}$ <br> Figure 3 | 3.00 |  | 0.4 |  |  | 0.8 |  |
|  |  | $\begin{aligned} & \text { Ion }=100 \mathrm{~mA}, \mathrm{nB0} \text { or } \mathrm{nB} 1=0 \mathrm{~V} \text {, } \\ & 0.7 \mathrm{~V}, 1.6 \mathrm{~V}, 2.3 \mathrm{~V} \end{aligned}$ $\text { Figure } 3$ | 2.30 |  | 0.52 |  |  |  |  |
|  |  | $\mathrm{I}_{\mathrm{N}}=100 \mathrm{~mA}, \mathrm{nB} 0 \text { or } \mathrm{nB} 1=0 \mathrm{~V} \text {, }$ <br> $0.7 \mathrm{~V}, 1.65 \mathrm{~V}$ <br> Figure 3 | 1.65 |  | 1.00 |  |  |  |  |
| $\Delta \mathrm{R}_{\text {ON }}$ | On Resistance Matching Between Channels ${ }^{(3}$ | $\mathrm{I}_{\mathrm{ON}}=100 \mathrm{~mA}, \mathrm{nB} 0$ or $\mathrm{nB} 1=0.7 \mathrm{~V}$ | 4.30 |  | 0.04 |  |  | 0.13 | $\Omega$ |
|  |  |  | 3.00 |  | 0.06 |  |  | 0.13 |  |
|  |  |  | 2.30 |  | 0.12 |  |  |  |  |
|  |  |  | 1.65 |  | 1.00 |  |  |  |  |
| $\mathrm{R}_{\text {FLAt(ON) }}$ | On Resistance Flatness ${ }^{(4)}$ | $\text { lout }=100 \mathrm{~mA}, \mathrm{nB} 0 \text { or nB1 }=0 \mathrm{~V}$$\text { to } V_{\mathrm{cc}}$ | 4.30 |  |  |  |  | 0.25 | $\Omega$ |
|  |  |  | 3.00 |  |  |  |  | 0.25 |  |
|  |  |  | 2.30 |  | 0.5 |  |  |  |  |
|  |  |  | 1.65 |  | 0.6 |  |  |  |  |
| $\mathrm{R}_{\text {TERM }}$ | Internal Termination Resistors ${ }^{(5)}$ |  |  |  | 10 |  |  |  | k $\Omega$ |
| Icc | Quiescent Supply Current | $\mathrm{V}_{1 \mathrm{~N}}=0$ or $\mathrm{V}_{\text {cc }}$, lout $=0$ | 4.30 | -100 |  | 100 | -500 | 500 | nA |
| $\mathrm{I}_{\text {CCT }}$ | Increase in Icc per Input | Input at 2.6 V | 4.30 |  | 3.0 |  |  | 10.0 | $\mu \mathrm{A}$ |
|  |  | Input at 1.8V |  |  | 7.0 |  |  | 15.0 |  |

## Notes:

2. On resistance is determined by the voltage drop between the $A$ and $B$ pins at the indicated current through the switch.
3. $\quad \Delta R_{O N}=R_{o N ~ m a x ~}-R_{\text {ON min }}$ measured at identical $\mathrm{V}_{\mathrm{CC}}$, temperature, and voltage.
4. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
5. Guaranteed by characterization, not production tested.

## AC Electrical Characteristics

All typical value are for $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ at $25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{c c}$ <br> (V) | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \\ & \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. | Min. | Max. |  |
| ton | Turn-On Time | $\begin{aligned} & \mathrm{nB0} \text { or } \mathrm{nB} 1=1.5 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=50 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \\ & \text { Figure 4, Figure } 10 \end{aligned}$ | 3.60 to 4.30 |  |  | 60 | 15 | 65 | ns |
|  |  |  | 2.70 to 3.60 |  |  | 65 | 15 | 70 |  |
|  |  |  | 2.30 to 2.70 |  |  | 80 | 15 | 85 |  |
|  |  |  | 1.65 to 1.95 |  | 100 |  |  |  |  |
| toff | Turn-Off Time | $\begin{aligned} & \mathrm{nB0} \text { or } \mathrm{nB} 1=1.5 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=50 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \\ & \text { Figure 4, Figure } 10 \end{aligned}$ | 3.60 to 4.30 |  |  | 55 | 5 | 60 | ns |
|  |  |  | 2.70 to 3.60 |  |  | 60 | 5 | 65 |  |
|  |  |  | 2.30 to 2.70 |  |  | 65 | 5 | 70 |  |
|  |  |  | 1.65 to 1.95 |  | 65 |  |  |  |  |
| $\mathrm{t}_{\text {BbM }}$ | Break-Before-Make Time | $\begin{aligned} & \mathrm{nB0} \text { or } \mathrm{nB} 1=1.5 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=50 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \\ & \text { Figure } 11 \end{aligned}$ | 3.60 to 4.30 |  | 3 |  | 1 |  | ns |
|  |  |  | 2.70 to 3.60 |  | 5 |  | 2 |  |  |
|  |  |  | 2.30 to 2.70 |  | 10 |  | 2 |  |  |
|  |  |  | 1.65 to 1.95 |  | 15 |  | 2 |  |  |
| Q | Charge Injection | $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{~V}_{\mathrm{S}}=0 \mathrm{~V} ; \mathrm{R}_{\mathrm{S}}=0 \Omega$ <br> Figure 14 | 1.65 to 4.30 |  | 25 |  |  |  | pC |
| OIRR | Off Isolation | $\mathrm{f}=100 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ <br> Figure 12 | 1.65 to 4.30 |  | -70 |  |  |  | dB |
| Xtalk | Crosstalk | $\mathrm{f}=100 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=50 \Omega ; \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ <br> Figure 13 | 1.65 to 4.30 |  | -70 |  |  |  | dB |
| BW | -3db Bandwidth | $\mathrm{R}_{\mathrm{L}}=50 \Omega ; \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ <br> Figure 9 | 1.65 to 4.30 |  | >50 |  |  |  | MHz |
| THD | Total Harmonic Distortion | $\mathrm{R}_{\mathrm{L}}=32 \Omega, \mathrm{~V}_{\mathrm{SW}}=2 \mathrm{~V}_{\mathrm{PP}}, \mathrm{f}=20 \mathrm{~Hz} \text { to }$ 20 kHz , $\mathrm{V}_{\text {BIAS }}=0 \mathrm{~V}$ <br> Figure 15 | 1.65 to 4.30 |  | . 06 |  |  |  | \% |

## Capacitance

| Symbol | Parameter | Conditions | $V_{c c}$ <br> (V) | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. | Min. | Max. |  |
| $\mathrm{Cin}^{\text {N }}$ | Control Pin Input Capacitance | $\mathrm{f}=1 \mathrm{MHz}$ Figure 7 | 0 |  | 2.5 |  |  |  | pF |
| Coff | B port Off Capacitance | $\mathrm{f}=1 \mathrm{MHz}$ <br> Figure 7 | 3.3 |  | 30 |  |  |  | pF |
| Con | A port On Capacitance | $\mathrm{f}=1 \mathrm{MHz}$ <br> Figure 8 | 3.3 |  | 120 |  |  |  | pF |

## Test Diagrams



Figure 3. On Resistance


Figure 5. On Leakage


Figure 7. Off Capacitance

$C_{L}$ includes test fixture and stray capacitance.

Figure 9. Bandwidth


Figure 4. Test Circuit Load


Each switch port is tested separately.
Figure 6. Off Leakage (Each Port Tested Separately)


Figure 8. On Capacitance


Figure 10. Turn-On / Turn-Off Waveforms

## Test Diagrams (Continued)



Figure 11. Break-Before-Make Timing


Figure 13. Adjacent Channel Crosstalk


Figure 14. Charge Injection Test
 environment (see AC tables for specific values).

Figure 15. Total Harmonic Distortion

## Physical Dimensions



TOP VIEW


BOTTOM VIEW
NOTES:


OPTIONAL MINIMIAL TOE LAND PATTERN


DETAIL A
PIN \#1 TERMINAL
SCALE: 2X
A. DIMENSIONS ARE IN MILLIMETERS.
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
C. DRAWING FILENAME: UMLP10Arev2

Figure 16. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

SEMICONDUCTOR

## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPowertm
Auto-SPM ${ }^{\text {™ }}$
Build it Now ${ }^{T M}$
CorePLUSTM
CorePOWERT™
CROSSVOLTTM
CTLTM
Current Transfer LogicTm
DEUXPEED ${ }^{\circ}$
Dual Cool ${ }^{\text {TM }}$
Ecospark ${ }^{\oplus}$
EfficientMax ${ }^{\text {™ }}$
EZSWITCHT**

$\underbrace{\text { E }}$
Fairchild ${ }^{\text {© }}$
Fairchild Semiconductor ${ }^{\text {© }}$
FACT Quiet Series ${ }^{\text {TM }}$
FACT ${ }^{\circ}$
FAST ${ }^{\text {© }}$
FastVCore ${ }^{\text {TM }}$
FETBench ${ }^{\text {TM }}$

FlashWriter ${ }^{\text {®* }}$
FPSTM
F-PFSTM
FRFET ${ }^{\text {® }}$
Global Power Resource ${ }^{\text {SM }}$
Green FPSTM
Green FPSTTM e-Series ${ }^{\text {TM }}$
Gmax ${ }^{\text {™ }}$
GTOTM
Intellimax'm
ISOPLANARTM
MegaBuck ${ }^{\text {TM }}$
MICROCOUPLERTM
MicroFETTM
MicroPak ${ }^{\text {TM }}$
MicroPak2 ${ }^{\text {Tm }}$
MillerDrive ${ }^{\text {TM }}$
MotionMax ${ }^{\text {TM }}$
Motion-SPM ${ }^{\text {TM }}$
OptoHiT ${ }^{\text {TM }}$
OPTOLOGIC ${ }^{\ominus}$
OPTOPLANAR ${ }^{\circledR}$
-

PDP SPM ${ }^{\text {TM }}$
Power-SPM ${ }^{\text {TM }}$
PowerTrench ${ }^{\circ}$
Power S $^{\text {TM }}$
Programmable Active Droop ${ }^{\text {™ }}$
QFET ${ }^{\text {® }}$
QS ${ }^{\text {TM }}$
Quiet Series ${ }^{\text {TM }}$
RapidConfigure ${ }^{\text {TM }}$
$0^{\text {TM }}$
Saving our world, $1 \mathrm{~mW} / \mathrm{W} / \mathrm{kW}$ at a time ${ }^{\text {TM }}$
SignalWise ${ }^{\text {TM }}$
SmartMax ${ }^{\text {TM }}$
SMART STARTTM
SPM ${ }^{\text {® }}$
STEALTH ${ }^{\text {TM }}$
SuperFETTM
SupersOTTM-3
SuperSOTTM-6
SuperSOTTM-8
SupreMOS'm
SyncFETTM
Sync-Lock ${ }^{\text {TM }}$

C SYSTEM © ${ }^{\text {® }}$
The Power Franchise ${ }^{\otimes}$

## ${ }^{\text {tha }} \mathbf{\rho}$ wer

TinyBoost ${ }^{\text {TM }}$
TinyBuckTM
TinyCalctm
TinyLogic ${ }^{\text {® }}$
TINYOPTOTM
TinyPowertm
TinyPMM ${ }^{\text {™ }}$
TinyMire ${ }^{\text {M }}$
TriFault Detect ${ }^{\text {TM }}$
TRUECURRENTTM*
$\mu$ SerDes ${ }^{\text {TM }}$


UHC ${ }^{\text {® }}$
Ultra FRFETTM
UniFETTM
VCX ${ }^{\text {TM }}$
VisualMax ${ }^{\text {TM }}$
$X S^{T M}$
*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WTHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TOIMPROVE RELIABILTY, FUNCTION, ORDESIGN. FAIRCHILDDOESNOT ASSUME ANY LIABILITY ARISING OUT OF THEAPPUCATION ORUSE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DCES IT CONVEY ANY LICENSE UNDER ITS PATENTRIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPEGFICATIONS DONOT EXPAND THE TERMS OF FAIRCHID'SWORLDMDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WTHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTORCORPORATION.

## As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semioonductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our extemal website, wowv.fairchildsemi.com, under Sales Support.
Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Faichild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by oountry on our web page ated above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide ary warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and enouurage our customers to do their part in stopping this practioe by buying direct or from authorized distributors.

PRODUCT STA TUS DEFINITIONS

## Definition of Terms

| Datasheet Identification | Product Status |  |
| :--- | :--- | :--- |
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in <br> any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild <br> Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes <br> at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. <br> The datasheet is for reference information only. |

Rev. 146

