FS84; FS85

Fail-safe system basis chip with multiple SMPS and LDO

Rev. 1.0 — 19 December 2018 Product brief

SAFE ASSURE by NXP

1 About this document

This Product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

2 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible.

The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

3 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.

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- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

4 Applications

- Radar
- Vision
- ADAS domain controller
- Radio
- V2x
- Infotainment

5 Ordering information

Table 1. Ordering information

Type number [1]	Package		
	Name	Description	Version
PC33FS8500**A0**ES	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT684-21
PC33FS8510**A0**ES			
PC33FS8520**A0**ES			
PC33FS8530**A0**ES			
PC33FS8400**A0**ES			
PC33FS8410**A0**ES			
PC33FS8420**A0**ES			
PC33FS8430**A0**ES			

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5.1 Ordering options

Table 2. Ordering options

Family	Part number [1][2]	BUCK1	BUCK2	BUCK3	ASIL
FS84 [3]	PC33FS8400**A0**ES	Yes	No	No	B
	PC33FS8410**A0**ES	Yes	No	Yes	B
	PC33FS8420**A0**ES	Yes	Yes	No	B
	PC33FS8430**A0**ES	Yes	Yes	Yes	B
FS85 [4]	PC33FS8500**A0**ES	Yes	No	No	D
	PC33FS8510**A0**ES	Yes	No	Yes	D
	PC33FS8520**A0**ES	Yes	Yes	No	D
	PC33FS8530**A0**ES	Yes	Yes	Yes	D

[1] Part number OTP customization suffix (other than BUCK regulators and ASIL level): **from A0 to Z9**
[2] Part number delivery suffix: add R2 for tape and reel
[3] FS84 (ASIL B) customer samples availability: **now**
[4] FS85 (ASIL D) customer samples availability: **now**

6 Block diagram

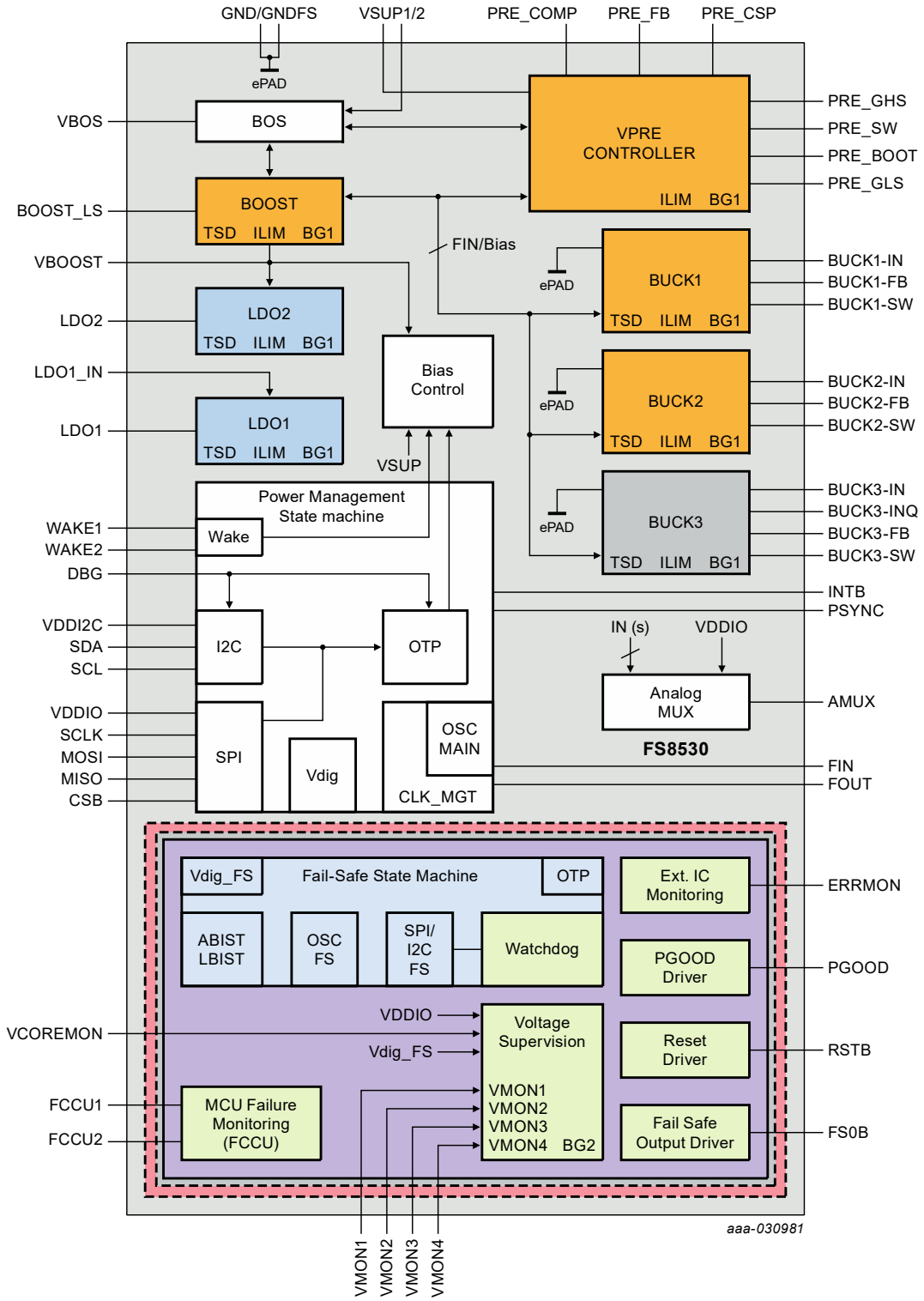


Figure 1. Block diagram of FS8530

7 Simplified application diagram

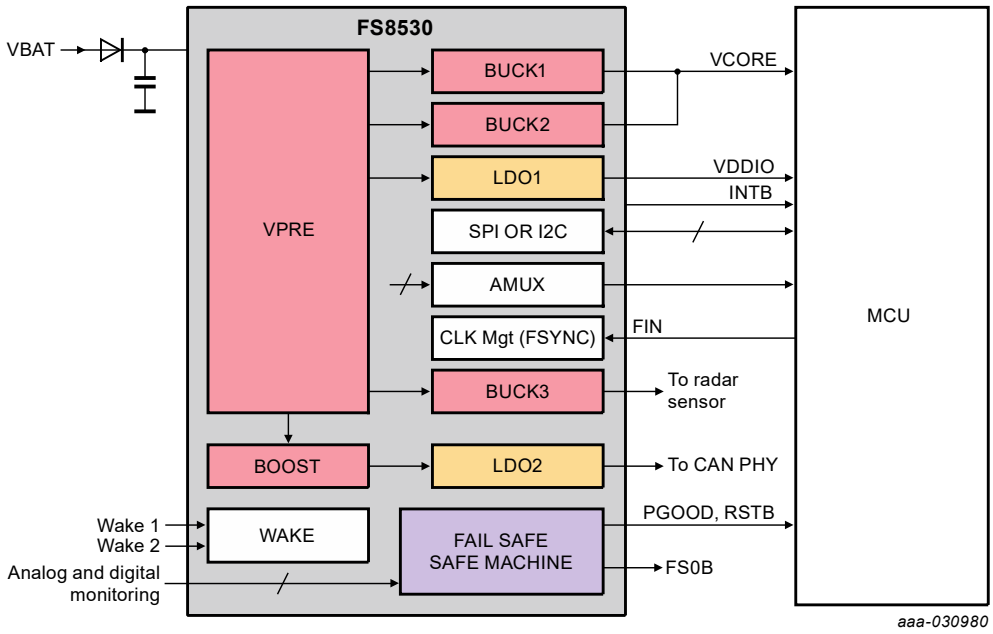


Figure 2. FS8530 superset device of the family

8 Pinning information

8.1 Pinning

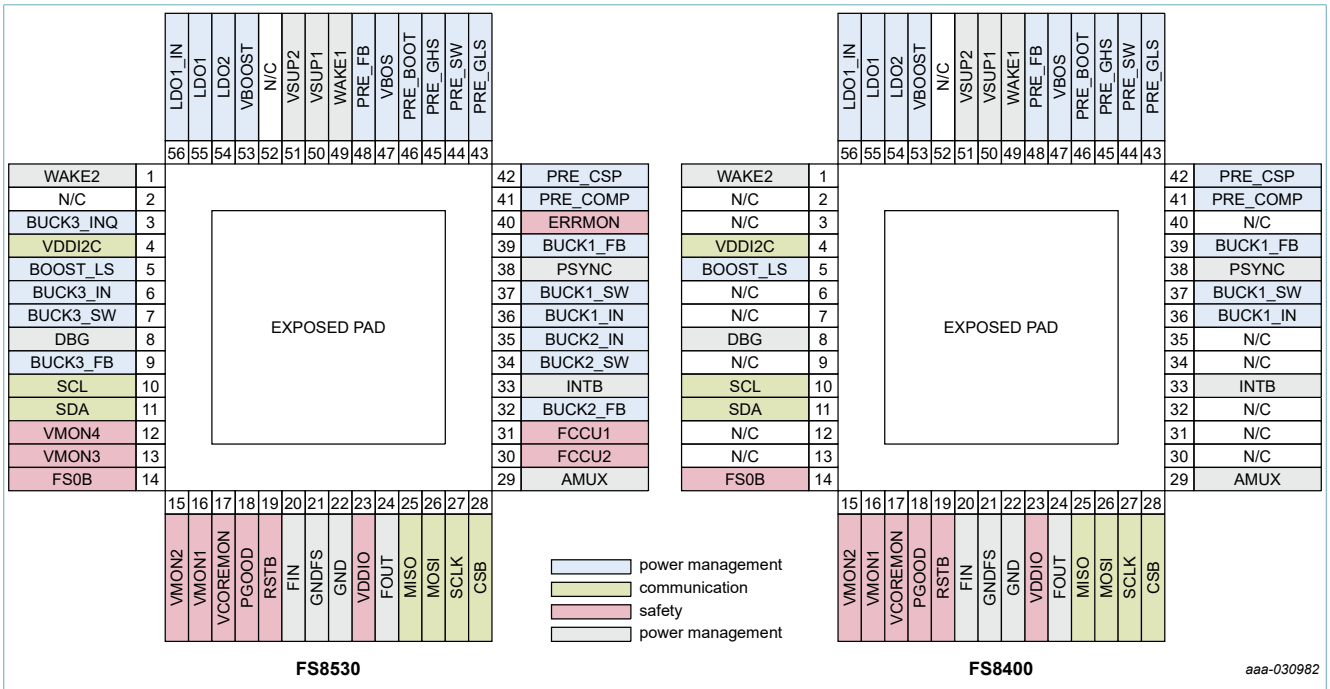


Figure 3. Pin configuration

8.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description [1]
WAKE2	1	A_IN / D_IN	Wake-up input 2 An external serial resistor is required if WAKE2 is a global pin
N/C	2	N/C	Not connected pin
BUCK3_INQ	3	A_IN	Low voltage Buck3 quiet input voltage
VDDI2C	4	A_IN	Input voltage for I2C buffers
BOOST_LS	5	A_IN	Boost low-side drain of internal MOSFET
BUCK3_IN	6	A_IN	Low voltage Buck3 input voltage
BUCK3_SW	7	A_OUT	Low voltage Buck3 switching node
DBG	8	A_IN	Debug mode entry
BUCK3_FB	9	A_IN	Low voltage Buck3 voltage feedback
SCL	10	D_IN	I2C bus Clock input
SDA	11	D_IN/OUT	I2C bus Bidirectional data line
VMON4	12	A_IN	Voltage monitoring input 4
VMON3	13	A_IN	Voltage monitoring input 3
FS0B	14	D_OUT	Fail-safe output 0 Active low Open drain structure
VMON2	15	A_IN	Voltage monitoring input 2
VMON1	16	A_IN	Voltage monitoring input 1
VCOREMON	17	A_IN	VCORE monitoring input: Must be connected to Buck1 output voltage
PGOOD	18	D_OUT	Power good output Active low Pull up to VDDIO mandatory
RSTB	19	D_OUT	Reset output Active low The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault condition. Pull up to VDDIO mandatory
FIN	20	D_IN	Frequency synchronization input
GNDFS	21	GND	Fail-safe ground
GND	22	GND	Main ground
VDDIO	23	A_IN	Input voltage for SPI, FOUT and AMUX buffers Allow voltage compatibility with MCU I/Os
FOUT	24	D_OUT	Frequency synchronization output
MISO	25	D_OUT	SPI bus Master input slave output
MOSI	26	D_IN	SPI bus Master output slave Input
SCLK	27	D_IN	SPI bus Clock input
CSB	28	D_IN	Chip select (active low)

Symbol	Pin	Type	Description [1]
AMUX	29	A_OUT	Multiplexed output to connect to MCU ADC Selection of the analog parameter through SPI or I2C
FCCU2	30	D_IN	MCU error monitoring input 2
FCCU1	31	D_IN	MCU error monitoring input 1
BUCK2_FB	32	A_IN	Low voltage Buck2 voltage feedback
INTB	33	D_OUT	Interrupt output
BUCK2_SW	34	A_OUT	Low voltage Buck2 switching node
BUCK2_IN	35	A_IN	Low voltage Buck2 input voltage
BUCK1_IN	36	A_IN	Low voltage Buck1 input voltage
BUCK1_SW	37	A_OUT	Low voltage Buck1 switching node
PSYNC	38	D_IN/OUT	Power synchronization input/output
BUCK1_FB	39	A_IN	Low voltage Buck1 voltage feedback
ERRMON	40	D_IN	External IC error monitoring input
PRE_COMP	41	A_IN	VPRE compensation network
PRE_CSP	42	A_IN	VPRE positive current sense input
PRE_GLS	43	A_OUT	VPRE low-side gate driver for external MOSFET
PRE_SW	44	A_OUT	VPRE switching node
PRE_GHS	45	A_OUT	VPRE high-side gate driver for external MOSFET
PRE_BOOT	46	A_IN/OUT	VPRE bootstrap capacitor
VBOS	47	A_OUT	Best of supply output voltage
PRE_FB	48	A_IN	VPRE voltage feedback and negative current sense input
WAKE1	49	A_IN / D_IN	Wake up input 1 An external serial resistor is required if WAKE1 is a global pin
VSUP1	50	A_IN	Power supply 1 of the device An external reverse battery protection diode in series is mandatory
VSUP2	51	A_IN	Power supply 2 of the device An external reverse battery protection diode in series is mandatory
N/C	52	N/C	Not connected pin
VBOOST	53	A_IN	VBOOST voltage feedback
LDO2	54	A_OUT	Linear regulator 2 output voltage
LDO1	55	A_OUT	Linear regulator 1 output voltage
LDO1_IN	56	A_IN	Linear regulator 1 input voltage
EP	57	GND	Expose pad Must be connected to GND

[1] See Section 9 for connection of unused pins.

9 Connection of unused pins

Table 4. Connection of unused pins

Pin	Name	Type	Connection if not used
1	WAKE2	A_IN / D_IN	External pull down to GND
2	N/C	N/C	Open

Pin	Name	Type	Connection if not used
3	BUCK3_INQ	A_IN	Open
4	VDDI2C	A_IN	Open
5	BOOST_LS	A_IN	See VBOOST not populated
6	BUCK3_IN	A_IN	Open
7	BUCK3_SW	A_OUT	Open
8	DBG	A_IN	**Connection mandatory**
9	BUCK3_FB	A_IN	Open – 1.5 MΩ internal resistor bridge pull down to GND
10	SCL	D_IN	External pull down to GND
11	SDA	D_IN/OUT	External pull down to GND
12	VMON4	A_IN	Open – 2 MΩ internal pull down to GND, OTP_VMON4_EN=0
13	VMON3	A_IN	Open – 2 MΩ internal pull down to GND, OTP_VMON3_EN=0
14	FS0B	D_OUT	Open – 400 kΩ internal pull down to GND
15	VMON2	A_IN	Open – 2 MΩ internal pull down to GND, OTP_VMON2_EN=0
16	VMON1	A_IN	Open – 2 MΩ internal pull down to GND, OTP_VMON1_EN=0
17	VCOREMON	A_IN	**Connection mandatory**
18	PGOOD	D_OUT	**Connection mandatory**
19	RSTB	D_OUT	**Connection mandatory**
20	FIN	D_IN	External pull down to GND
21	GNDFS	GND	**Connection mandatory**
22	GND	GND	**Connection mandatory**
23	VDDIO	A_IN	**Connection mandatory**
24	FOUT	D_OUT	Open – push pull structure
25	MISO	D_OUT	Open – push pull structure
26	MOSI	D_IN	Open – 450 kΩ internal pull up to VDDIO
27	SCLK	D_IN	External pull down to GND
28	CSB	D_IN	Open – 450 kΩ internal pull up to VDDIO
29	AMUX	A_OUT	Open
30	FCCU2	D_IN	Open – 450 kΩ internal pull up to VDDIO
31	FCCU1	D_IN	Open – 450 kΩ internal pull down to GND
32	BUCK2_FB	A_IN	Open – 1.5 MΩ Internal resistor bridge pull down to GND
33	INTB	D_OUT	Open – 10 kΩ internal pull up to VDDIO
34	BUCK2_SW	A_OUT	Open
35	BUCK2_IN	A_IN	Open
36	BUCK1_IN	A_IN	**Connection mandatory**
37	BUCK1_SW	A_OUT	**Connection mandatory**
38	PSYNC	D_IN/OUT	External pull up to VBOS
39	BUCK1_FB	A_IN	**Connection mandatory**
40	ERRMON	D_IN	External pull down to GND

Pin	Name	Type	Connection if not used
41	PRE_COMP	A_IN	See VPRE not populated
42	PRE_CSP	A_IN	See VPRE not populated
43	PRE_GLS	A_OUT	See VPRE not populated
44	PRE_SW	A_OUT	See VPRE not populated
45	PRE_GHS	A_OUT	See VPRE not populated
46	PRE_BOOT	A_IN/OUT	See VPRE not populated
47	VBOS	A_OUT	**Connection mandatory**
48	PRE_FB	A_IN	See VPRE not populated
49	WAKE1	A_IN / D_IN	External pull down to GND
50	VSUP1	A_IN	**Connection mandatory**
51	VSUP2	A_IN	**Connection mandatory**
52	N/C	N/C	Open
53	VBOOST	A_OUT	See VBOOST not populated
54	LDO2	A_OUT	Open – power sequence slot 7, OTP_LDO1S[2:0] = ‘111’
55	LDO1	A_OUT	Open – power sequence slot 7, OTP_LDO2S[2:0] = ‘111’
56	LDO1_IN	A_IN	Open
57	EP	GND	**Connection mandatory**

10 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage ratings					
VSUP1/2	DC voltage	power supply VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC voltage	WAKE1,2 pins; external serial resistor mandatory	−1.0	60	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	60	V
VMONx, FS0B	DC voltage	VMON1,2,3,4, VCOREMON, FS0B pins	−0.3	60	V
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	−0.3	65.5	V
DBG	DC voltage	DBG pin	−0.3	10	V
BOOST_LS	DC voltage	BOOST_LS pin	−0.3	8.5	V
VBOOST, LDO1_IN	DC voltage	VBOOST, LDO1_IN pins	−0.3	6.5	V
All other pins	DC voltage	at all other pins	−1.0	5.5	V
Current ratings					
I_WAKE	Maximum current capability	WAKE1,2	−5.0	5.0	mA
I_SUP	Maximum current capability	VSUP1,2	−5.0	—	mA

11 Electrostatic discharge

11.1 Human body model (JESD22/A114)

The device is protected up to 2 kV, according to the human body model at 100 pF and 1.5 kΩ. This protection is ensured at all pins.

11.2 Charged device model (JESD22/C101)

The device is protected up to 500 V, according to the charged device model. This protection is ensured at all pins.

Additionally, the device is protected up to 750 V at the corner pins, according to the charged device model.

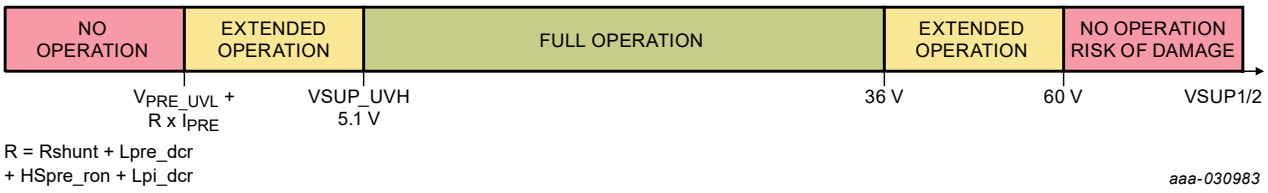
11.3 Discharged contact test

The device is protected up to 8 kV, according to the following discharged contact tests.

Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2, FS0B pins.

12 Operating range



Assumptions

R = 100 mΩ (Rshunt = 10 mΩ, Lpre_dcr = 30 mΩ, HSpre_ron = 30 mΩ, Lpi_dcr = 30 mΩ)
Ipre = 3.0 A
V_{RBD} = 0.5 V
VBAT_min = 3.5 V when VPRE = V_{PRE_UVL}

Figure 4. Operating range

- Below VSUP_UVH threshold, the extended operation range depends on VPRE output voltage configuration and external components.
  - When VPRE is configured at 5.0 V, VPRE may not remain in its regulation range
  - VSUP minimum voltage depends on external components (R) and application conditions (I_{PRE})
- The FS85/FS84 maximum continuous operating voltage is 36 V.
- The FS85/FS84 has been validated at 48 V for limited duration of 15 minutes at room temperature to satisfy the jump start requirement of 24 V applications.
- The FS85/FS84 can sustain 24 V load dump at 58 V without external protection.

13 Thermal ratings

Table 6. Thermal ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient	2s2p circuit board [1]	—	31	°C/W
$R_{\theta JA}$	Thermal resistance junction to ambient	2s6p circuit board [1]	—	23	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s2p circuit board [1]	—	15	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s6p circuit board [1]	—	10	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom	between the die and the solder pad on the bottom of the package [1]	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal resistance junction to package top	between package top and the junction temperature [1]	—	3	°C/W
T_A	Ambient temperature		−40	125	°C
T_J	Junction temperature		−40	150	°C
T_{STG}	Storage temperature		−55	150	°C

[1] per JEDEC JESD51-2 and JESD51-8

14 Characteristics

Table 7. Electrical characteristics

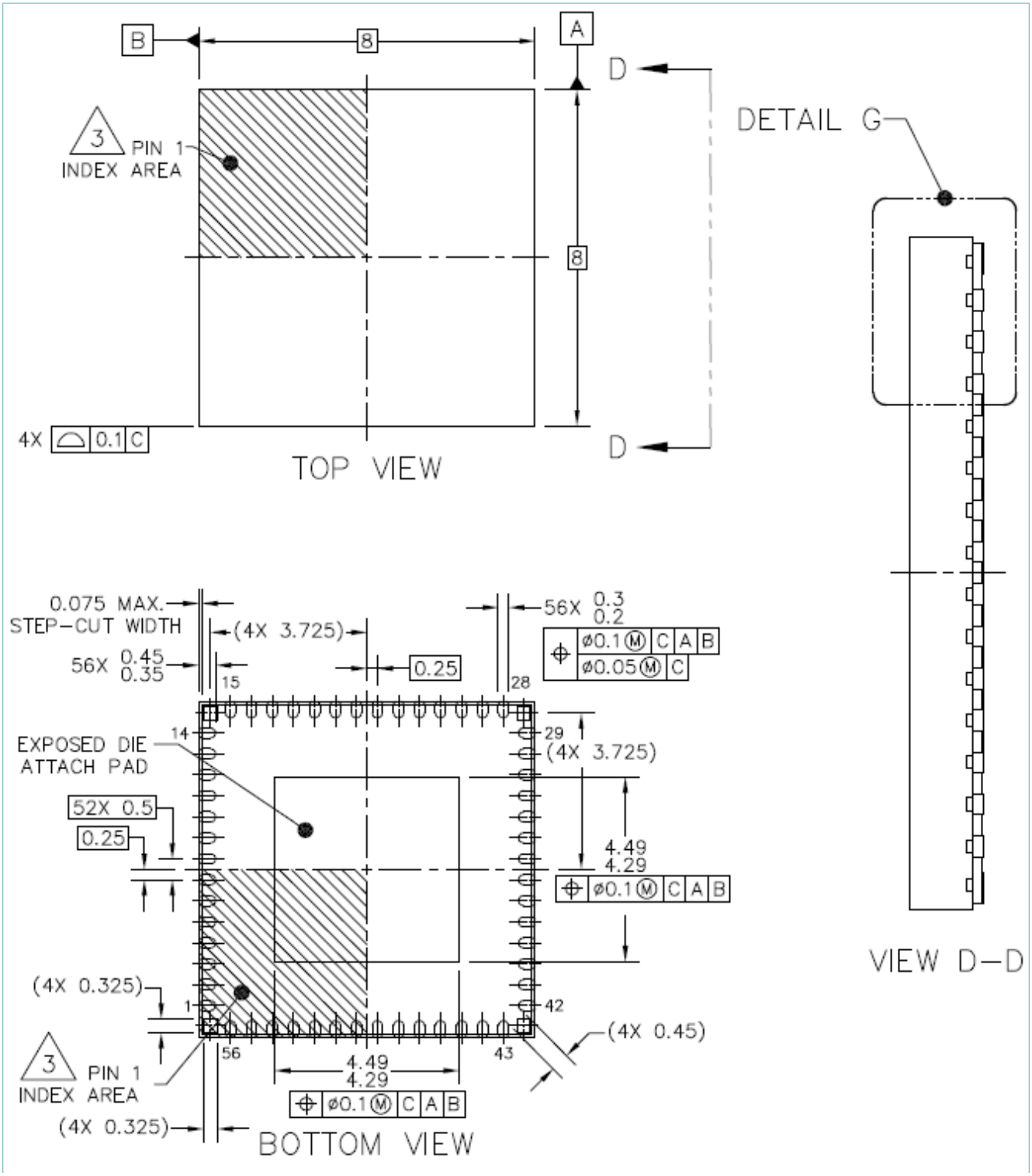
T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

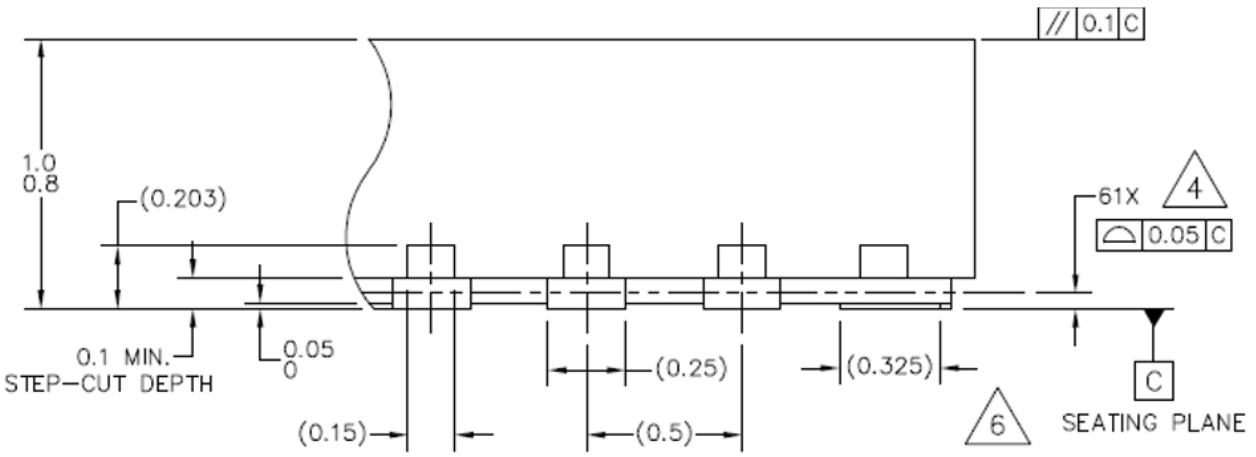
Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
I_{SUP_NORMAL}	Current in Normal mode, all regulators ON (I_{OUT} = 0)	—	15	25	mA
$I_{SUP\_STANDBY}$	Current in Normal mode, all regulators OFF	—	5	10	mA
I_{SUP_OFF1}	Current in OFF mode, T_A < 85 °C	—	10	15	µA
I_{SUP_OFF2}	Current in OFF mode, T_A = 125 °C	—	—	25	µA

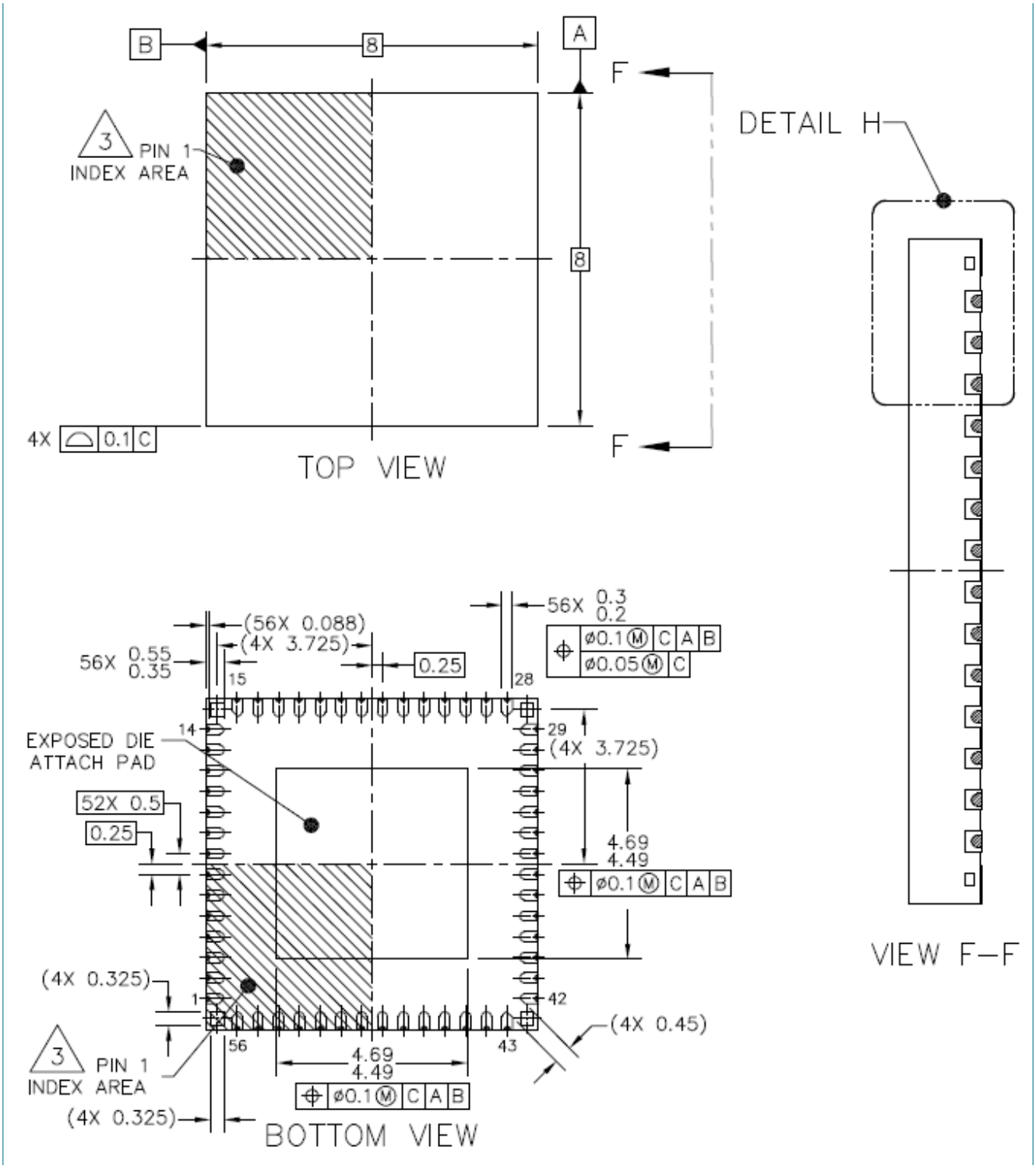
15 Package information

FS85/FS84 package is a QFN (sawn), thermally enhanced wettable flanks, 8 x 8 x 0.85 mm, 0.5 mm pitch, 56 pins. The assembly can be done at two different NXP assembly sites with slight wettable flank difference but sharing the same PCB footprint.

16 Package outline







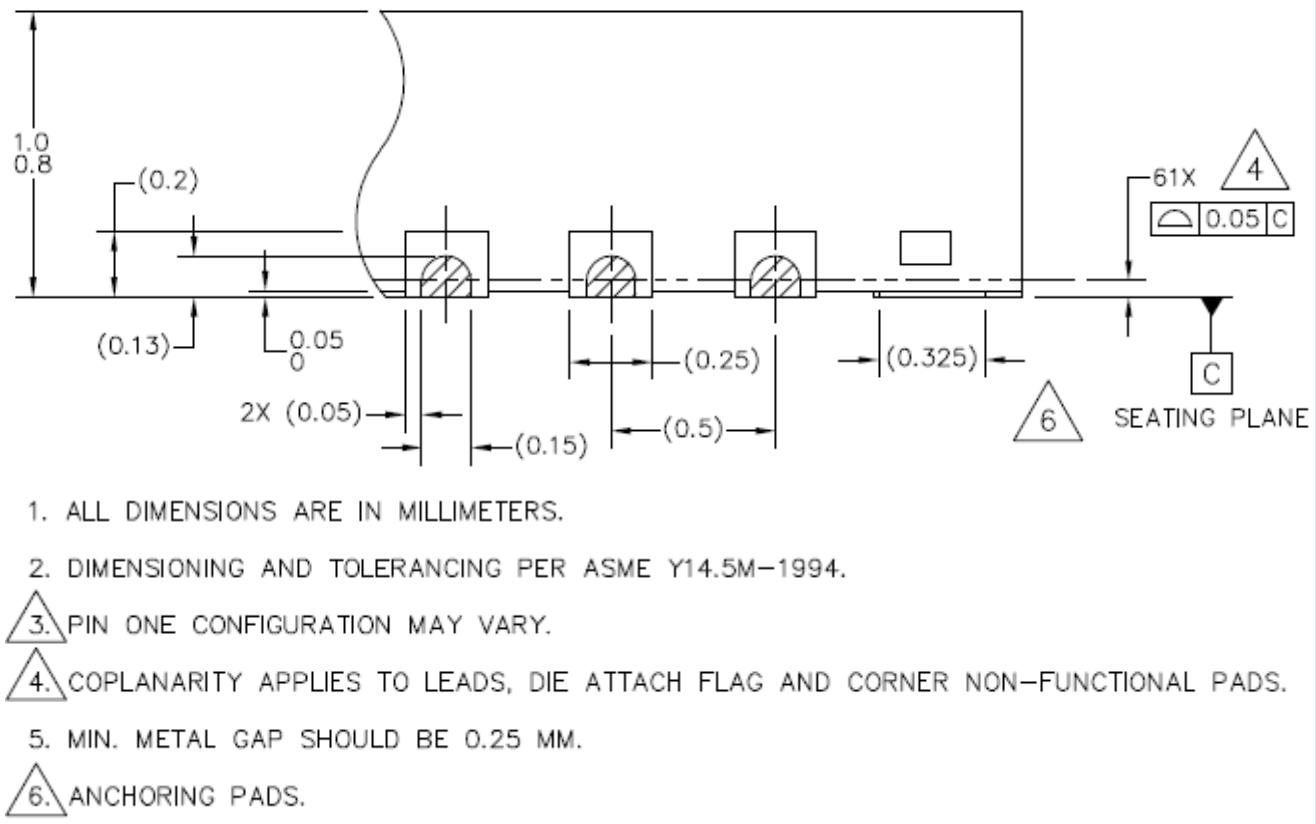


Figure 5. Package outline for FS85/FS84

17 References

[1] **FS85_PDTCALC**[1] — VPRE compensation network calculation and power dissipation tool (Excel file)

[2] **FS85_OTP_Mapping**[1] — OTP programming configuration (Excel file)

[3] **FS85_FMEDA**[1] — FMEDA analysis

[4] **FS85_Safety_Manual**[1] — Safety manual

[5] **FS85_PCB_Apps_Note**[1] — PCB layout guidelines

[6] **FS85_VPRE_Simplis_Model**[1] — Simplis model for stability and transient simulations

[7] **Schematic**[1] — Reference schematic in Cadence and PDF formats

[8] **Layout**[1] — Reference layout in Cadence format

[9] **EVB**[1] — Evaluation board (EVB)

[10] **FlexGUI**[1] — Graphical user interface to be used with the EVB

[1] Contact NXP sales representative.

18 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PB_FS84_FS85 v.1.0	20181219	Product brief	-	-

19 Legal information

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