FAIRCHILD SEMICONDUCTOR®

November 2012

FPF1504
Advanced Load Management Switch

Features

- 1.0 V to 3.6 V Input Voltage Operating Range
- Typical $R_{DS(ON)}$:
  - 15 mΩ at V_{IN}=3.3 V
  - 20 mΩ at V_{IN}=1.8 V
  - 55 mΩ at V_{IN}=1.0 V
- Slew Rate Control with t_R: 130 µs
- Output Discharge Function
- Low <1 µA Quiescent Current at V_{ON}=V_{IN}
- ESD Protected: 4000 V HBM, 2000 V CDM
- GPIO/CMOS-Compatible Enable Circuitry

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Digital Cameras
- Advanced Notebook, UMPC, and MID
- Portable Medical Devices
- GPS and Navigation Equipment

Description

The FPF1504 is a low-R_{DS} P-channel MOSFET load switch of the IntelliMAX™ family. Integrated slew-rate control prevents excessive inrush current from the supply rails with capacitive loads common in power applications. In addition, the FPF1504 features output discharge capability.

The input voltage range operates from 1.0 V to 3.6 V to fulfill today's mobile device supply requirements. Switch control is by a logic input (ON pin) capable of interfacing directly with low-voltage CMOS control signals and GPIOs in embedded processors.

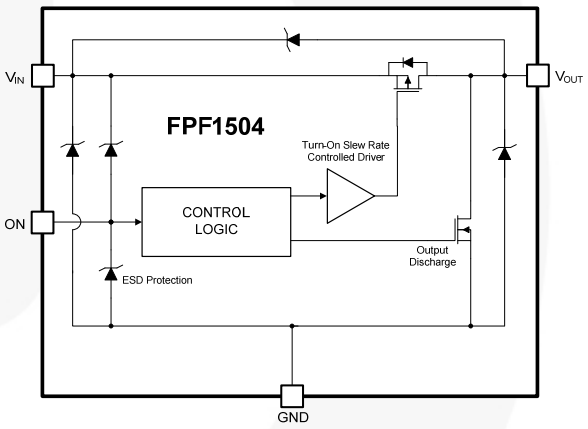


Figure 1. Block Diagram

Ordering Information

Part Number	Part Marking	$R_{DS(ON)}$ (Typical) At 1.8V_{IN}	Input Buffer	Output Discharge	ON Pin Activity	t_R	Package
FPF1504UCX	G4	20 mΩ	CMOS	YES	Active HIGH	130 µs	4-Ball, Wafer-Level Chip-Scale Package (WLCSP), 1.0 x 1.0 mm, 0.5 mm Pitch
FPF1504BUCX (Preliminary)	G4	20 mΩ	CMOS	YES	Active HIGH	130 µs	4-Ball, WLCSP, with Backside Laminate (BSL), 1.0 x 1.0 mm, 0.5 mm Pitch

Application Diagram

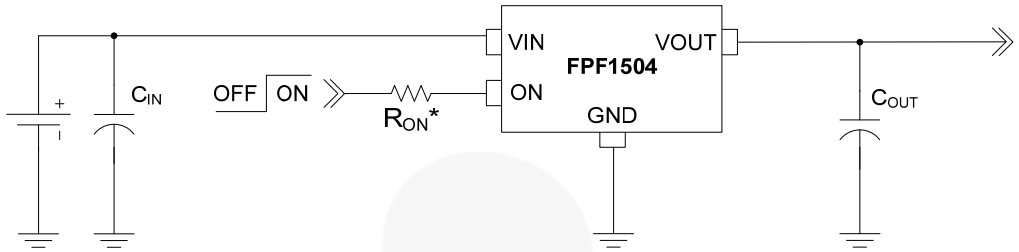


Figure 2. Typical Application

Notes:
1. C_{IN}=1μF, X5R, 0603, for example Murata GRM185R60J105KE26.
2. C_{OUT}=1μF, X5R, 0805, for example Murata GRM216R61A105KA01.
3. R_{ON} =470 kΩ, typical recommended. * Required for applications with $V_{IH} > V_{IN}$.

Pin Configurations

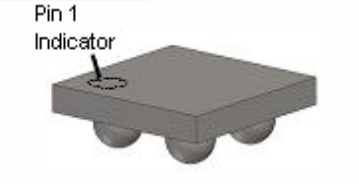


Figure 3. 1 x 1 mm WLCSP Bumps Facing Down

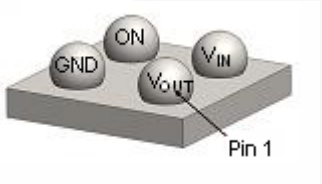


Figure 4. 1 x 1 mm WLCSP Bumps Facing Up

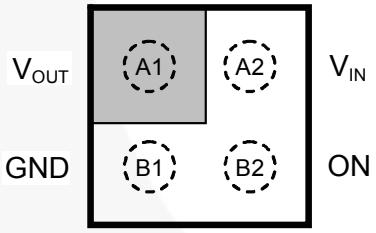


Figure 5. Pin Assignments (Top View)

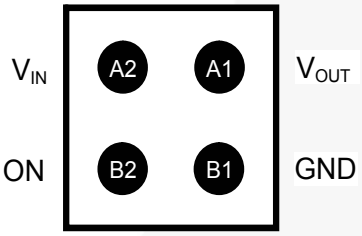
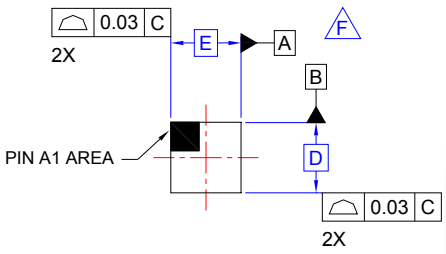


Figure 6. Pin Assignments (Bottom View)

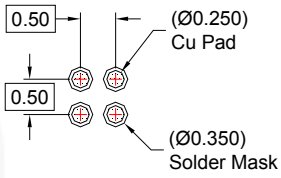
Pin Definitions

Pin #	Name	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Supply Input; Input to the Power Switch
B1	GND	Ground
B2	ON	ON/OFF Control, Active HIGH

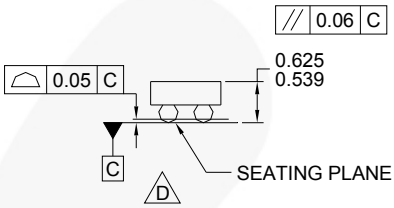
Physical Dimensions

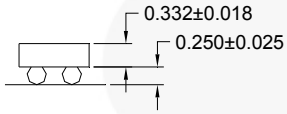


TOP VIEW

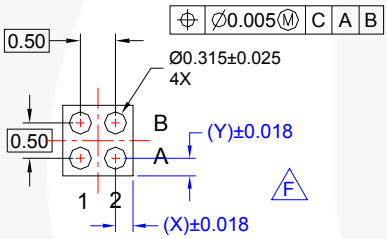


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC004ABrev2.

Figure 25. 4-Ball, 1.0 x 1.0mm Wafer-Level Chip Scale (WLCSP) Packaging

Product-Specific Dimensions

Product	D	E	X	Y
FPF1504UCX	960 µm ±30 µm	960 µm ±30 µm	0.230 mm	0.230 mm
FPF1504BUCX (Preliminary)	960 µm ±30 µm	960µm ±30µm	0.230 mm	0.230 mm

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