# FPD87310

***FPD87310 Universal Interface XGA Panel Timing Controller with RSDS (Reduced Swing Differential Signaling) and FPD-Link***

Literature Number: SNOS466

National Semiconductor

**PRELIMINARY**

May 2000

# FPD87310
# Universal Interface XGA Panel Timing Controller with RSDS™ (Reduced Swing Differential Signaling) and FPD-Link

## General Description

The FPD87310 Panel Timing Controller is an integrated FPD-Link + RSDS + TFT-LCD Timing Controller. It resides on the Flat Panel Display and provides the interface signal routing and Timing Control between Graphics or Video Controllers and a TFT-LCD system. FPD-Link, a low power, low EMI (ElectroMagnetic Interference) interface is used between this Controller and the Host system.

A RSDS (Reduced Swing Differential Signaling) Column Driver interface is used between the Timing Controller and the Column Drivers.

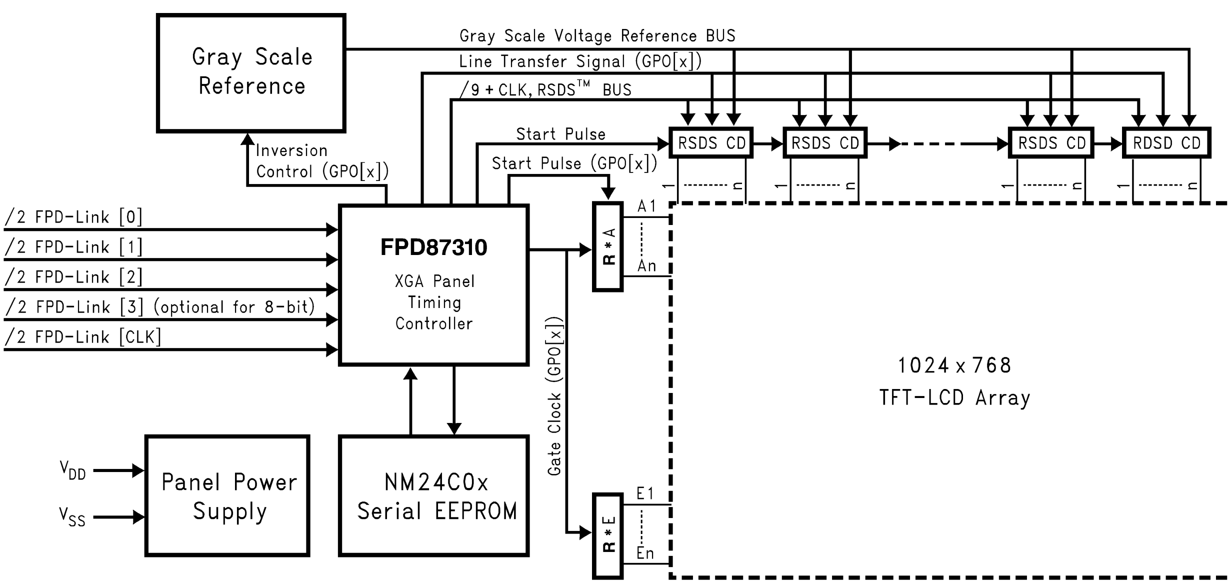
Programmable, General Purpose Outputs provide Row and Column Driver control. The FPD87310 is configured via metal mask initialization value or an optional external serial EEPROM. Reserved space in the EEPROM is available for display identification information. The system can access the EEPROM to read the display identification data or program initialization values used by the FPD87310.

This single 9-bit+CLK differential bus conveys the 18 bits color data for XGA panels at 130 Mb/s when using VESA 60 Hz standard timing.

## Features

- RSDS (Reduced Swing Differential Signaling) Column Driver bus for low power and reduced EMI
- Drives RSDS Column Drivers at 130 Mb/s with a 65 MHz clock
- 6- or 8-bit LVDS Video System Interface (FPD-Link)
- 10 General Purpose Outputs for Column/Row Drivers
- Optional EEPROM programming allows fine tuning in development and production environments
- Selectable dual initialization value sets to share parts for the different model panel module
- Ability to drive XGA/SVGA TFT-LCD Systems
- Narrow 9-bit+CLK differential Column Driver Bus minimizes width of Source PCB
- CMOS circuitry operates from a 3.3V supply
- Supports Graphics Controllers with spread spectrum interface featurefor lower EMI

## System Diagram

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | 4V |
| DC Input Voltage ($V_{IN}$) | −0.3V to 4.0V |
| DC Output Voltage ($V_{OUT}$) | −0.3V to $V_{DD}$ +0.3V |
| Storage Temperature Range ($T_{STG}$) | −65˚C to +150˚C |
| Lead Temperature ($T_L$) (Soldering 10 sec.) | 260˚C |
| ESD Rating: | |
| HBM | ≥2kV |
| MM | ≥200V |

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 3.0 | 3.6 | V |
| Operating Temp Range ($T_A$) | 0 | 70 | ˚C |
| Operating Frequency ($f_{CLK}$) | | 67 | MHz |

## Electrical Characteristics

**DC ELECTRICAL CHARACTERISTICS** $V_{DD}$ = 3.3V ± 0.3V, $V_{SS}$ = 0.0V (Unless otherwise specified).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Minimum High Level Output Voltage | $V_{DD}$ = 3.3V, $I_{OH}$ = 8 mA | 2.2 | | | V |
| $V_{OL}$ | Maximum Low Level Output Voltage | $V_{DD}$ = 3.3V, $I_{OL}$ = 8 mA | | | 0.8 | V |
| $V_{IH}$ | Minimum High Level Input Voltage | | 2.0 | | | V |
| $V_{IL}$ | Maximum Low Level Input Voltage | | | | 0.8 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | −10 | | 10 | µA |
| $I_{DD}$ | Supply Current | $f_{CLK}$ = 65 MHz, $R_{PI}$ = 13kΩ, See *Figure 1* | | | 140 | mA |

**FPD-Link (LVDS) RECEIVER INPUT** (RxCLK+/−, RxIN[y]+/−; y = 0, 1, 2, 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH_{LVDS}}$ | LVDS Input High Level Threshold Voltage | $V_{CM_{LVDS}}$ = +1.2V (Note 2) | | | +100 | mV |
| $V_{IL_{LVDS}}$ | LVDS Input Low Level Threshold Voltage | $V_{CM_{LVDS}}$ = +1.2V (Note 2) | −100 | | | mV |
| $V_{CM_{LVDS}}$ | LVDS Input Common Mode Voltage Range | $V_{DIFF_{LVDS}}$ = ± 100 mV (Note 2) | | 1.25 | | V |
| $I_{IN}$ | LVDS Input Current | $V_{IN}$ = +2.4V, $V_{CC}$ = 3.6V | | | ±10 | µA |
| | | $V_{IN}$ = 0V, $V_{CC}$ = 3.6V | | | ±10 | µA |

**RSDS TRANSMITTER OUTPUT** (RSCKP/N, RSx[y]P/N; x = R, G, B y = 0, 1, 2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH_{RSDS}}$ | RSDS High Differential Output Voltage | $V_{CM_{RSDS}}$ = +1.3V ± 5% (Note 3) | +150 | +200 | | mV |
| $V_{OL_{RSDS}}$ | RSDS Low Differential Output Voltage | $V_{CM_{RSDS}}$ = +1.3V ± 5% (Note 3) | | −200 | −150 | mV |
| $V_{CM_{RSDS}}$ | RSDS Common Mode Output Voltage | $V_{DIFF_{RSDS}}$ = ± 200 mV (Note 3) | | 1.3 | | V |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** $V_{CM_{LVDS}} = (V_{RxCLK+} + V_{RxCLK-})/2$ or $V_{CM_{LVDS}} = (V_{RxIN[y]+} + V_{RxIN[y]-})/2$; y = 0, 1, 2, 3.

$V_{DIFF_{LVDS}} = V_{RxCLK+} - V_{RxCLK-}$ or $V_{DIFF_{LVDS}} = V_{RxIN[y]+} - V_{RxIN[y]-}$; y = 0, 1, 2, 3

**Note 3:** $V_{CM_{RSDS}} = (V_{RSCKP} + V_{RSCKN})/2$ or $V_{CM_{RSDS}} = (V_{RSx[y]P} + V_{RSx[y]N})/2$; x = R, G, B y = 0, 1, 2

$V_{DIFF_{RSDS}} = V_{RSCKP} - V_{RSCKN}$ or $V_{DIFF_{RSDS}} = V_{RSx[y]P} - V_{RSx[y]N}$; x = R, G, B y = 0, 1, 2

The Termination Resister for differential line between positive and negative output is 100Ω.

Pin "PI" is connected to ground by 13.0 kΩ. This parameter is Guaranteed by Design.

## AC Electrical Characteristics

**FPD-Link INPUT TIMING** $V_{DD}$ = 3.3V ± 0.3V, $V_{SS}$ = 0.0V (Unless otherwise specified).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| RPLLS | FPD-Link Receiver Phase Lock Loop Wake-up Time | | | | 10 | ms |
| RSKM | RxIN Skew Margin (Note 4) | $V_{DD}$ = 3.3V, $T_A$ = 25˚C | 400 | | | ps |

**Note 4:** Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs.

This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window) allowing for FPD-Link LVDS cable skew dependent on type/length of cable, and source clock (FPD-Link Transmitter TxCLK IN) jitter.

RSKM ≤ cable skew (type, length) + source clock jitter (cycle to cycle). The specified RSKM minimum assumes a TPPOSmax limit of 200ps (65MHz). This parameter is Guaranteed by Design.

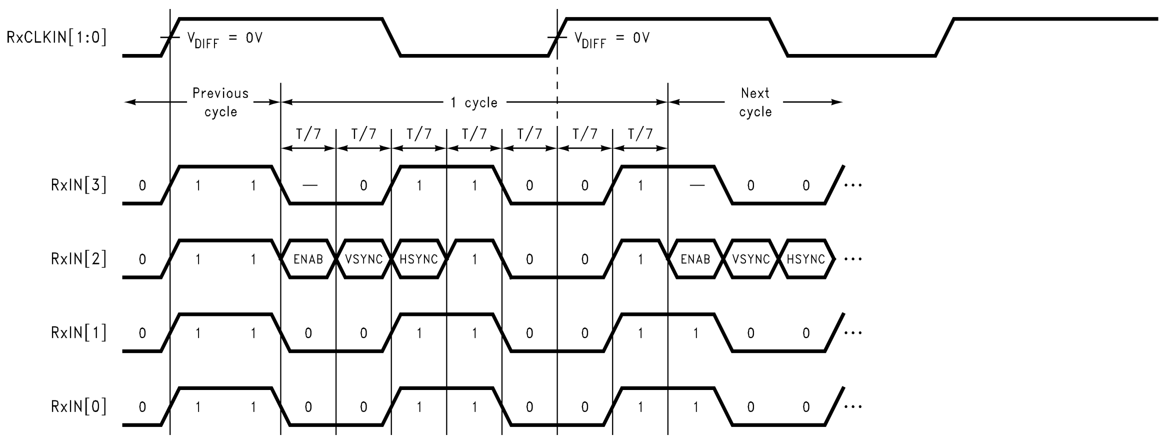
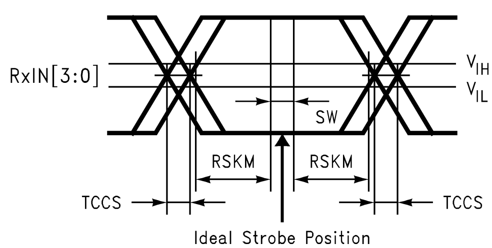



**FIGURE 1. FPD87310 Input $I_{DD}$ Test Pattern**




| | |
|---|---|
| SW | Setup and Hold Time (internal data sampling window) |
| TCCS | Transmitter Output Skew |
| RSKM | ≥ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) |
| Cable Skew | Typically 10 ps - 40 ps per foot. |

**FIGURE 2. FPD87310 (FPD-Link Receiver) Input Skew Margin**

## AC Electrical Characteristics (Continued)

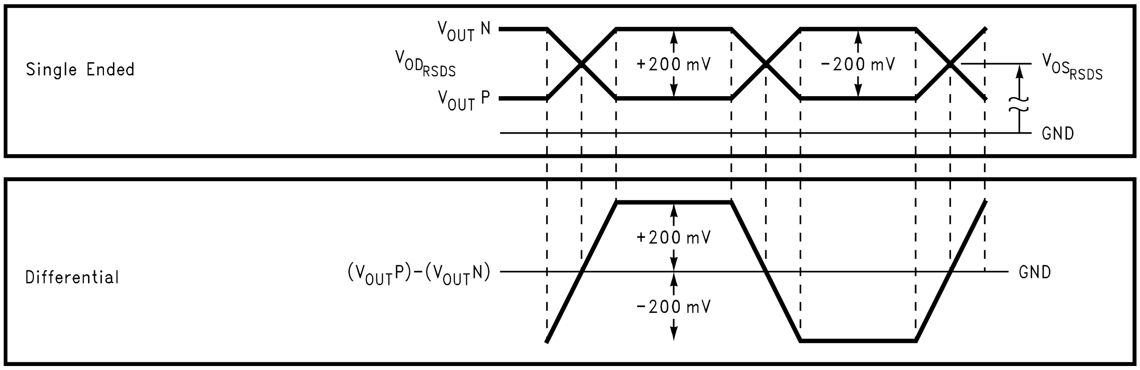



**FIGURE 3. RSDS Waveform - Single Ended and Differential**

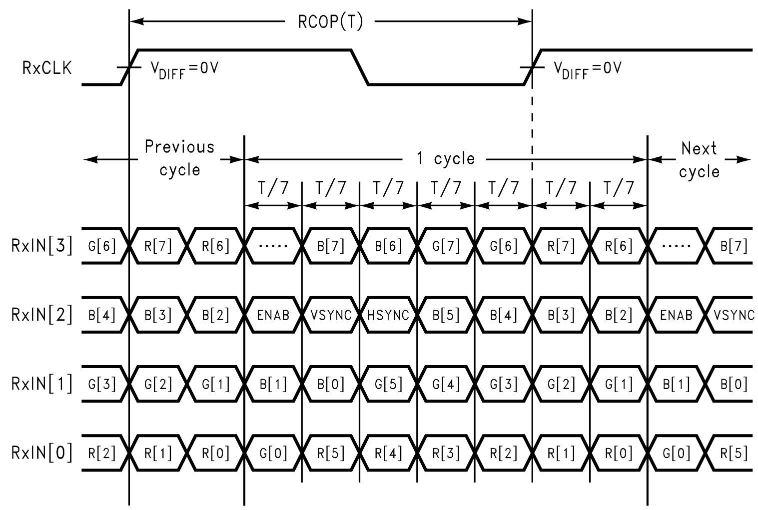



**FIGURE 4. FPD87310 (FPD-Link Receiver) Input Data Mapping**

Note: R/G/B [7] are the MSBs and R/G/B [0] are LSBs. This mapping is specific to this device only. Transmitters must be able to support this mapping for inter-operability.

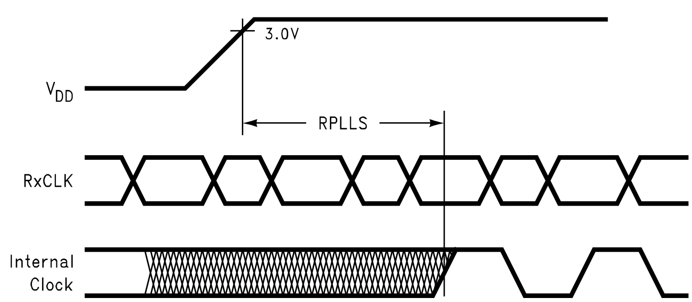



**FIGURE 5. FPD87310 (FPD-Link Receiver) Phase Lock Loop Wake-up Time**

## AC Electrical Characteristics (Continued)

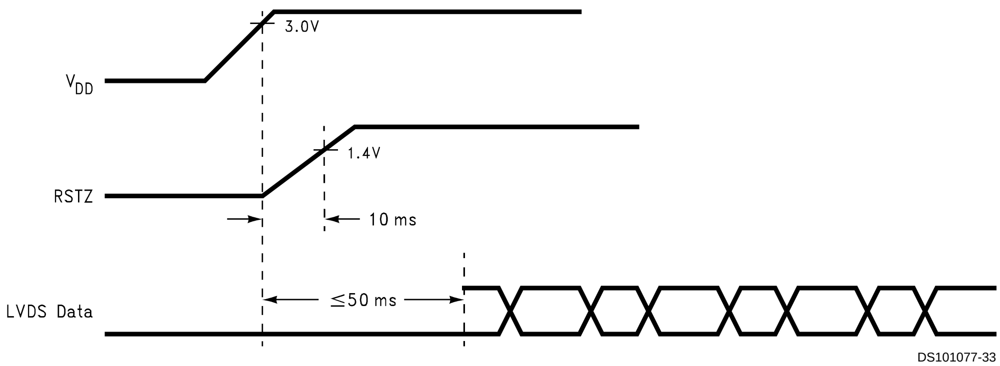



**FIGURE 6. FPD87310 Power Up Sequence**

## AC Electrical Characteristics (Continued)

**RSDS** (Reduced Swing Differential Signalling) Output Timing, these parameters are Guaranteed by Design.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SPD1 | SP Rising from RSCK Rising | $C_L$ = 15 pF | 0 | | 3.0 | ns |
| SPD2 | SP Falling from RSCK Rising | $C_L$ = 15 pF | 0 | | 3.0 | ns |
| GPD1 | GPO[9:0] Rising from RSCK Rising | $C_L$ = 15 pF | 0 | | 14 | ns |
| GPD2 | GPO[9:0] Falling from RSCK Rising | $C_L$ = 15 pF | 0 | | 14 | ns |
| RCHP | RSDS Clock (RSCK) High Period | $R_T$ = 100Ω, $C_T$ = 5 pF<br>$I_{PI}$ = 100 µA,<br>f=65MHz | 7.0 | | | ns |
| RCLP | RSDS Clock (RSCK) Low Period | $R_T$ = 100Ω, $C_T$ = 5 pF<br>$I_{PI}$ = 100 µA,<br>f=65MHz | 7.0 | | | ns |
| RSTU | RSR,G,B Setup to Falling or Rising Edge of RSCK,<br>Register Output Format Control = 0010 | $R_T$ = 100Ω, $C_T$ = 5 pF<br>$I_{PI}$ = 100 µA,<br>f=65MHz, | 3.8 | | | ns |
| RHLD | RSR,G,B Hold from Falling or Rising Edge of RSCK,<br>Register Output Format Control = 0010 | $R_T$ = 100Ω, $C_T$ = 5 pF<br>$I_{PI}$ = 100 µA,<br>f=65MHz | 0.2 | | | ns |

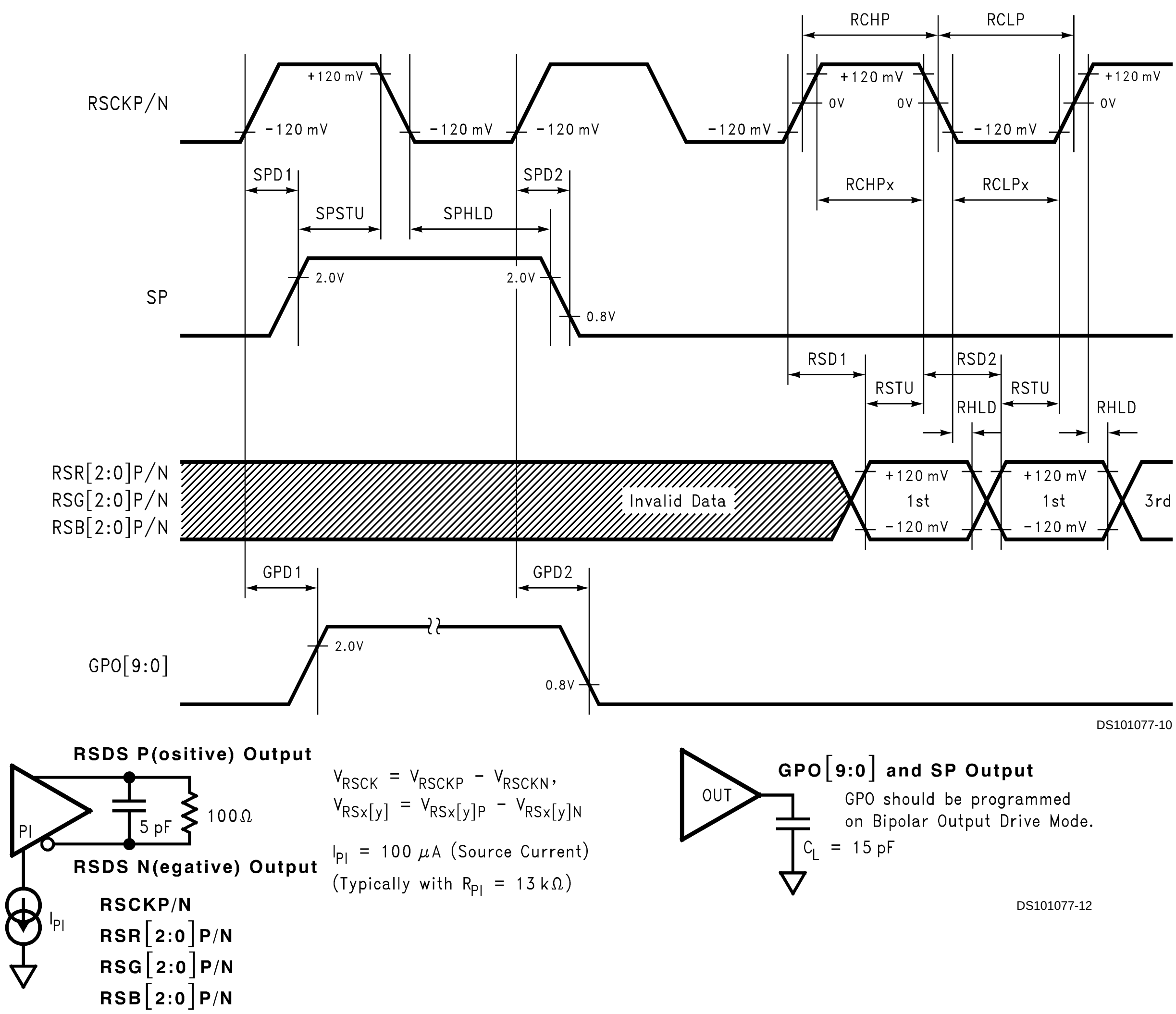
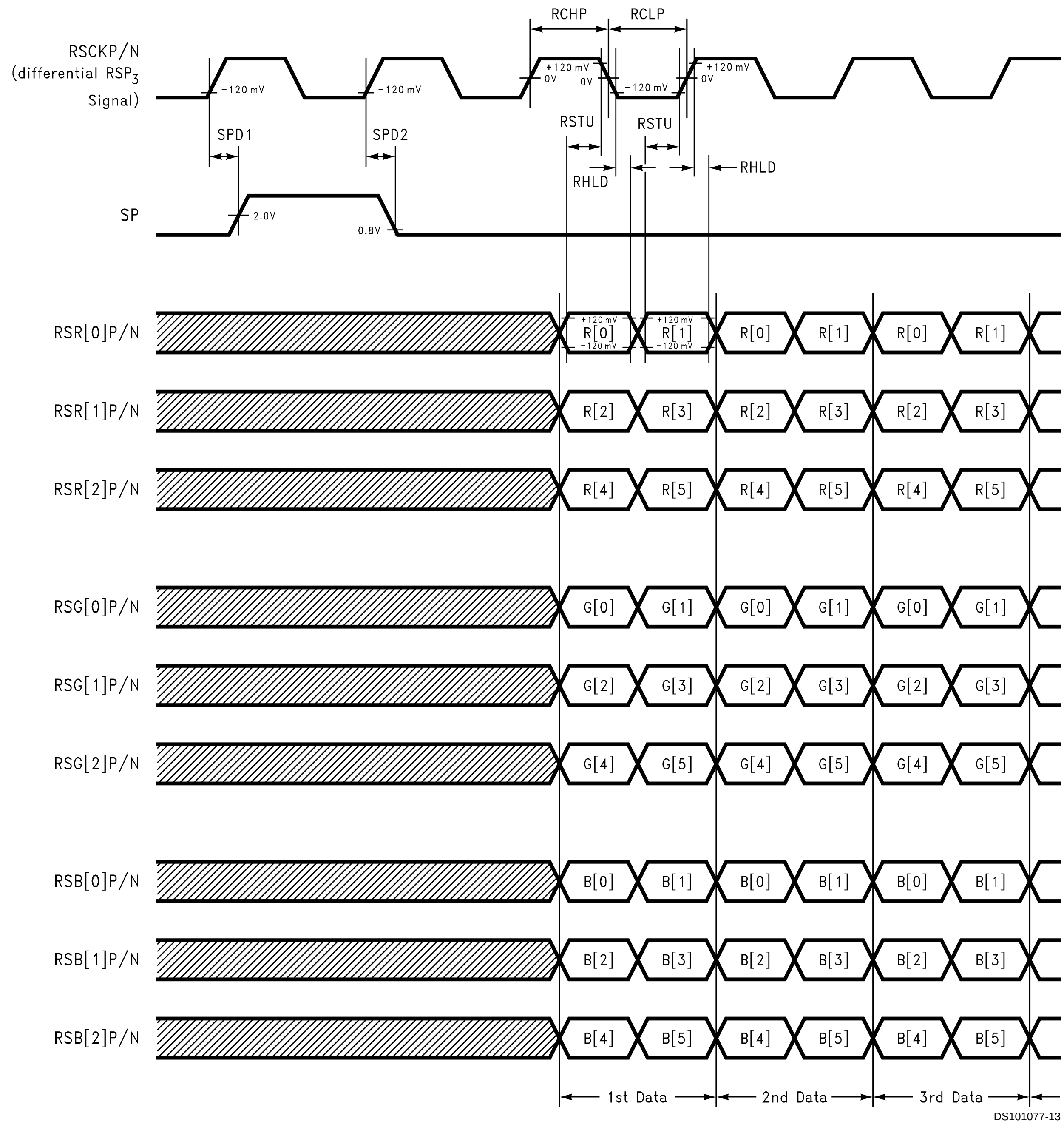



**FIGURE 7. FPD87310 RSDS Output Timing Diagram**

## AC Electrical Characteristics (Continued)




**Note:** RSCKP/N, RSR[2:0]P/N, RSG[2:0]P/N and RSB[2:0]P/N are differential outputs, SP is single ended output.

**FIGURE 8. FPD87310 RSDS Output Data Mapping**

## AC Electrical Characteristics (Continued)

**EEPROM INTERFACE TIMING**
This table is provided for reference only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{SC}$ | EE_SC Clock Frequency | | | 100 | | kHz |
| SC:LOW | Clock Low Period | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 4.7 | | | µs |
| SC:HIGH | Clock High Period | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 4.0 | | | µs |
| SCD:TR | EE_SC and EE_SD Rise Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | | | 1.0 | µs |
| SCD:TF | EE_SC and EE_SD Fall Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | | | 0.3 | µs |
| HD:STA | Start Condition Hold Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 4.0 | | | µs |
| HD:STO | Stop Condition Hold Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 0.6 | | | µs |
| $DL:DAT_H$ | Clock Falling Edge to Data High | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | | | 400 | ns |
| $DL:DAT_L$ | Clock Falling Edge to Data Low | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | | | 400 | ns |
| SU:DAT | Data Latch Setup Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 250 | | | ns |
| HD:DAT | Data Latch Hold Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 5 | | | µs |
| BUF | Bus Free Time | $R_P$ = 4.7 kΩ, $C_L$ = 50 pF | 4.7 | | | µs |

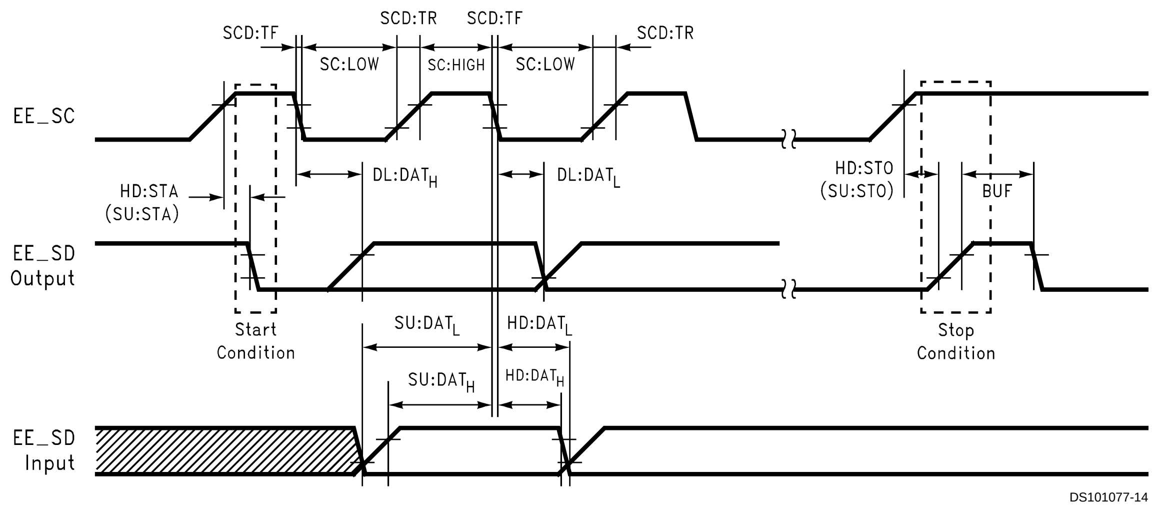



**FIGURE 9. EEPROM Interface Bus Timing**

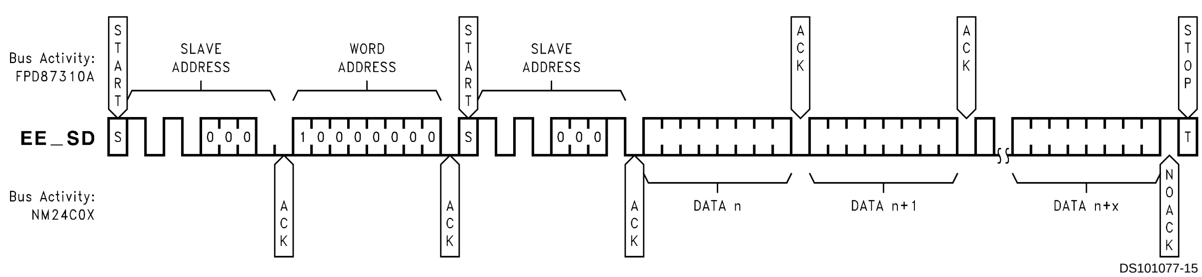
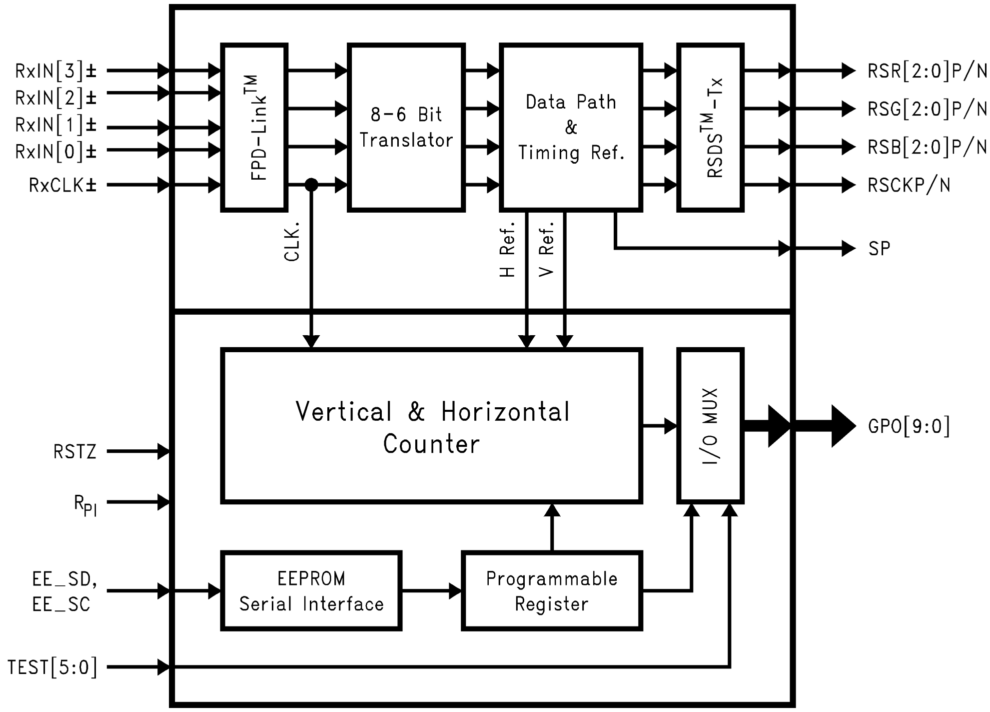



**FIGURE 10. EEPROM Sequential Read**

## Block Diagram

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## Functional Description

### FPD-Link RECEIVER

The LVDS based FPD-Link Receiver inputs video data and control timing. 4-LVDS channels plus clock provide 24 bits color. 3-LVDS channels can be used for 18 bits color. The video data is regenerated to a parallel data stream and routed to the 8-6 bit translator.

The GPOs (General Purpose Outputs) continue outputting the programmed control sequence at a reduced frame rate. RSTZ initialized the chip with the default register values.

### SPREAD SPECTRUM SUPPORT

The FPD-Link receiver supports graphics controllers with Spread Spectrum interfaces for reducing EMI. The Spread Spectrum method supported is Center Spread. A maximum of 2% Center Spread is supported at a frequency modulation of 200kHz maximum.

### 8–6 BIT TRANSLATOR

8-bit data is reduced to a 6-bit data path via a time multiplexed dithering technique or simple truncation of the LSBs. This function is enabled via the Input Control Register bits [4,3]. Care should be taken in providing the correct input color mapping (see *Figure 4*)

### DATAPATH BLOCK AND RSDS TRANSMITTER

6-bit video data (RGB) is input to the Datapath Block at a 65 MHz rate.

The data is delayed to align the Column Driver Start Pulse (SP) with the Column Driver data. The data (RSR[2:0]P/N, RSG[2:0]P/N, RSB[2:0]P/N) is output at a 130 MHz rate on 9 differential output channels (9 pairs of outputs).

The clock is output on the RSCKP/N differential pair.

The RSDS Column Drivers latch data on both positive and negative edges of the clock.

### VERTICAL AND HORIZONTAL COUNTER

The counter block provides control to the Column Drivers, Row Drivers, and power supply as GPOs (General Purpose Outputs). Several video input formats are supported; Video timing which is fixed vertically, and horizontally (ENAB is ignored); Video timing which is fixed vertically, but uses ENAB for horizontal positioning; ENAB Only Mode which uses ENAB to position both vertically and horizontally. The FIX_VERT and FIX_HORIZ along with internal ENAB detection circuitry; control the operational mode. The fixed vertical and horizontal position points are programmable.

### TIMING CONTROL

The Timing Control function generates control to Column Drivers, Row Drivers, and power supply. The programmable GPOs (General Purpose Outputs) provide for CD latch pulse, REV, and Row Driver control generation.

The General Purpose Outputs allow the user to generate control anywhere within the frame data. Standard Row Driver interface or Custom Row Driver interfaces can be implemented with the 10 GPOs (General Purpose Outputs).

Note that GPO[9] must be used for output blanking control.

### THE GENERAL PURPOSE OUTPUTS

Five registers provide the timing definition for each GPO.

- The Horizontal Start Register defines the output pixel number for which the GPO output goes active.
- The Horizontal Duration Register determines how many clocks the output will remain active during the line.
- The Vertical Start Register defines at what line# the output become active.
- The Vertical Duration Register defines how many lines the output remains active.

## Functional Description (Continued)

- Each output has a Control Register (bit [0]) which defines the GPO polarity (active high or low). Another bit in the Control Register (bit [1] enables the “toggle” mode. This mode is useful in REV generation when alternating polarity is required from line to line. Frame to Frame polarity changes are made by programming an odd # in the vertical duration register when in “toggle” mode.

Two of the General Purpose Outputs have additional capabilities.

GPO[0] is capable of performing line inversion on the output data. Bits [4,3] of the Output Format Control Register provides control for this function.

GPO[9] controls output blanking and must be used for this purpose. If output blanking is not desired, this register must be programmed to always be active.

Black or White Data Generation (all “0” or “1” data) at the end of each frame is generated when Input Format Control Register bits [7,6] is set “10” or “11”. When those bits are set, Black or White data is output after line #768 if GPO[9] is active.

### SERIAL EEPROM INTERFACE

The Serial EEPROM Interface controls the FPD87310 initialization. If the first byte word read from the EEPROM is not “00”, the internal default values are used to initialize all programmable function of the FPD87310.

At power-up, the FPD87310 configures the internal programmable registers with data from the EEPROM. After the FPD87310 is initialized, the EEPROM can be accessed by the system in which display configuration and manufacturing information can be obtained. The EEPROM can be programmed “in system” providing quick evaluation of different display timing. External access to the EEPROM must be preceded by pin TEST[2] = “1” in order to interrupt the FPD87310 download. Continuous initialization with EEPROM is also selectable by pin TEST[2] = “0”.

The FPD87310 initialization data begins at EEPROM address $080_H$. The first 128 bytes ($00_H$–$07F_H$) are reserved for display identification data.

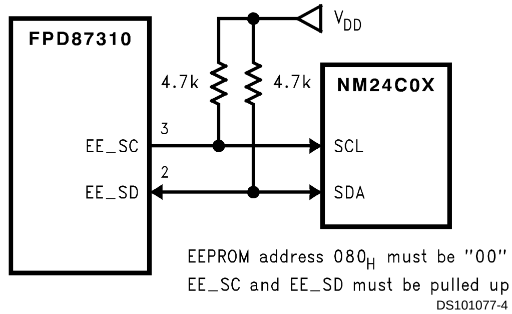



**FIGURE 11. EEPROM Connection**

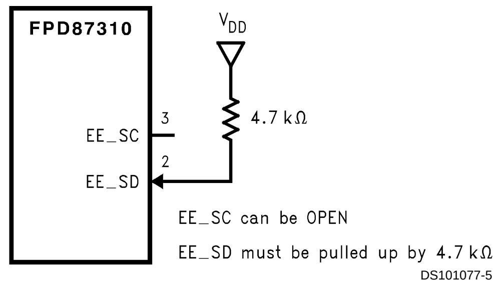



**FIGURE 12. Without EEPROM**

### RSDS OUTPUT VOLTAGE CONTROL

The RSDS output voltage swing is controlled through an external load resistor connected to the $R_{PI}$ pin. Typical value for the $R_{PI}$ is 13kΩ for most applications. However, this is dependent on overall LCD module design characteristics such as trace impedance, termination, etc. The RSDS output voltage is inversely related to the $R_{PI}$ value. Lower $R_{PI}$ values will increase the RSDS output voltage swing and consequently overall power consumption will also increase. See .*Figure 13*

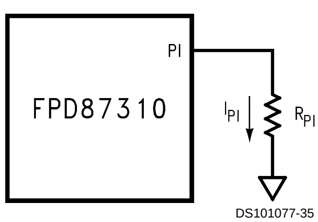



**FIGURE 13. $R_{PI}$ Connection Diagram**

## Programmable Registers

At power-up, data is read from an external EEPROM. If anything other than 00H is read back on the first EEPROM access (indicating EEPROM not present), the internal default values are used.

Pull-Up must be used on EE_SD pin if external EEPROM is not used.

The following parameters are initialized at power up.

**TABLE 1. FPD87310 Programmable Register Definition**

| Control Registers | EEPROM Address | | The CONTROL REGISTER provide more setting information to the input and output interfaces. |
|---|---|---|---|
| Output Format Control (16 bits) | $082_H$, $081_H$ | [2:0] | Reserved |
| | | [3] | Output Data Inversion<br>“0” - Data inversion is Disabled<br>“1” - Data inversion is Enabled |
| | | [4] | Output Data Inversion/Polarity<br>“0” - Data Inversion when GPO[0] is “0”<br>“1” - Data inversion when GPO[0] is “1” |
| | | [7:5] | Reserved |
| | | [11:8] | RSDS output setup/hold time control |
| | | [13:12] | Unused Pixels<br>“00” - no unconnected pixels at beginning of first CD<br>“01” - 1 unconnected pixels at beginning of first CD<br>“10” - 2 unconnected pixels at beginning of first CD<br>“11” - 3 unconnected pixels at beginning of first CD |
| | | [15:14] | Reserved |
| Input Format Control (8 bits) | $085_H$ | [1:0] | Reserved |
| | | [2] | Reserved |
| | | [3] | Frame Rate Control (8 bits only)<br>“0” - Enable Frame Rate Control<br>“1” - Disable Frame Rate Control (Truncate LSBs) |
| | | [4] | 8/6 Bits Video<br>“0” - 6 Bits Video<br>“1” - 8 Bits Video |
| | | [5] | Reserved |
| | | [7:6] | Black or White data Generation<br>“00” - No data manipulation is performed<br>“10” - Data goes to “0” when GPO[9] is “0”<br>“11” - Data goes to “1” when GPO[9] is “0”<br>Black data “0” or White data “1” will be output on lines > 768.<br>GPO[9] must be programmed to > 768 lines for data to be output. |
| Horizontal Backporch (11 bits) | $087_H$, $086_H$ | | # of 65 MHz clocks after the falling edge of HYSYNC until start of video. |
| Vertical Backporch (11 bits) | $089_H$, $088_H$ | | # of HSYNC from VSYNC falling edge until start of video. |

## Programmable Registers (Continued)

**TABLE 1. FPD87310 Programmable Register Definition** (Continued)

| Control Registers | EEPROM Address | The CONTROL REGISTER provide more setting information to the input and output interfaces. |
|---|---|---|
| General Purpose Output GPO Registers (10 sets) | **See Table 2 EEPROM Memory Map**<br>GPO[0]:a=$08B_H$<br>GPO[1]:a=$094_H$<br>GPO[2]:a=$09D_H$<br>GPO[3]:a=$0A6_H$<br>GPO[4]:a=$0AF_H$<br>GPO[5]:a=$0B8_H$<br>GPO[6]:a=$0C1_H$<br>GPO[7]:a=$0CA_H$<br>GPO[8]:a=$0D3_H$<br>GPO[9]:a=$0DC_H$ | The GPO registers provide complete control over placement of control edges/strobes within the data frame.<br>The GPO timing registers (Vertical Start, Vertical Duration, Horizontal Start, and Horizontal Duration) define the control timing relative to the Internal line and pixel counters.<br>The line counter corresponds to the line being displayed. The pixel counter corresponds to the pixel output each line. The Control Register provides polarity selection and/or generation of a line to line frame to frame alternating signal (REV). Each General Purpose Output can be uniquely configured.<br>See the GPO programming examples for details.<br>- GPO[0]: provides for the data inverting function enabled by bit [3] of the Output Format Control Register.<br>- GPO[9]: provides programmable data and clock blanking. |
| Horizontal Start (11 bits) | (a+1), (a) | Internal count (pixel counter) at which GPO[x] goes active |
| Horizontal Duration (11 bits) | (a+3), (a+2) | # Pixel Clocks GPO[x] is active after Horizontal Start (if “0”, Horizontal component is always on) |
| Vertical Start (11 bits) | (a+5), (a+4) | Line# at which GPO[x] control generation begins |
| Vertical Duration (11 bits) | (a+7), (a+6) | # Lines GPO[x] control generation continues (if “0”, Vertical component is always on) |

## Programmable Registers (Continued)

**TABLE 1. FPD87310 Programmable Register Definition** (Continued)

| Control Registers | EEPROM Address | The CONTROL REGISTER provide more setting information to the input and output interfaces. | |
|---|---|---|---|
| Control Register (8 bits) | (a+8) | [0] | Output polarity - defines active high or active low output |
| | | | "0" - Normal output (active high) |
| | | | "1" - Inverted output (active low) |
| | | [1] | Toggle circuit Enable/Disable |
| | | | "0" - Toggle circuitry Disabled; Normal GPO output |
| | | | "1" - Toggle circuitry Enabled |
| | | [2] | Automatic Frame Size Detection |
| | | | GPO[1:0]. |
| | | | "0" - Normal Operation. |
| | | | "1" - Used with Toggle circuitry to create a "continuous" REV signal. The value of the Vertical Duration Register is overwritten. |
| | | | GPO[9:2]. |
| | | | "0" - Normal Operation. |
| | | | "1" - Early Start capability. |
| | | | The value in the Vertical Start Register is subtracted from the total number of lines/frames (auto-detected) to determine the vertical start position. |
| | | [4:3] | GPO[9:1] Combination Select. |
| | | | "00" - Select GPO[x] as programmed. (No combination function). |
| | | | "01" - Select GPO[x] "ANDed" with GPO[x-1]. |
| | | | "10" - Select GPO[x] "ORed" with GPO[x-1]. |
| | | | "11" - Select GPO[x] and GPO[x-1] on alternating frames. |
| | | [6:5] | Power-up sequence delay. |
| | | | "00" - Outputs active after 1st VSYNC after EEPROM download. |
| | | | "01" - Outputs active after 2nd VSYNC after EEPROM download. |
| | | | "10" - Outputs active after 3rd VSYNC after EEPROM download. |
| | | | "11" - Outputs actve after 4th VSYNC after EEPROM download. |
| | | [7] | Open Drain Output Control |
| | | | "0" - Outputs are Normal Operation. (sink/source drive current) |
| | | | "1" - Outputs are Open Drain. (sink current only) |

**TABLE 2. Internal Default Register Values and EEPROM Memory Map**

| No | Address | | Bits | Control Register | Register Name | Default Values | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | FF–EF | | | not used/not loaded | | Init#1 | | Init#2 | | Init#3 | |
| 56 | E4 | | 8 | GPO9 Control Register | reg_gpo9_cont | 30 | | 09 | | | |
| 55 | E3 | E2 | 11 | GPO9 Vertical Duration | reg_gpo9_lcount | 00 | 00 | 00 | 00 | | |
| 54 | E1 | E0 | 11 | GPO9 Vertical Start | reg_gpo9_lstart | 00 | 01 | 00 | 01 | | |
| 53 | DF | DE | 11 | GPO9 Horizontal Duration | reg_gpo9_pcount | 00 | 40 | 00 | 40 | | |
| 52 | DC | DD | 11 | GPO9 Horizontal Start | reg_gpo9_pstart | 03 | 86 | 03 | 86 | | |
| 51 | DB | | 8 | GPO8 Control Register | reg_gpo8_cont | 21 | | 09 | | | |
| 50 | DA | D9 | 11 | GPO8 Vertical Duration | reg_gpo8_lcount | 00 | 00 | 00 | 01 | | |
| 49 | D8 | D7 | 11 | GPO8 Vertical Start | reg_gpo8_lstart | 00 | 01 | 00 | 01 | | |
| 48 | D6 | D5 | 11 | GPO8 Horizontal Duration | reg_gpo8_pcount | 00 | 00 | 00 | 40 | | |
| 47 | D4 | D3 | 11 | GPO8 Horizontal Start | reg_gpo8_pstart | 00 | 01 | 01 | C2 | | |
| 46 | D2 | | 8 | GPO7 Control Register | reg_gpo7_cont | 00 | | 09 | | | |
| 45 | D1 | D0 | 11 | GPO7 Vertical Duration | reg_gpo7_lcount | 00 | 00 | 00 | 01 | | |
| 44 | CF | CE | 11 | GPO7 Vertical Start | reg_gpo7_lstart | 00 | 00 | 00 | 01 | | |
| 43 | CD | CC | 11 | GPO7 Horizontal Duration | reg_gpo7_pcount | 00 | 00 | 00 | 40 | | |

## Programmable Registers (Continued)

**TABLE 2. Internal Default Register Values and EEPROM Memory Map** (Continued)

| No | Address | | Bits | Control Register | Register Name | Default Values | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 42 | CB | CA | 11 | GPO7 Horizontal Start | reg_gpo7_pstart | 00 | 00 | 01 | 42 | | |
| 41 | C9 | | 8 | GPO6 Control Register | reg_gpo6_cont | 00 | | 09 | | | |
| 40 | C8 | C7 | 11 | GPO6 Vertical Duration | reg_gpo6_lcount | 00 | 00 | 00 | 01 | | |
| 39 | C6 | C5 | 11 | GPO6 Vertical Start | reg_gpo6_lstart | 00 | 00 | 00 | 01 | | |
| 38 | C4 | C3 | 11 | GPO6 Horizontal Duration | reg_gpo6_pcount | 00 | 00 | 00 | 40 | | |
| 37 | C2 | C1 | 11 | GPO6 Horizontal Start | reg_gpo6_pstart | 00 | 00 | 00 | C2 | | |
| 36 | C0 | | 8 | GPO5 Control Register | reg_gpo5_cont | 00 | | 01 | | | |
| 35 | BF | BE | 11 | GPO5 Vertical Duration | reg_gpo5_lcount | 00 | 00 | 00 | 01 | | |
| 34 | BD | BC | 11 | GPO5 Vertical Start | reg_gpo5_lstart | 00 | 00 | 00 | 01 | | |
| 33 | BB | BA | 11 | GPO5 Horizontal Duration | reg_gpo5_pcount | 00 | 00 | 00 | 40 | | |
| 32 | B9 | B8 | 11 | GPO5 Horizontal Start | reg_gpo5_pstart | 00 | 00 | 00 | 42 | | |
| 31 | B7 | | 8 | GPO4 Control Register | reg_gpo4_cont | 00 | | 00 | | | |
| 30 | B6 | B5 | 11 | GPO4 Vertical Duration | reg_gpo4_lcount | 00 | 00 | 00 | 00 | | |
| 29 | B4 | B3 | 11 | GPO4 Vertical Start | reg_gpo4_lstart | 00 | 01 | 00 | 01 | | |
| 28 | B2 | B1 | 11 | GPO4 Horizontal Duration | reg_gpo4_pcount | 00 | 50 | 00 | 50 | | |
| 27 | B0 | AF | 11 | GPO4 Horizontal Start | reg_gpo4_pstart | 03 | FA | 03 | FA | | |
| 26 | AE | | 8 | GPO3 Control Register | reg_gpo3_cont | 00 | | 20 | | | |
| 25 | AD | AC | 11 | GPO3 Vertical Duration | reg_gpo3_lcount | 00 | 00 | 00 | 00 | | |
| 24 | AB | AA | 11 | GPO3 Vertical Start | reg_gpo3_lstart | 00 | 01 | 00 | 01 | | |
| 23 | A9 | A8 | 11 | GPO3 Horizontal Duration | reg_gpo3_pcount | 02 | A0 | 00 | 00 | | |
| 22 | A7 | A6 | 11 | GPO3 Horizontal Start | reg_gpo3_pstart | 03 | 86 | 00 | 02 | | |
| 21 | A5 | | 8 | GPO2 Control Register | reg_gpo2_cont | 00 | | 01 | | | |
| 20 | A4 | A3 | 11 | GPO2 Vertical Duration | reg_gpo2_lcount | 00 | 01 | 00 | 01 | | |
| 19 | A2 | A1 | 11 | GPO2 Vertical Start | reg_gpo2_lstart | 00 | 01 | 00 | 01 | | |
| 18 | A0 | 9F | 11 | GPO2 Horizontal Duration | reg_gpo2_pcount | 05 | 46 | 00 | A0 | | |
| 17 | 9E | 9D | 11 | GPO2 Horizontal Start | reg_gpo2_pstart | 00 | 02 | 00 | 02 | | |
| 16 | 9C | | 8 | GPO1 Control Register | reg_gpo1_cont | 07 | | 07 | | | |
| 15 | 9B | 9A | 11 | GPO1 Vertical Duration | reg_gpo1_lcount | 00 | 01 | 00 | 01 | | |
| 14 | 99 | 98 | 11 | GPO1 Vertical Start | reg_gpo1_lstart | 00 | 01 | 00 | 01 | | |
| 13 | 97 | 96 | 11 | GPO1 Horizontal Duration | reg_gpo1_pcount | 04 | 00 | 04 | 00 | | |
| 12 | 95 | 94 | 11 | GPO1 Horizontal Start | reg_gpo1_pstart | 03 | FA | 03 | FA | | |
| 11 | 93 | | 8 | GPO0 Control Register | reg_gpo0_cont | 06 | | 06 | | | |
| 10 | 92 | 91 | 11 | GPO0 Vertical Duration | reg_gpo0_lcount | 00 | 01 | 00 | 01 | | |
| 9 | 90 | 8F | 11 | GPO0 Vertical Start | reg_gpo0_lstart | 00 | 02 | 00 | 02 | | |
| 8 | 8E | 8D | 11 | GPO0 Horizontal Duration | reg_gpo0_pcount | 04 | 00 | 04 | 00 | | |
| 7 | 8C | 8B | 11 | GPO0 Horizontal Start | reg_gpo0_pstart | 03 | FA | 03 | FA | | |
| 6 | 8A | | 8 | (Reserved) | | | | | | | |
| 5 | 89 | 88 | 11 | Vertical Backporch | reg_vbp | 00 | 23 | 00 | 23 | | |
| 4 | 87 | 86 | 11 | Horizontal Backporch | reg_hbp | 01 | 28 | 01 | 28 | | |
| 3 | 85 | | 8 | Input Format Control | reg_input_format | 00 | | 00 | | 00 | |
| 2 | 84 | | 8 | (Reserved) | | | | | | | |
| 1 | 83 | | 8 | (Reserved) | | | | | | | |
| 0 | 82 | 81 | 16 | Output Format Control | reg_output_format | 02 | 00 | 02 | 00 | 02 | 00 |
| | 80 | | 8 | (Programmed to “00H” for EEPROM auto detect) | | 00 | | 00 | | 00 | |
| | 7F–00 | | | DDC VESA DATA | | | | | | | |

# Timing Definition

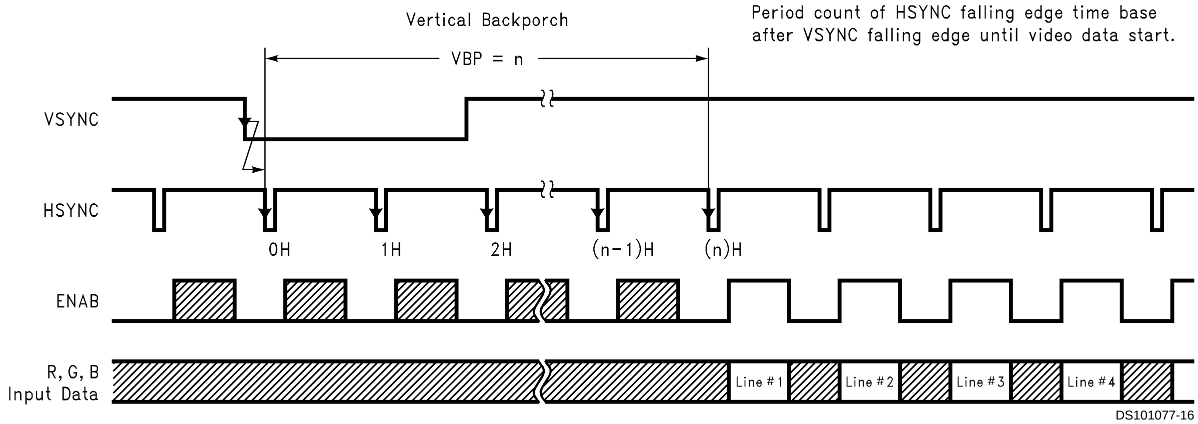
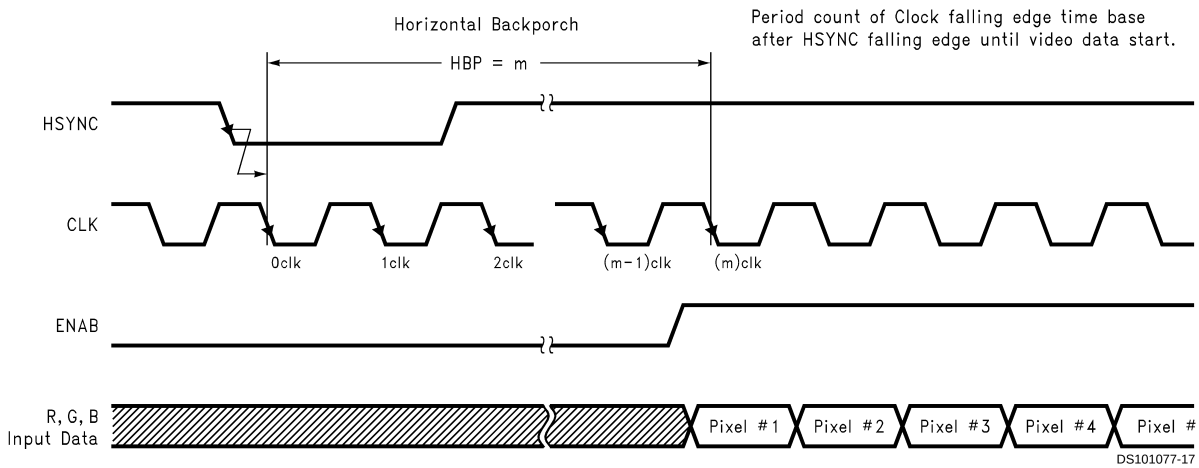



**FIGURE 14. Vertical Backporch Definition**




**Note:** Horizontal Position determined by ENAB if FIX_VERT = "0" and ENAB is active.

**FIGURE 15. Horizontal Backporch Definition**

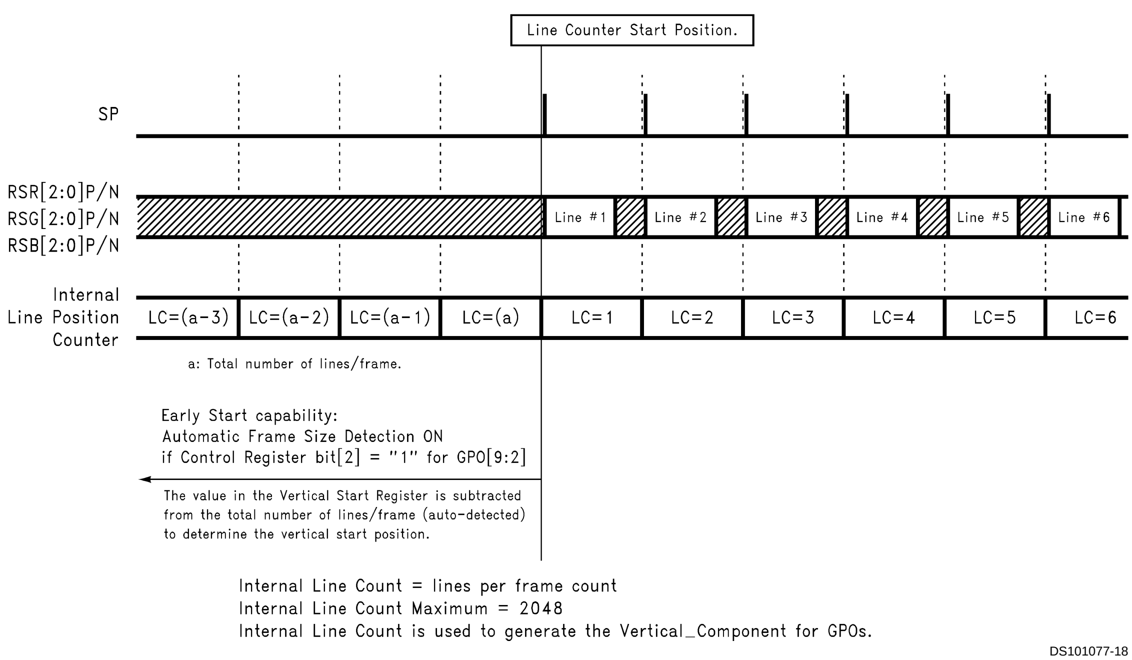



**FIGURE 16. Internal Line Position Counter**

## Timing Definition (Continued)

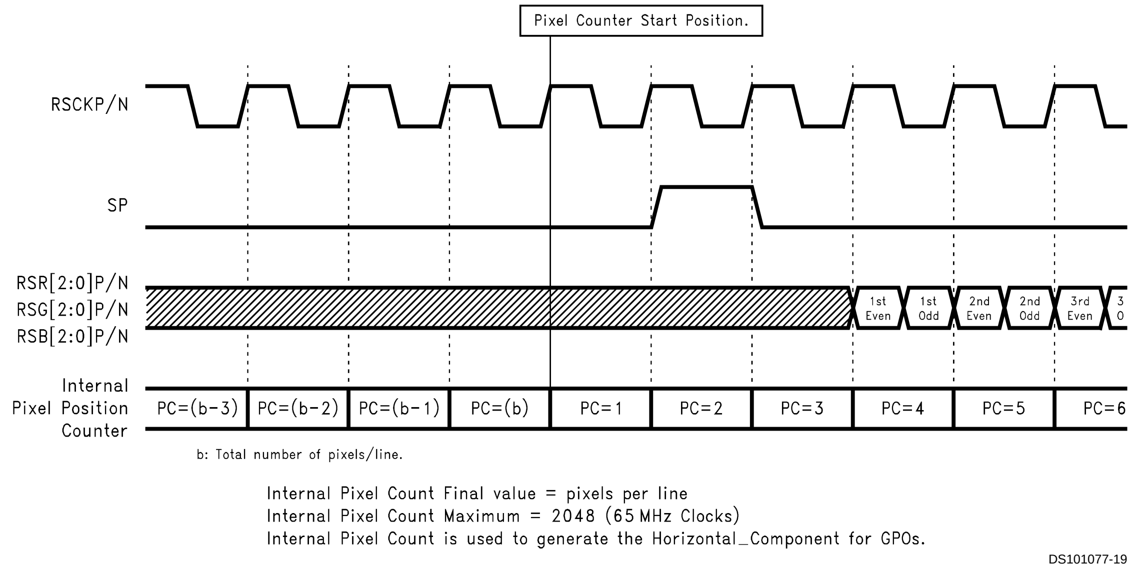
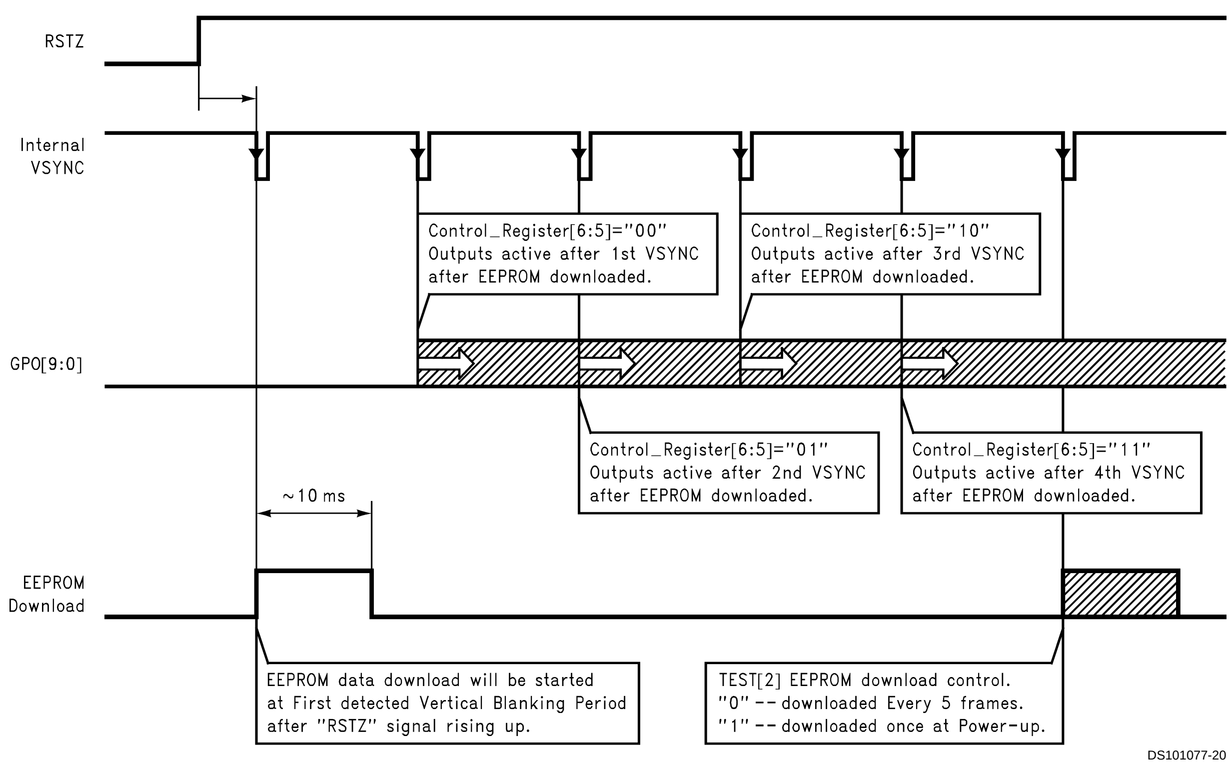


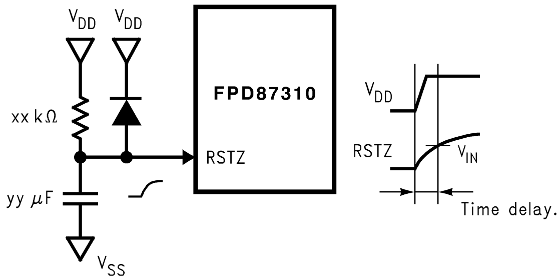

**FIGURE 17. Internal Pixel Position Counter**

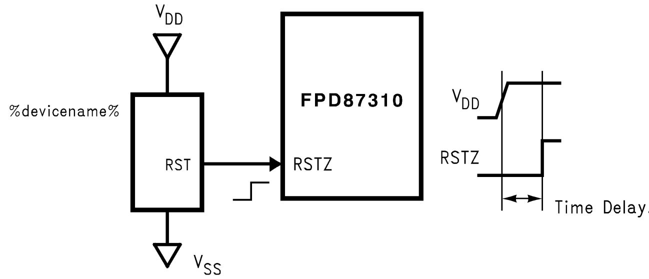



EEPROM download occurs at first detected Vertical Blanking Period after “RSTZ” signal rising up.
When in “ENAB Only Mode”, VSYNC timing is generated internally when ENAB remains “Low” (No Toggle) for more then 2 line times.
Outputs activation depends on GPO_Control_Register bits [6:5].
EEPROM download occur every 5 frames when TEST[2] = “0”.
When FPD87310 detected no EEPROM connection, the default value will be used for timing generation.
If set Early Start Capability, Outputs might be delayed activate position.

**FIGURE 18. Power-Up Sequence and EEPROM Downloading**

## Timing Definition (Continued)




If RSTZ is required long time constant delay or start slow ramping up supply ($V_{DD}$), NOT recommended to use this reset circuit.

**FIGURE 19. Suggested Power-Up Resetting Circuit**

## Timing Modes

The FPD87310 has Three Input Timing Operation Mode.

1. Fixed Vertical/Fixed Horizontal Mode. (FIX_VERT/FIX_HORIZ)
2. Fixed Vertical/ENAB Horizontal Mode. (FIX_VERT/ENAB_HORIZ/FIX_HORIZ)
3. ENAB Only Mode.

Input Timing Operation Mode can be programmed by input pin “FIX_VERT”, and “FIX_HORIZ”

| FIX_ VERT | FIX_ HORIZ | ENAB Tog-gling | Operation Mode |
|---|---|---|---|
| 0 | 0 | Yes | ENAB ONLY |
| 1 | 0 | Yes | FIX_VERT/FIX_HORIZ/ENAB |
| 1 | 1 | X | FIX_VERT/FIX_HORIZ |

**ENAB ONLY MODE**

FIX_VERT=”0”, FIX_HORIZ=”0”, ENAB is Toggling

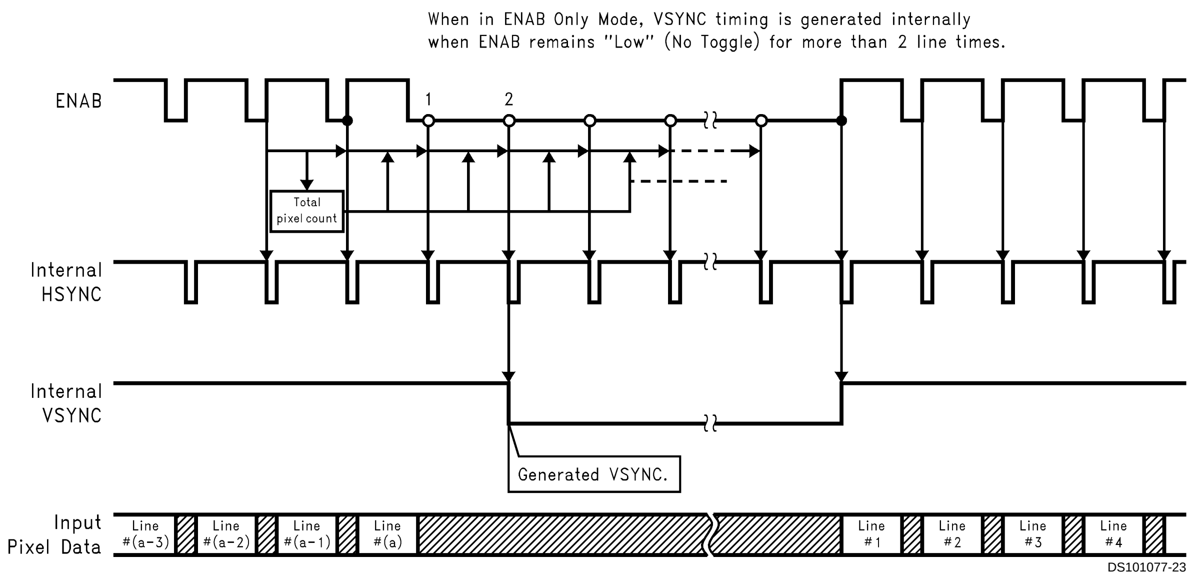
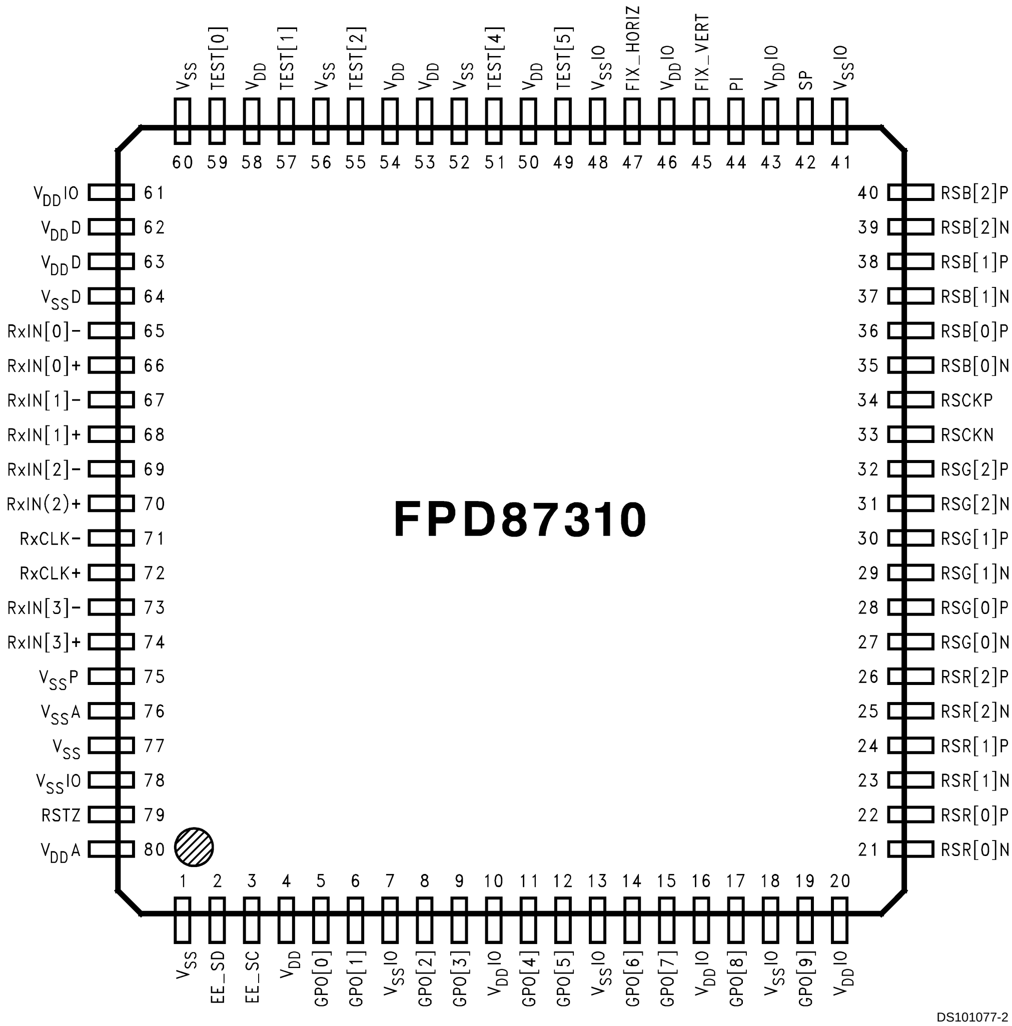



**FIGURE 20. ENAB ONLY MODE and Internally Generated Timing**

## Connection Diagram




**Thin Quad Flatpak (TQFP80)**

## Pin Description

**SYSTEM INTERFACE**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| RxIN[0]+/− | 2 | LVDSI | FPD-Link Data Differential Pair 0 Input |
| RxIN[1]+/− | 2 | LVDSI | FPD-Link Data Differential Pair 1 Input |
| RxIN[2]+/− | 2 | LVDSI | FPD-Link Data Differential Pair 2 Input |
| RxIN[3]+/− | 2 | LVDSI | FPD-Link Data Differential Pair 3 Input (Used in 8 Bits Video Application) |
| RxCLK+/− | 2 | LVDSI | FPD-Link Clock Differential Pair Input |
| RSTZ | 1 | STI | Reset Input, Active Low |

**COLUMN DRIVER INTERFACE**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| RSR[2:0]P/N | 6 | RSDSO | Red Reduced Swing Differential Outputs to Column Drivers |
| RSG[2:0]P/N | 6 | RSDSO | Green Reduced Swing Differential Outputs to Column Drivers |
| RSB[2:0]P/N | 6 | RSDSO | Blue Reduced Swing Differential Outputs to Column Drivers |
| RSCKP/N | 2 | RSDSO | Clock Reduced Swing Differential Outputs to Column Drivers |
| SP | 1 | TO | Start Pulse Output to Column Driver |

## Pin Description (Continued)

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| PI | 1 | I | Reference for Reduced Swing Differential Outputs |

**GENERAL PURPOSE OUTPUTS**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| GPO[9:0] | 10 | TO/OD | General Purpose Outputs (Programmable) |

**EEPROM INTERFACE**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| EE_SD | 1 | I/OD | EEPROM Serial Data |
| EE_SC | 1 | OD | EEPROM Clock |

**POWER SUPPLY**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| $V_{DD}A$ | 1 | P | FPD-Link PLL and Bandgap Power |
| $V_{DD}D$ | 2 | P | FPD-Link Receiver Power |
| $V_{DD}$ | 5 | P | Digital Power |
| $V_{DD}IO$ | 6 | P | Digital I/O Power |
| $V_{SS}P$ | 1 | G | FPD-Link PLL Ground |
| $V_{SS}A$ | 1 | G | FPD-Link Bandgap Ground |
| $V_{SS}D$ | 1 | G | FPD-Link Receiver Ground |
| $V_{SS}$ | 5 | G | Digital Ground |
| $V_{SS}IO$ | 6 | G | Digital I/O Ground |

**TEST/CONFIGURATION**

| Symbol | Pin Count | Type | Function |
|---|---|---|---|
| FIX_VERT | 1 | I | Selects VSYNC or ENAB for Vertical Timing<br>”0” = ENAB Vertical Timing<br>”1” = VSYNC Vertical Timing |
| FIX_HORIZ | 1 | I | Selects HSYNC or ENAB for Horizontal Timing<br>“0” = ENAB Horizontal Timing<br>“1” = HYNC Horizontal Timing |
| TEST[0,1,2,4,5] | 5 | I | Test/Configuration Pins<br>TEST[0]-Must be “0”<br>TEST[1]-Must be “0”<br>TEST[2] EEPROM Init Value Download Control<br>“0” - Downloaded every 5 frames<br>“1” - Downloaded once at Power-Up TEST[4]-Must be “0”<br>TEST[5]-Must be “0” |

**Pin Type Legend**

| | |
|---|---|
| I | TTL Input |
| STI | Schmitt Trigger TTL Input |
| I/TO | TTL Input/TRI-STATE® Output |
| TO | TRI-STATE Output |
| OD | Open Drain Output |
| LVDSI | Low Voltage Differential Signal Input |
| RSDSO | Reduced Swing Differential Sgnal Output |
| P | Power |
| G | Ground |

## Appendix A: GPO (General Purpose Output) Programming Examples

The GPO control generation is based on the internal line count and pixel count shown in *Figures 16, 17*. Two programmable registers (Vertical Start and Vertical Duration) control the vertical component of the control signal. This establishes at what line and for how many lines the control sig-

## Appendix A: GPO (General Purpose Output) Programming Examples (Continued)

nal will be active. Likewise, two programmable registers (Horizontal Start and Horizontal Duration) control the horizontal component of the control signal. The Horizontal register values determine at what pixel count the signal goes active and for how many pixel counts the signal stays active during each line. The Vertical Component enables the signal for however many lines programmed for and the Horizontal Component generates pulses within that vertical time period.

Generally the following types of signals are generated:

1. DC (either “1” or “0”)
2. A pulse every line.
3. A pulse once a frame (either in pixels or lines)
4. Pulsed during active video (pulses are blanked during vertical blanking period of frame).

*Table 3* describes the programming requirements for general types of pulses generated.

The GPO’s also have a “toggle mode”. This provides the capability to generate a “REVERSAL” signal used in most LCD applications. Bit[1] of the Central register is set to a “1” to enable toggle mode operation. The GPO is programmed so that a rising edge is produced when the control signal is required to toggle. This generally occurs once each line. Also, the # of edges generated per frame is programmed to be an odd #. This ensures that the control signal will alternate polarity from frame to frame.

Examples of GPO programming to produce specific control signals are included in the following pages.

**TABLE 3. GPO Pulse Generation**

| Type | Vertical Start | Vertical Duration | Horizontal Start | Horizontal Duration | GPO Output |
|---|---|---|---|---|---|
| 1 | =0 | =0 | =0 | =0 | Stuck 0 (When Output Polarity = “0”)<br>Stuck 1 (When Output Polarity = “1”)<br>Polarity control is in GPO Control Register bit [0] |
| 2 | =0 | =0 | #C | #D | Pulse is generated every line beginning at #C<br>pixel clocks from start of output line<br>and lasting for #D pixel clocks. |
| 3 | #A | #B | #C | =0 | Pulse begins at line #A, pixel #C and continues to line #(A+B), pixel #C (multi-line pulse) |
| 4 | #A | #B | #C | #D | Pulse generation begins at line #A and continue for #B lines.<br>Each pulse begins at pixel #C and lasts for #D pixel counts |

**Note 5:** GPO[0]: provides for the data inverting function enabled by bit[3] of the Output Format Control Register.

GPO[9]: provides programmable output RGB data, Clock and SP blanking function enabled by bit[6] of the Input Format Control Register (RSR[2:0]P/N, RSG[2:0]P/N, RSB[2:0]P/N, RSCKP/N and SP).

# Appendix A: GPO (General Purpose Output) Programming Examples

(Continued)

**GPO Programming Example #4a:**

Generate a control signal which transitions high at end of each line, has a pulse width of 0.5 µs, and remains low during the vertical blanking period.

This control signal is used for latch pulse to the Column Drivers.

Based on 65 MHz XGA video, 1024 pixel/line, 768 lines/frame.

Horizontal time (clocks/line) = 1300 dot clocks

Vertical period (lines/frame) = 850 lines

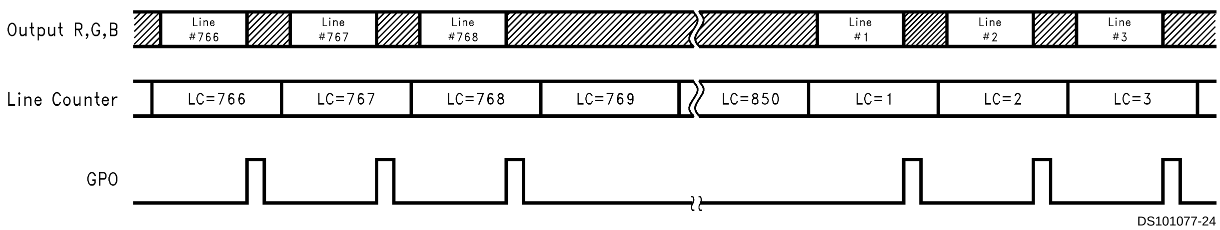



**FIGURE 21. Example #4a: GPO Vertical Scope View**

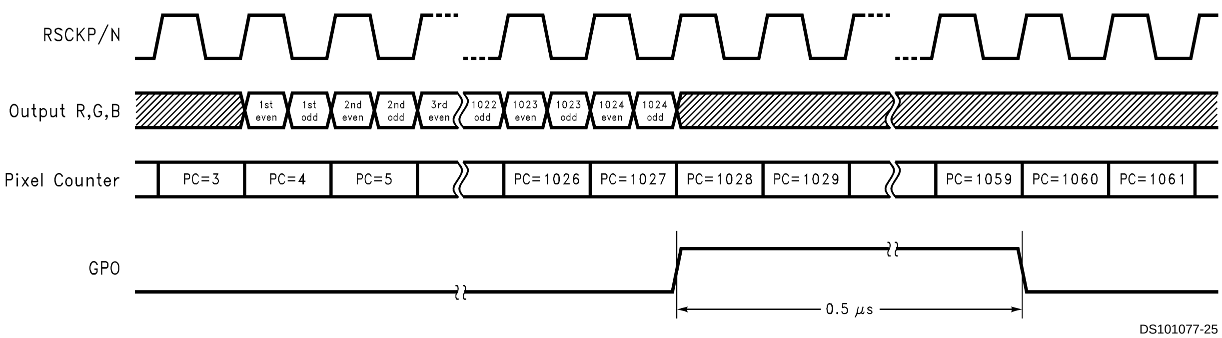



**FIGURE 22. Example #4a: GPO Horizontal Scope View**

Vertical control is active beginning at line #1 and remains active for line #768.

**GPO Vertical Start Register = 1** ($0001_H$)

**GPO Vertical Duration Register = 768** ($0300_H$)

Positive pulse goes high each line at 1024 output clocks after last pixel are outputted on R, G, B.

Pulse remains high for 32 output clocks (0.5 µs/15.38 ns = 32.5).

**Note:** 4 pixel counts are added to the output data start # because the GPO pixel count begins 4 clocks prior to the output data. Shown as *Figure 17* "Internal Pixel Position Counter".

**GPO Horizontal Start Register = 1028** ($0404_H$)

**GPO Horizontal Duration Register = 32** ($0020_H$)

The controlled pulses are positive (bit[0] = "0") and the toggle circuitry is disabled (bit[1] = "0").

**GPO Control Register = 0** ($00_h$) ($00000000_B$)

## Appendix A: GPO (General Purpose Output) Programming Examples (Continued)

**GPO Programming Example #4b:**

Generate a control signal which transitions low 20 output clocks after the beginning of each output line, has a pulse-width (low) of 12 µs, and goes high during horizontal blanking.

This control signal is used as an output enable for the Row Drivers.

Based on 65 MHz XGA video, 1024 pixel/line,

768 lines/frame.

Horizontal time (clocks/line) = 1300 dot clocks.

Vertical period (lines/frame) = 850 lines.

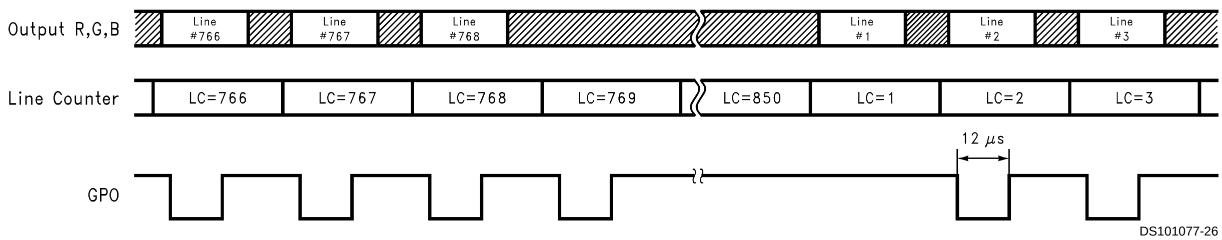



**FIGURE 23. Example #4b: GPO Vertical Scope View**

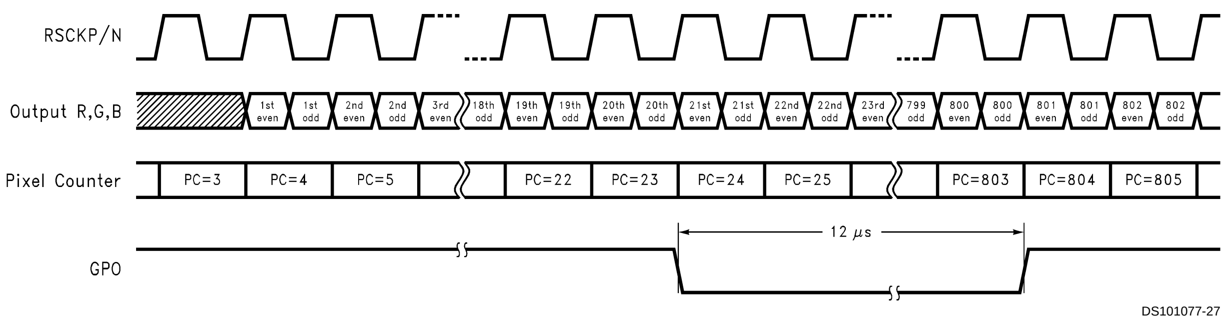



**FIGURE 24. Example #4b: GPO Horizontal Scope View**

Vertical control is active beginning at line #2 and remains active for line #768.

**GPO Vertical Start Register = 2** ($0002_H$)

**GPO Vertical Duration Register = 768** ($0300_H$)

Negative pulse goes low each line at 20 output clocks after first pixel data are outputted on R, G, B. Pulse remains low for 780 output clocks (12 µs/15.38 ns = 780).

**Note:** 4 pixel counts are added to the output data start # because the GPO pixel count begins 4 clocks prior to output data. (Shown as "*Figure 17* Internal Pixel Position Counter".

**GPO Horizontal Start Register = 24** ($0018_H$)

**GPO Horizontal Duration Register = 780** ($030c_H$)

The controlled pulses are negative (bit[0] = "1") and the toggle circuitry is disabled (bit[1] = "0").

**GPO Control Register = 1** ($01_H$) ($00000001_B$)

## Appendix A: GPO (General Purpose Output) Programming Examples (Continued)

**GPO Programming Example #4c:**

Generate a control signal which toggles at 20 output clocks after end of each output line during horizontal blanking and alternates polarity each frame.

This control signal is used as the reversal signal.

Based on 65 MHz XGA video, 1024 pixel/line, 768 lines/frame.

Horizontal time (clocks/line) = 1300 dot clocks

Vertical period (lines/frame) = 850 lines

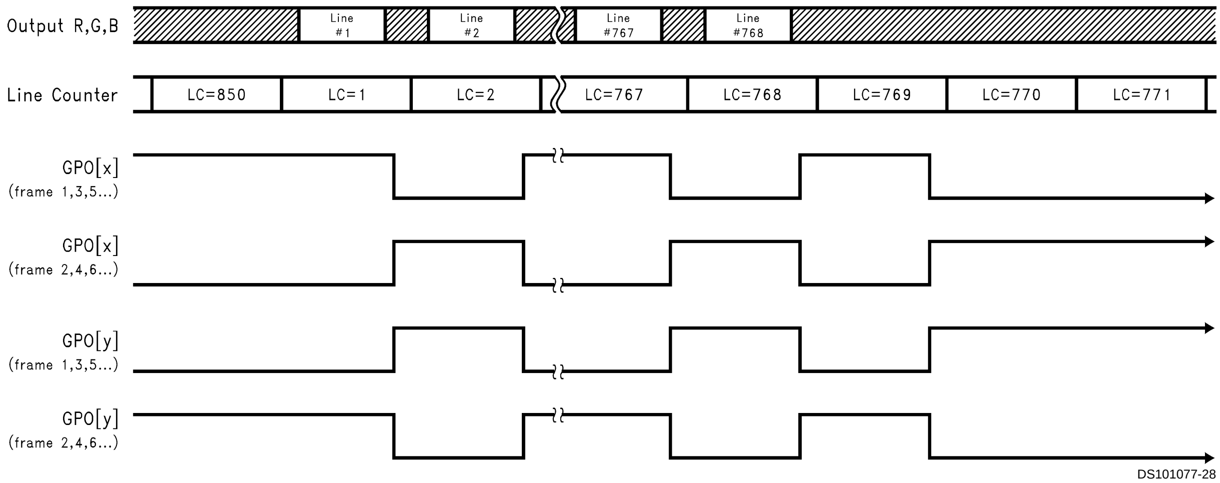



**FIGURE 25. Example #4c: GPO Vertical Scope View**

Control is active beginning at line #1 and remains active for line #769.

(Odd number programmed in Vertical Duration Register causes control signal to alternate polarity each frame)

**GPO Vertical Start Register = 1** ($0001_H$)

**GPO Vertical Duration Register = 769** ($0301_H$)

Positive going pulse causes output to toggle.

Edge occurs 20 output clocks after end of each line (1024 + 20 = 1044). Pulse duration is not critical since the output will be in toggle mode, but it cannot be “0”.

**Note:** 4 pixel counts are added to the output data start # because the GPO pixel count begins 4 clocks prior to the output data. Shown as “*Figure 17* Internal Pixel Position Counter.”

**GPO Horizontal Start Register = 1048** ($0418_H$) [1044+4=1048]

**GPO Horizontal Duration Register = 16** ($0010_H$)

The controlled pulses are positive (bit[0] = “0”) and the toggle circuitry is enabled (bit[1] = “1”).

**GPO Control Register = 2** ($02_H$) ($00000010_B$)

(For a second control signal of opposite polarity, (GPO[y]) program another GPO Control Register with same count values, signal are negative. (bit[0] = “1”).

**GPO Control Register = 3** ($03_H$) ($00000011_B$)

## Appendix A: GPO (General Purpose Output) Programming Examples (Continued)

### Special Function GPOs

FPD87310 has been provided two special purpose GPOs for manipulating the Output RGB Data, also the Clock and SP output can be controlled by GPO[9].

1. GPO[0] Output Data Inverting.

   Output _Format_Control_Register bits[4:3]

2. GPO[9] Output Data Blanking.

   Input_Format_Control_Register bits[7:6]

# Appendix A: GPO (General Purpose Output) Programming Examples

(Continued)

**TABLE 4. GPO[0] Inverting and GPO[9] Blanking Logical Function**

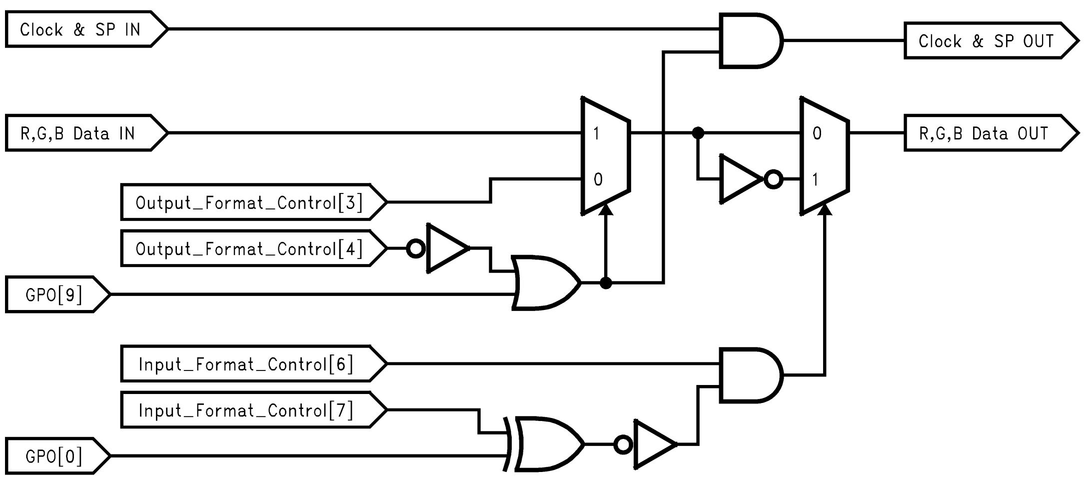
| **Output Format Control Register** | | **Output Format Control Register** | | **GPO[9]=0** | | **GPO[9]=1** | |
|---|---|---|---|---|---|---|---|
| bit[7] | bit[6] | bit[4] | bit[3] | GPO[0]=0 | GPO[0]=1 | GPO[0]=0 | GPO[0]=1 |
| 0 | x | x | 0 | - | - | - | - |
| | | 0 | 1 | inv(data) | - | inv(data) | - |
| | | 1 | 1 | - | inv(data) | - | inv(data) |
| 1 | 0 | x | 0 | 0 | 0 | - | - |
| | | 0 | 1 | 1 | 0 | inv(data) | - |
| | | 1 | 1 | 0 | 1 | - | inv(data) |
| 1 | 1 | x | 0 | 1 | 1 | - | - |
| | | 0 | 1 | 0 | 1 | inv(data) | - |
| | | 1 | 1 | 1 | 0 | - | inv(data) |

**Legends:**

| | |
|---|---|
| - | output data is unchanged |
| inv(data) | output data is inverted |
| 0 | output data is all “0” |
| 1 | output data is all “1” |

**TABLE 5. GPO[9] Blanking for Clock and SP**

| **Output Format Control Register** | | **GPO[9]=0** | **GPO[9]=1** |
|---|---|---|---|
| **bit[7]** | **bit[6]** | | |
| 0 | x | Output CLK & SP | Output CLK & SP |
| 1 | x | No Output (“0”) | Output CLK & SP |




DS101077-29

**FIGURE 26. GPO[0] Inverting and GPO[9] Blanking Method**

# Appendix A: GPO (General Purpose Output) Programming Examples
(Continued)

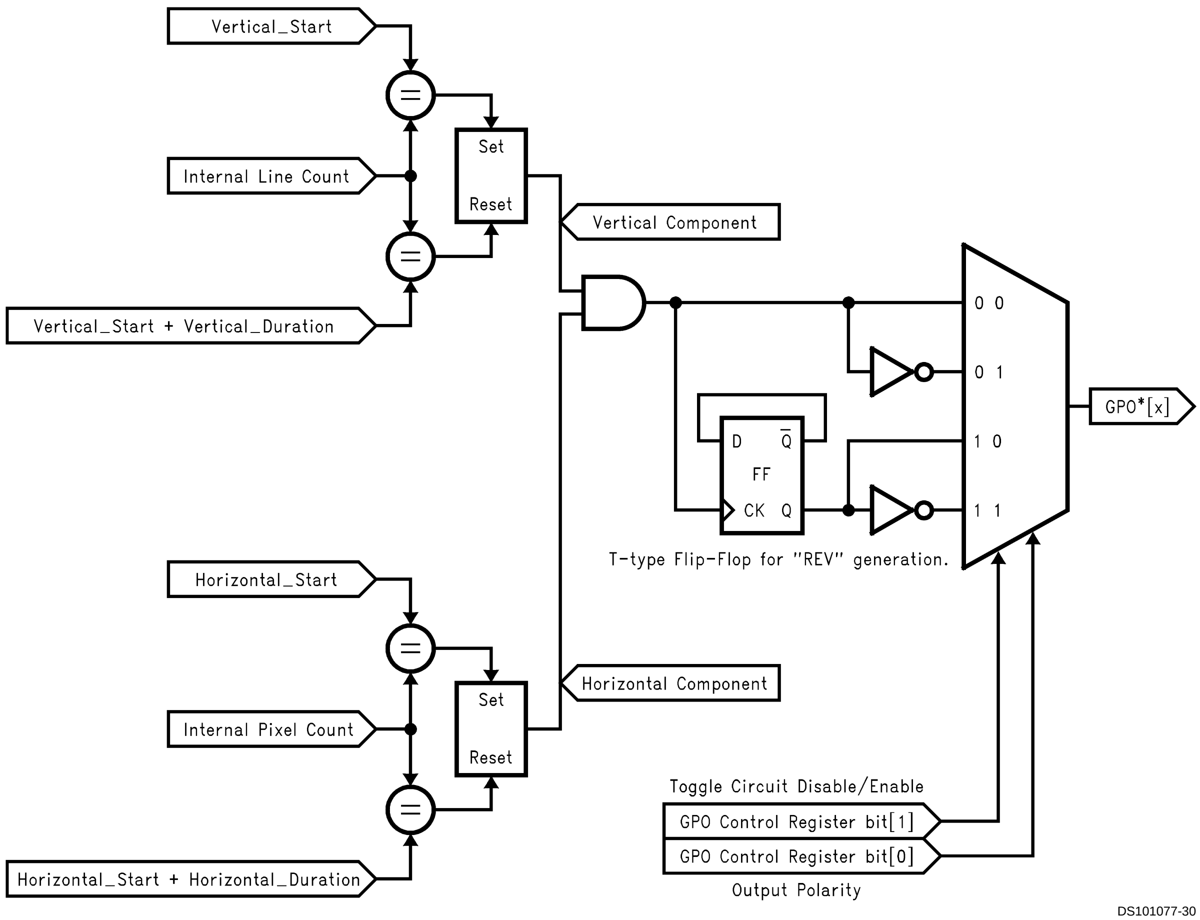



**FIGURE 27. GPO (General Purpose Output) Generation Method**

## Appendix A: GPO (General Purpose Output) Programming Examples
(Continued)

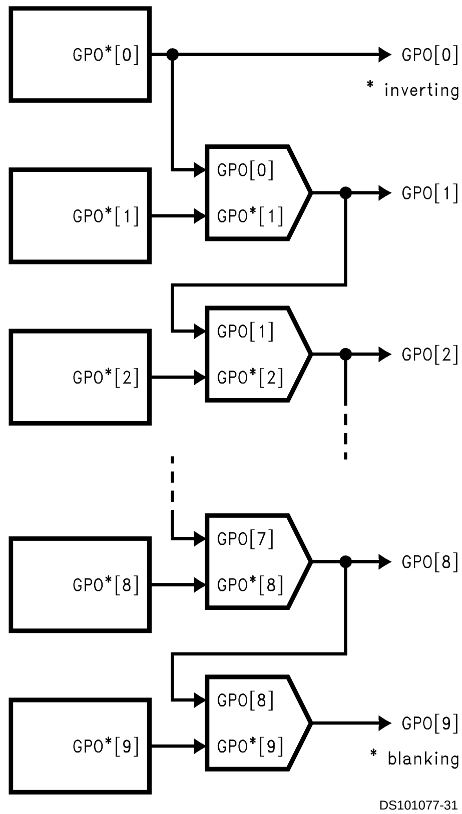



**FIGURE 28. GPO Nesting**

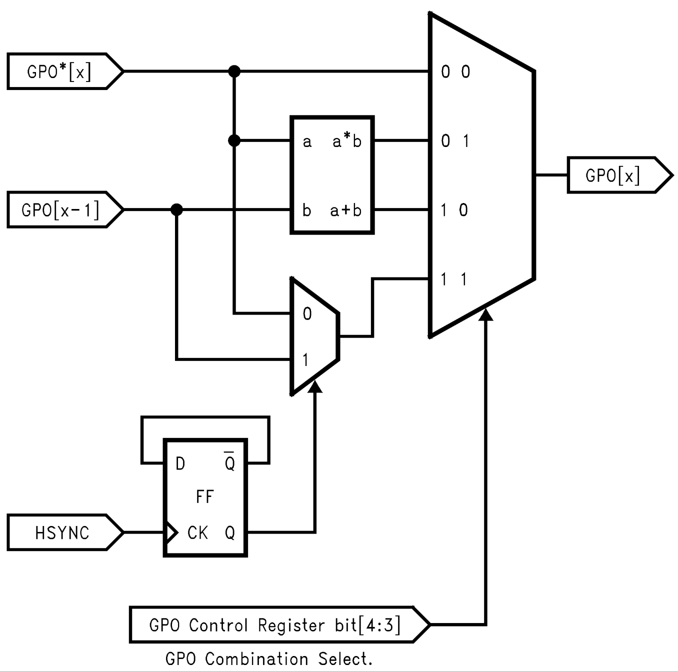
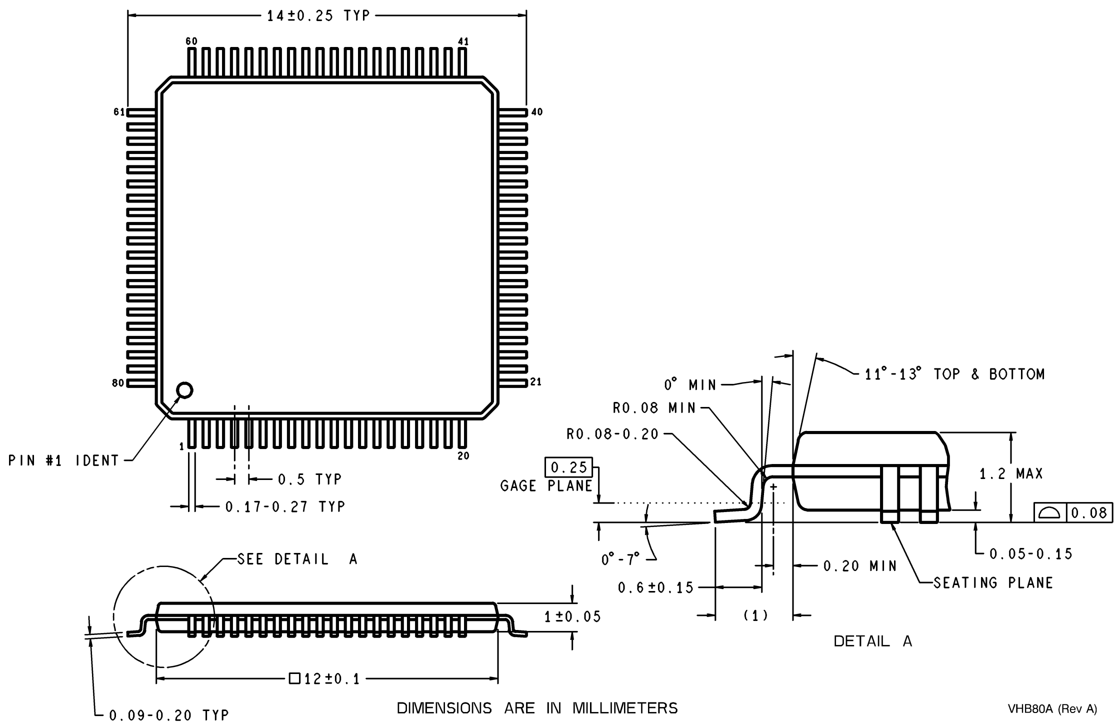



**FIGURE 29. GPO Combination Selector**

## Physical Dimensions inches (millimeters) unless otherwise noted




**Thin Plastic Quad Flatpak (TQFP)**
**Dimensions are in Millimeters**
**NS Package Number VHB80A**

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