FAIRCHILD SEMICONDUCTOR®

September 2012

FDZ2040L
Integrated Load Switch

Features

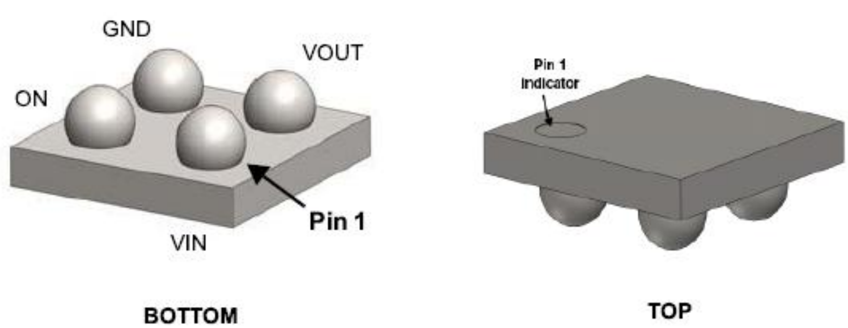
- Optimized for low-voltage core ICs in portable systems
- Very small package dimension: WL-CSP 0.8X0.8X0.5 mm^3
- Current = 1.2 A, V_{IN} max = 4 V
- Current = 2 A, V_{IN} max = 4 V (Pulsed)
- $R_{DS(ON)}$ = 80 mΩ at V_{ON} = 0 V, V_{IN} = 4 V
- $R_{DS(ON)}$ = 85 mΩ at V_{ON} = 0 V, V_{IN} = 3.6 V
- $R_{DS(ON)}$ = 90 mΩ at V_{ON} = 0 V, V_{IN} = 3 V
- RoHS Compliant

General Description

This device is particularly suited for compact power management in portable application where 1.6V to 4V input and 1.2A output current capability are needed. This load switch integrates a level shifting function that drives a P-Channel Power MOSFET in the very small 0.8X0.8X0.5 mm^3 WL-CSP package.

Applications

- Load switch
- Power management in portable applications



Ordering Information

Part Number	Device Marking	Ball Pitch	Operating Temperature Range	Switch	Eco Status	Package	Packing Method
FDZ2040L	ZL	0.4 mm	-25 to 75°C	80 mΩ, P-ch FET	RoHS	0.8x0.8x0.5 mm^3 WL-CSP	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram and Block Diagram

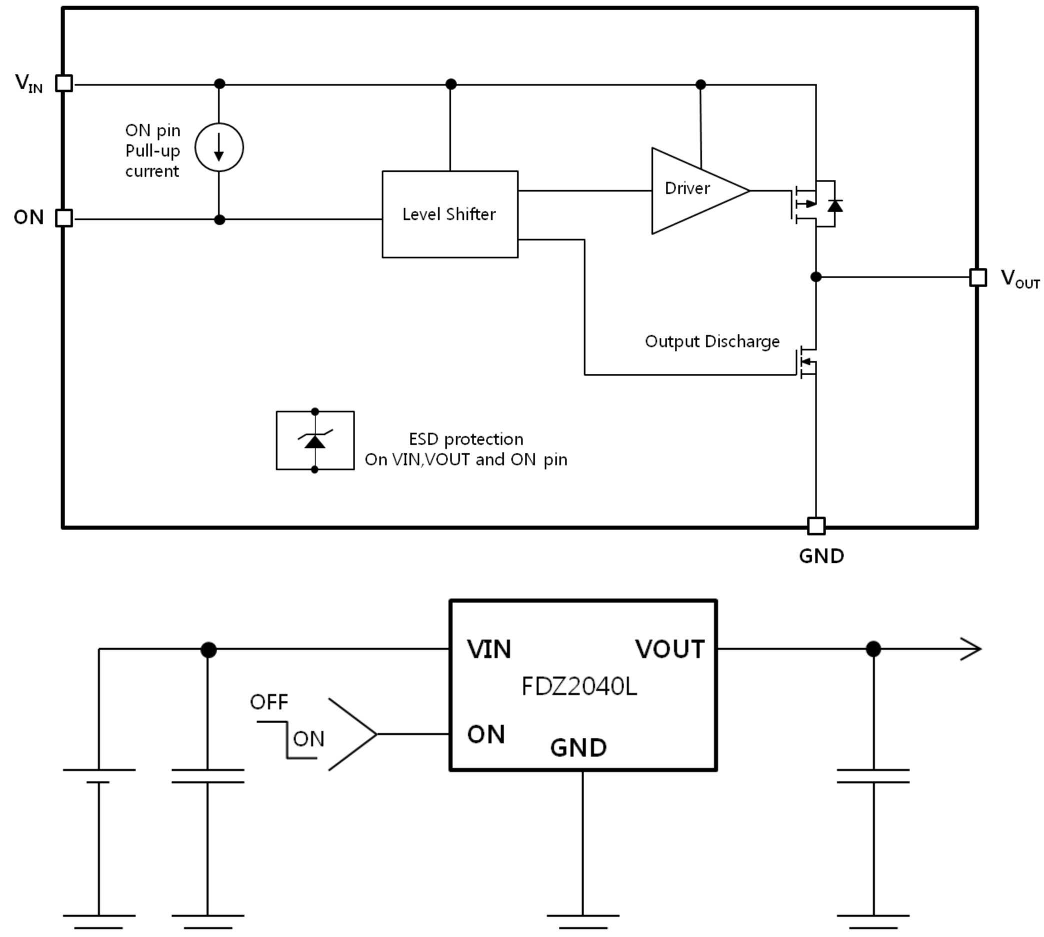


Figure 1. Block Diagram and Typical Application Pin Configuration

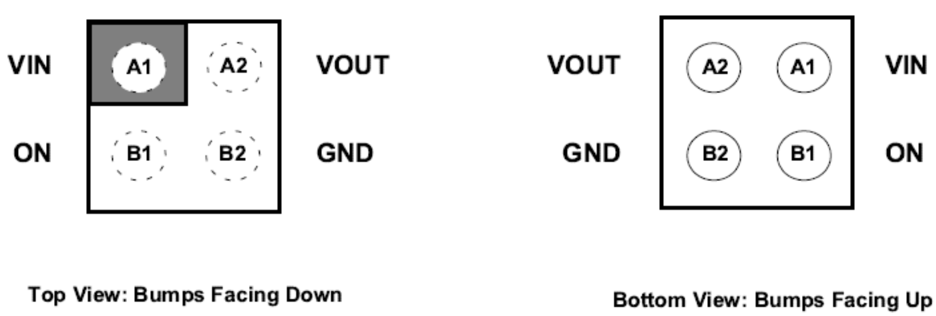


Figure 2. Pin Assignment

Pin Definitions

Pin #	Name	Description
A1	V_{IN}	Supply Input: Input to the load switch
A2	V_{OUT}	Switch Output: Output of the load switch
B1	ON	ON/OFF Control Input, active LOW
B2	GND	Ground

Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, ON to GND		-0.3	4.2	V
I_{OUT} – Load Current (Continuous)	(Note 1a)		1.2	A
I_{OUT} – Load Current (Pulsed)	(Note 2)		2	A
Power Dissipation @ T_A = 25℃	(Note 1a)		0.9	W
Operating Temperature Range		-40	105	℃
Storage Temperature		-65	150	℃
Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
	Charged Device Model, JESD22-C101	2		

Thermal Characteristics

Thermal Resistance, Junction to Ambient	(Note 1a)		117	℃/W

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
V_{IN}	1.6		4	V
Ambient Operating Temperature, T_A	-25		75	℃

Electrical Characteristics

T_J = 25 °C unless otherwise noted

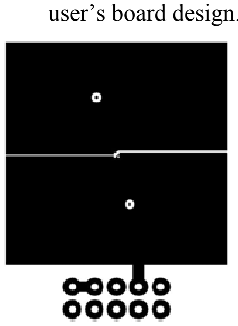
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IN}	Operation Voltage		1.6		4	V
V_{IL}	ON Input Logic Low Voltage	V_{IN} = 1.6V, Ramp down V_{ON} from 1V to 0V, V_{OUT} Low to High, T_J = -25 to 75 °C	0.35			V
		V_{IN} = 4V, Ramp down V_{ON} from 1V to 0V, V_{OUT} Low to High, T_J = -25 to 75 °C	0.35			V
V_{IH}	ON Input Logic High Voltage	V_{IN} = 1.6V, Ramp up V_{ON} from 0V to 1V, V_{OUT} High to Low, T_J = -25 to 75 °C			1.35	V
		V_{IN} = 4V, Ramp up V_{ON} from 0V to 1V, V_{OUT} High to Low, T_J = -25 to 75 °C			1.35	V
I_Q	Quiescent Current	V_{IN} = 3V, V_{ON} = 0.35V, I_{OUT} = 0A, T_J = -25 to 75 °C		1.55	2.5	µA
I_{Q_off}	Off Supply Current	V_{IN} = 3V, V_{ON} = 1.3V, I_{OUT} = 0A, T_J = -25 to 75 °C		2.4	6.5	µA
I_{SD_off}	Off Switch Current	V_{IN} = 3V, V_{ON} = 1.3V, V_{OUT} = 0V, T_J = -25 to 75 °C		0.1	3.5	µA
I_{Q_off} (VON float)	Off Supply Current with ON pin floating	V_{IN} = 3V, V_{ON} = floating, I_{OUT} = 0A,		1.6	2.3	µA
		V_{IN} = 3V, V_{ON} = floating, I_{OUT} = 0A, T_J = -25 to 75 °C		1.6	4	µA
$R_{DS(ON)}$	On Resistance	V_{IN} = 1.6V, V_{ON} = 0V, I_{OUT} = 300mA V_{IN} = 3V, V_{ON} = 0V, I_{OUT} = 300mA V_{IN} = 3.6V, V_{ON} = 0V, I_{OUT} = 300mA V_{IN} = 4V, V_{ON} = 0V, I_{OUT} = 300mA, T_J = -25 to 75 °C		68 50 48 47	120 90 85 80	mΩ
$C_{V\text{-}ON(INP)}$	ON Input Capacitance	T_J = -25 to 75 °C			5	pF
$I_{ON(PULL\text{-}UP)}$	ON Pull Up Current	V_{IN} = 3V, V_{ON} = 0V, T_J = -25 to 75 °C	0.3	0.76	1.2	µA

Switching Characteristics

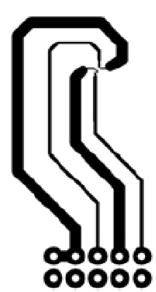
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
T_{on}	Turn on time (V_{ON} 50% to V_{OUT} 90%)	V_{IN}=3V, V_{ON} = 0V as logic low and 1.3V as logic high, C_{OUT} = 1nF, R_L = 30Ω, T_J = -25 to 75 °C		45	150	ns
T_{don}	Turn on delay time (V_{ON} 50% to V_{OUT} 10%)			35	100	ns
T_{rise}	Turn on rise time (V_{OUT} 10% to 90%)			10	50	ns
T_{off}	Turn off time (V_{ON} 50% to V_{OUT} 10%)			60	150	ns
T_{doff}	Turn off delay time (V_{ON} 50% to V_{OUT} 90%)			25	100	ns
T_{fall}	Turn off fall time (V_{OUT} 90% to 10%)			35	65	ns
$T_{don} - T_{doff}$	Turn on Turn off Delay Delta time				50	ns

Notes:

1. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta JA}$ is determined by the user's board design.



a. 117 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 277 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%.

Typical Performance Characteristics

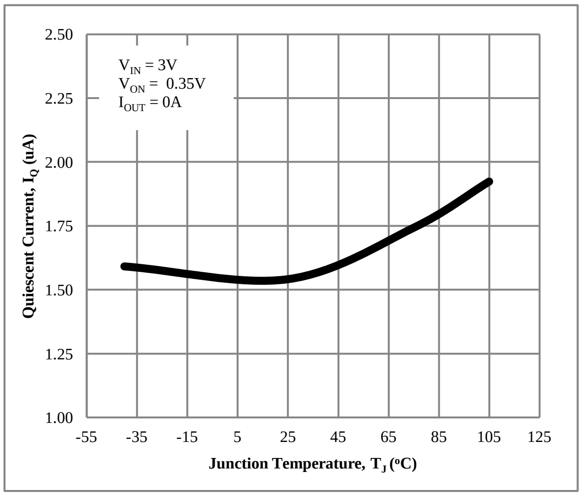


Figure 3. Quiescent Current vs. Temperature

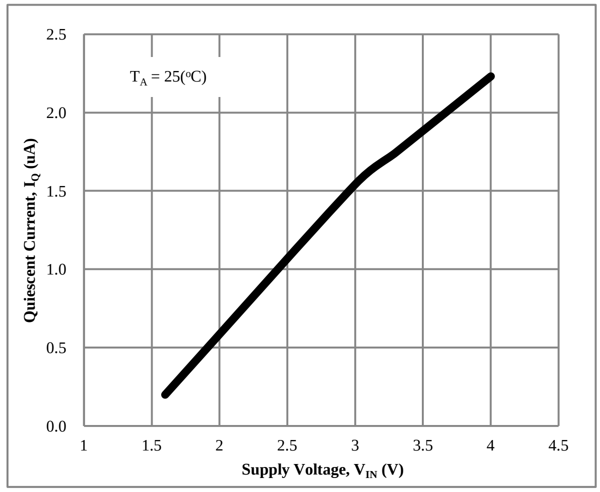


Figure 4. Quiescent Current vs. Supply Voltage

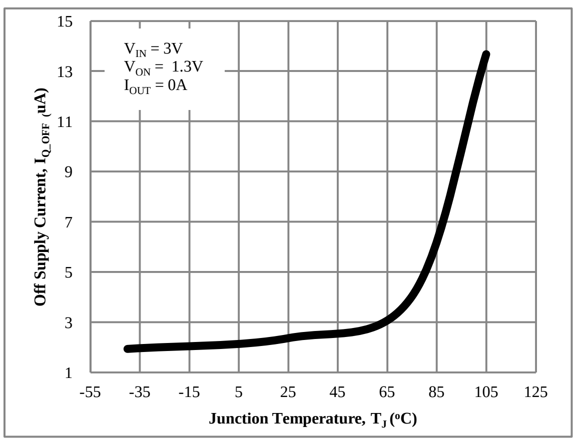


Figure 5. Off Supply Current vs. Temperature

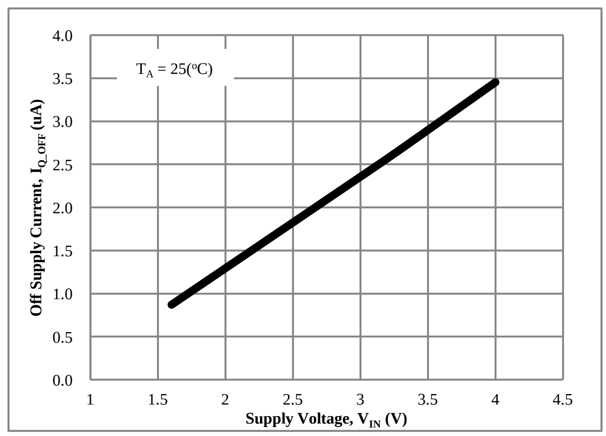


Figure 6. Off Supply Current vs. Supply Voltage

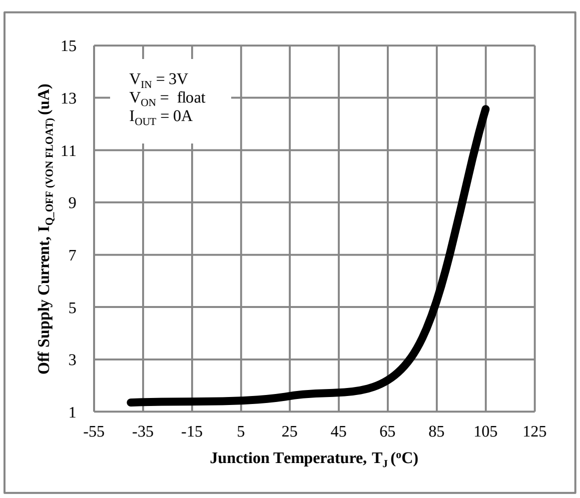


Figure 7. Off Supply Current(V_{ON} Float) vs. Temperature

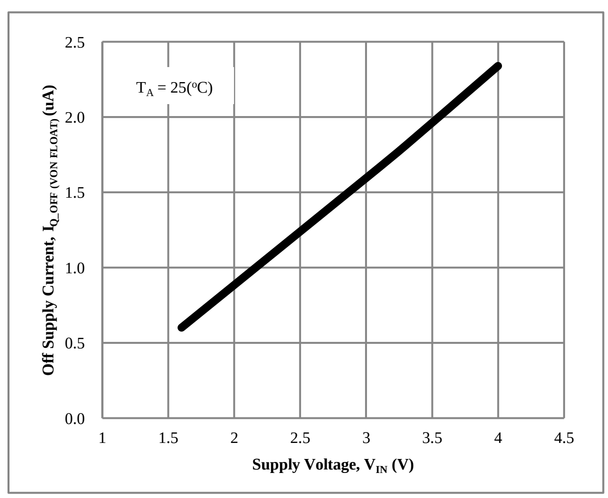


Figure 8. Off Supply Current(V_{ON} Float) vs. Supply Voltage

Typical Performance Characteristics (Continued)

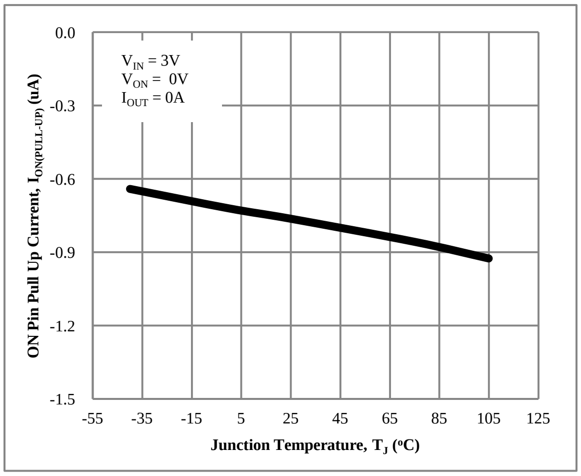


Figure 9. ON Pin Pull Up Current vs. Temperature

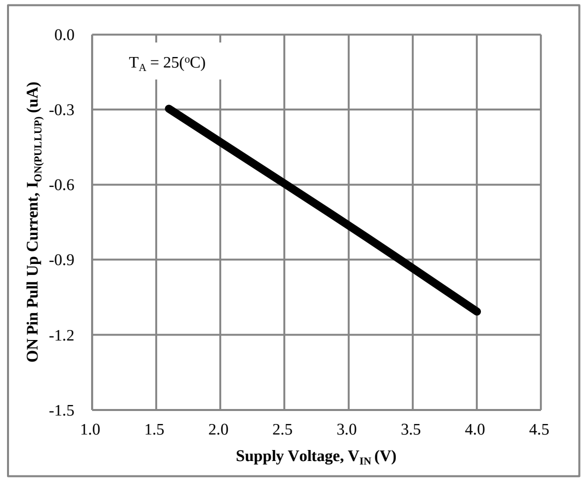


Figure 10. ON Pin Pull Up Current vs. Supply Voltage

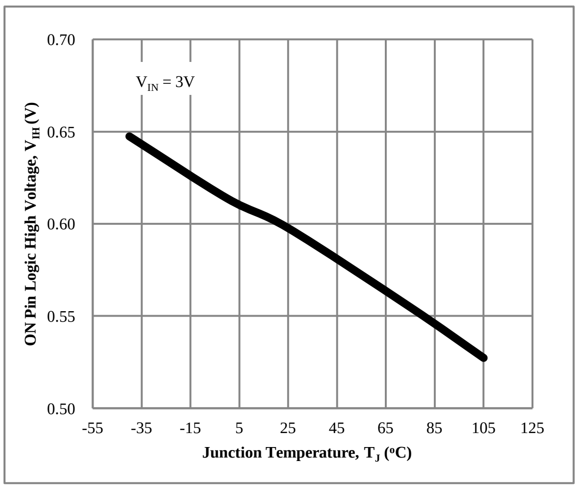


Figure 11. ON Pin Logic High Voltage vs. Temperature

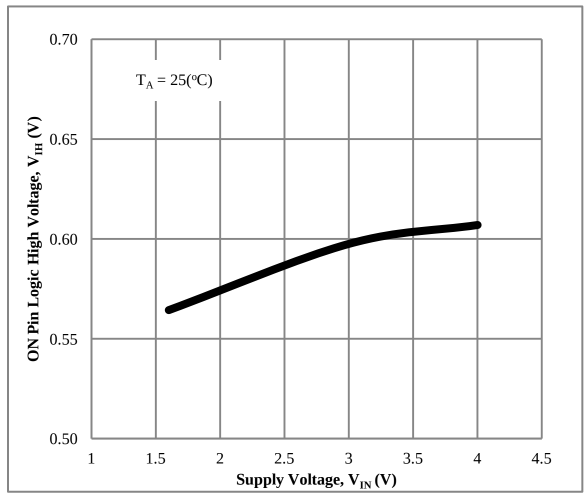


Figure 12. ON Pin Logic High Voltage vs. Supply Voltage

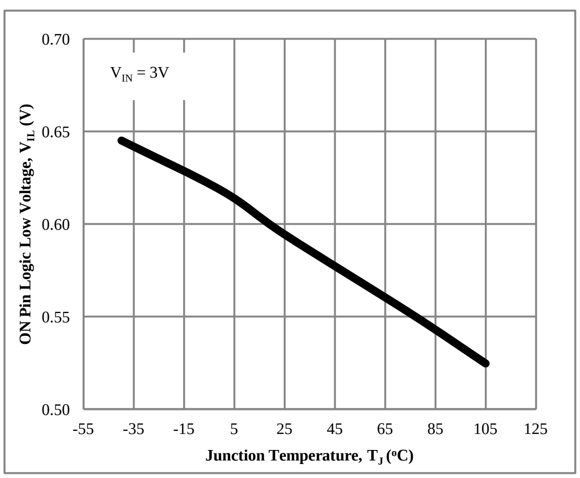


Figure 13. ON Pin Logic Low Voltage vs. Temperature

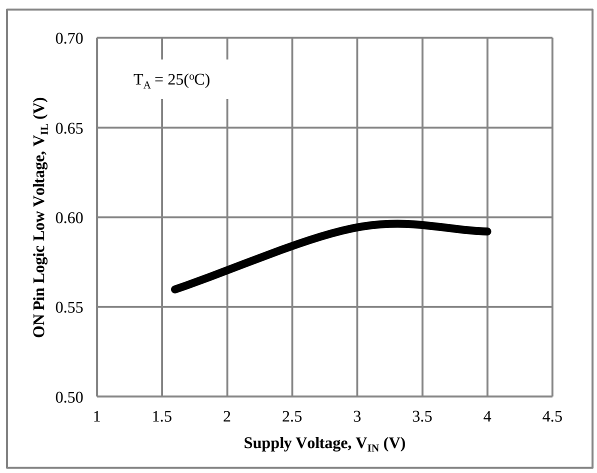


Figure 14. ON Pin Logic Low Voltage vs. Supply Voltage

Typical Performance Characteristics (Continued)

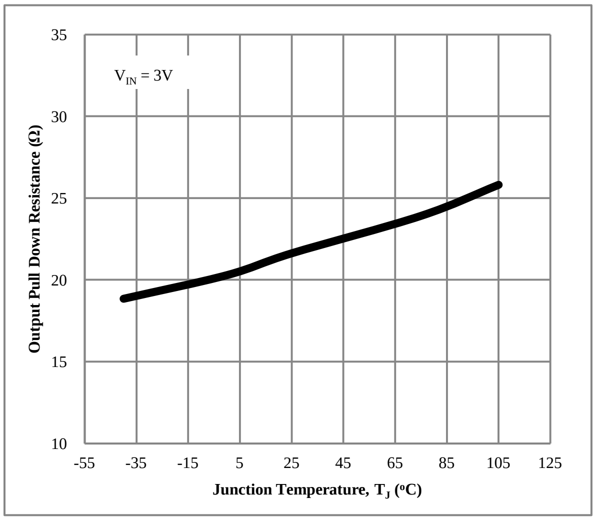


Figure 15. Output Pull Down Resistance vs. Temperature

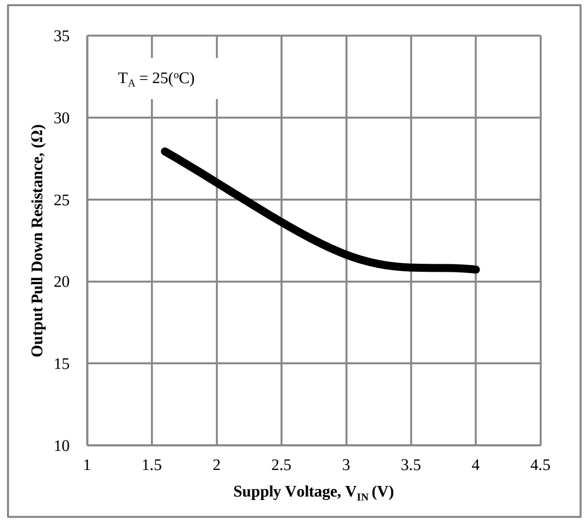


Figure 16. Output Pull Down Resistance vs. Supply Voltage

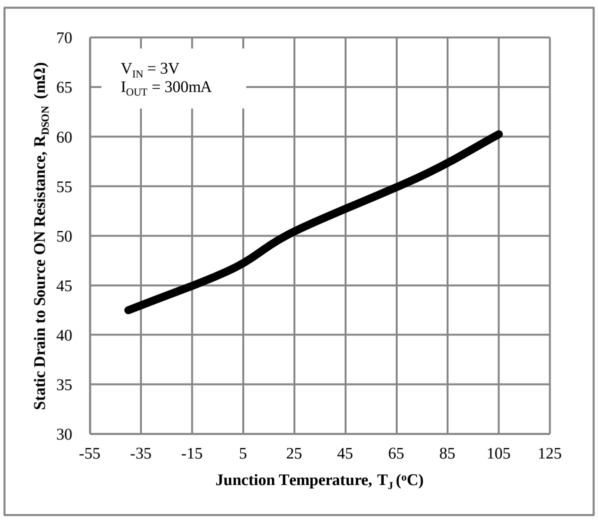


Figure 17. Static Drain to Source ON Resistance vs. Temperature

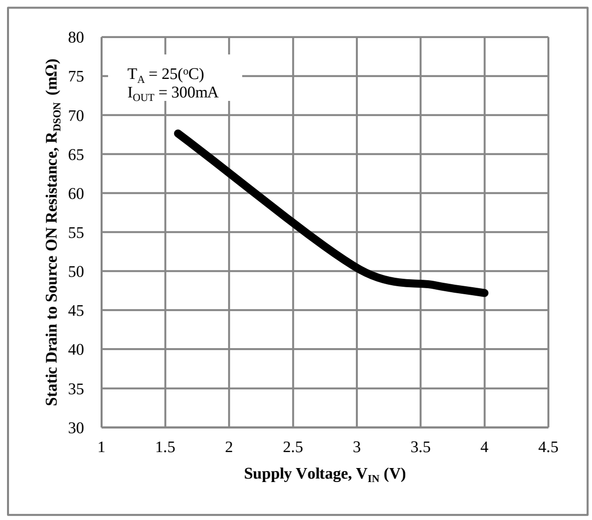
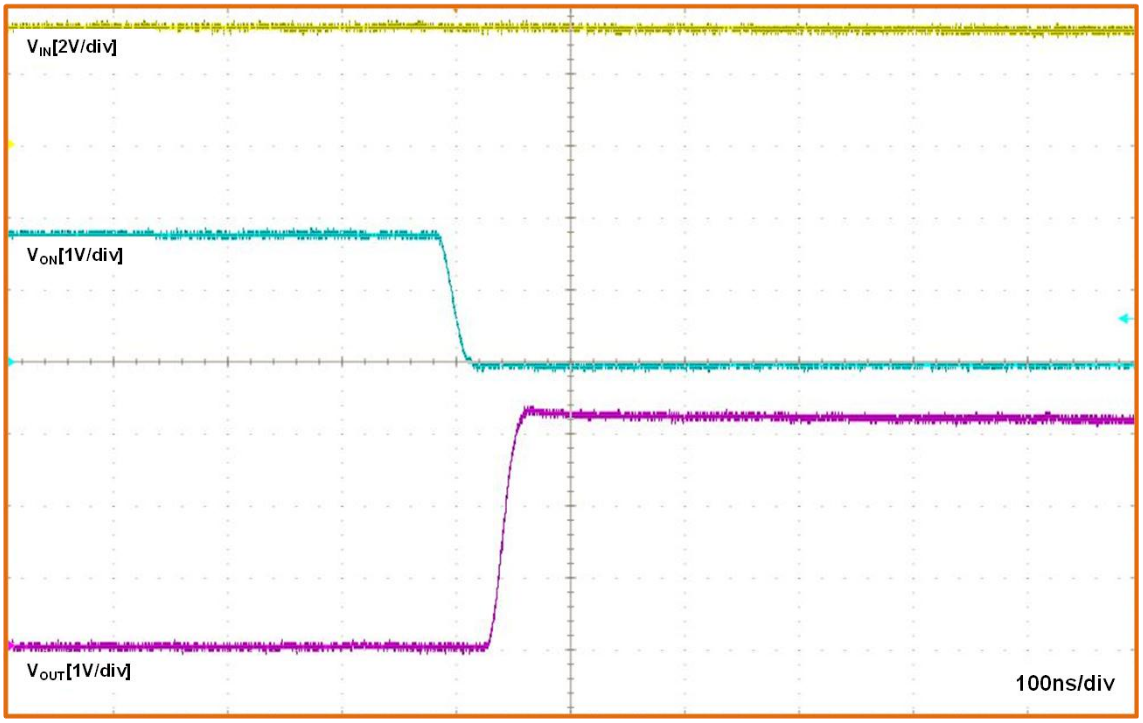


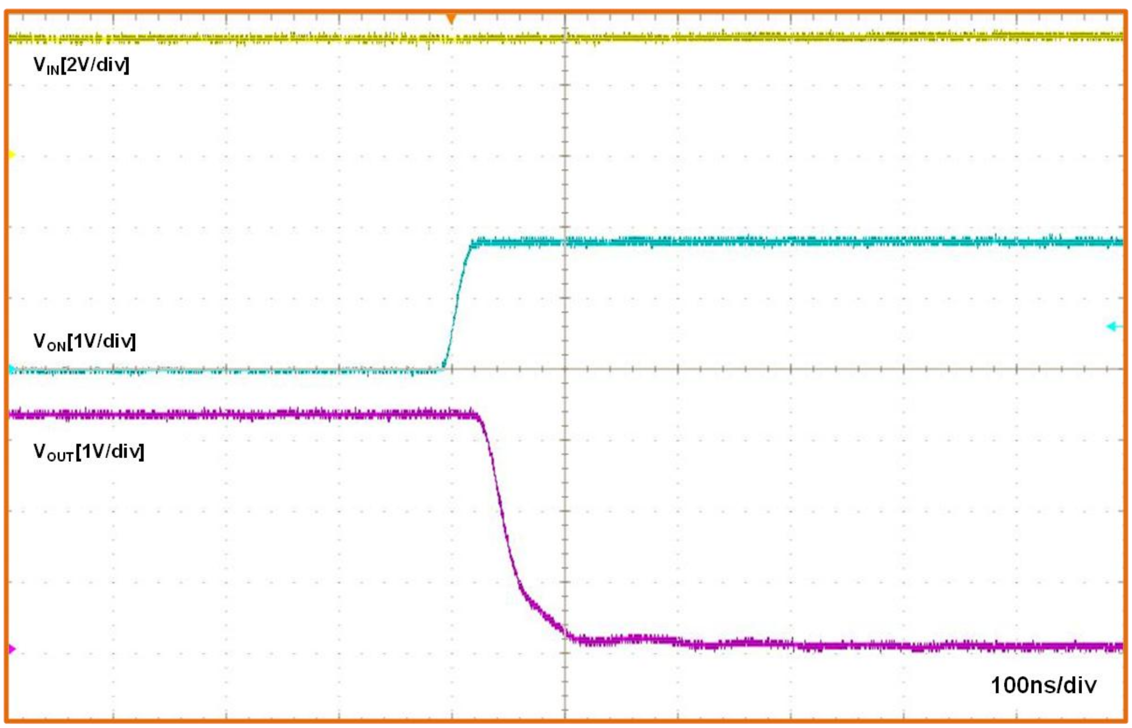
Figure 18. Static Drain to Source ON Resistance vs. Supply Voltage

Typical Performance Characteristics(Continued)



V_{IN} = 3.3V, V_{ON} = 0V, C_{IN} = 1uF, C_{OUT} = 1nF, R_L = 30Ω

Figure 19. T_{ON} Response



V_{IN} = 3.3V, V_{ON} = 0V, C_{IN} = 1uF, C_{OUT} = 1nF, R_L = 30Ω

Figure 20. T_{OFF} Response

Operation Description

The FDZ2040L is a low $R_{DS(ON)}$ P-Channel load switch packaged in space saving 0.8x0.8 WL-CSP.
The core of the device is a 80mΩ P-Channel MOSFET and capable of functioning over a wide input operating range of 1.6-4 V.

Applications Information

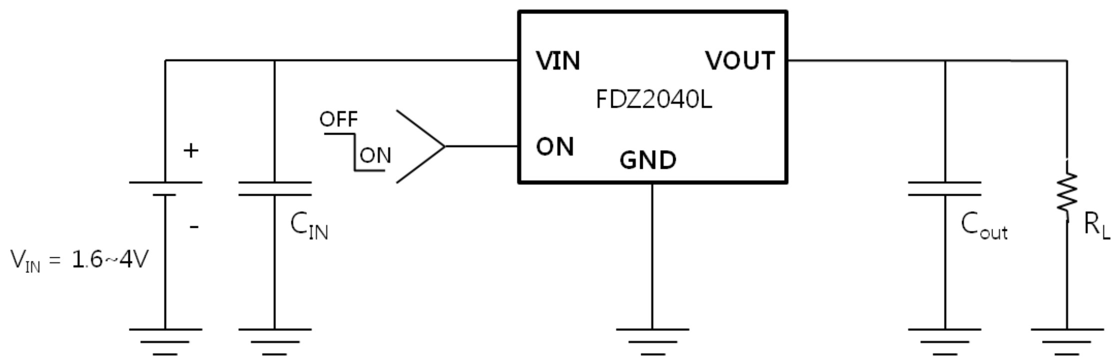


Figure 21. Typical Application

Input Capacitor

To reduce device inrush current effect, a 0.1uF ceramic capacitor, C_{IN} is recommended close to V_{IN} pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

FDZ2040L switch works without an output capacitor. However, if parasitic board inductance forces Vout below GND when switching off, a 1nF capacitor, C_{OUT}, should be placed between Vout and GND.

Notes: The intrinsic diode for P-Channel load switch would conduct if V_{OUT} is greater than V_{IN}, by a diode drop

Demo Board Layout

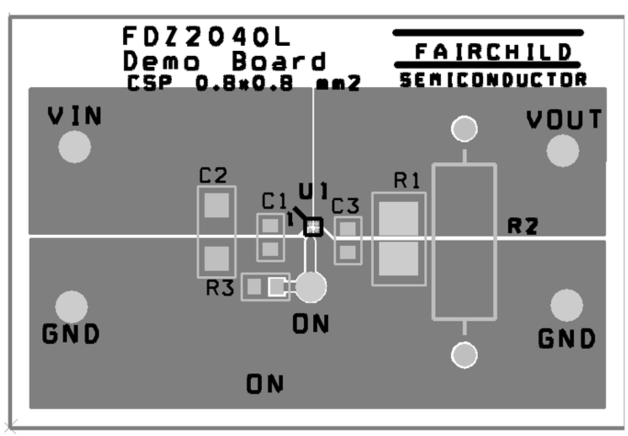


Figure 22. Top View

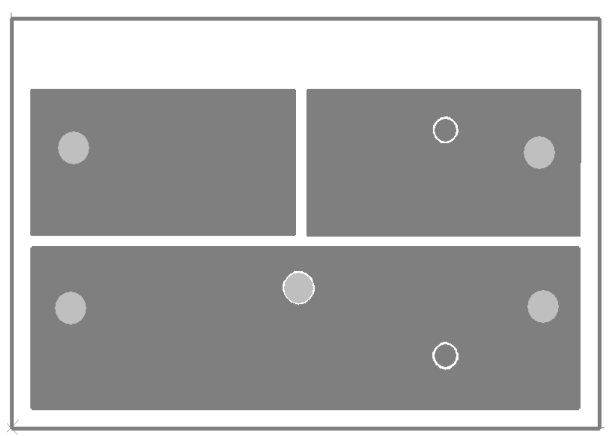


Figure 23. Bottom View

Dimensional Outline and Pad Layout

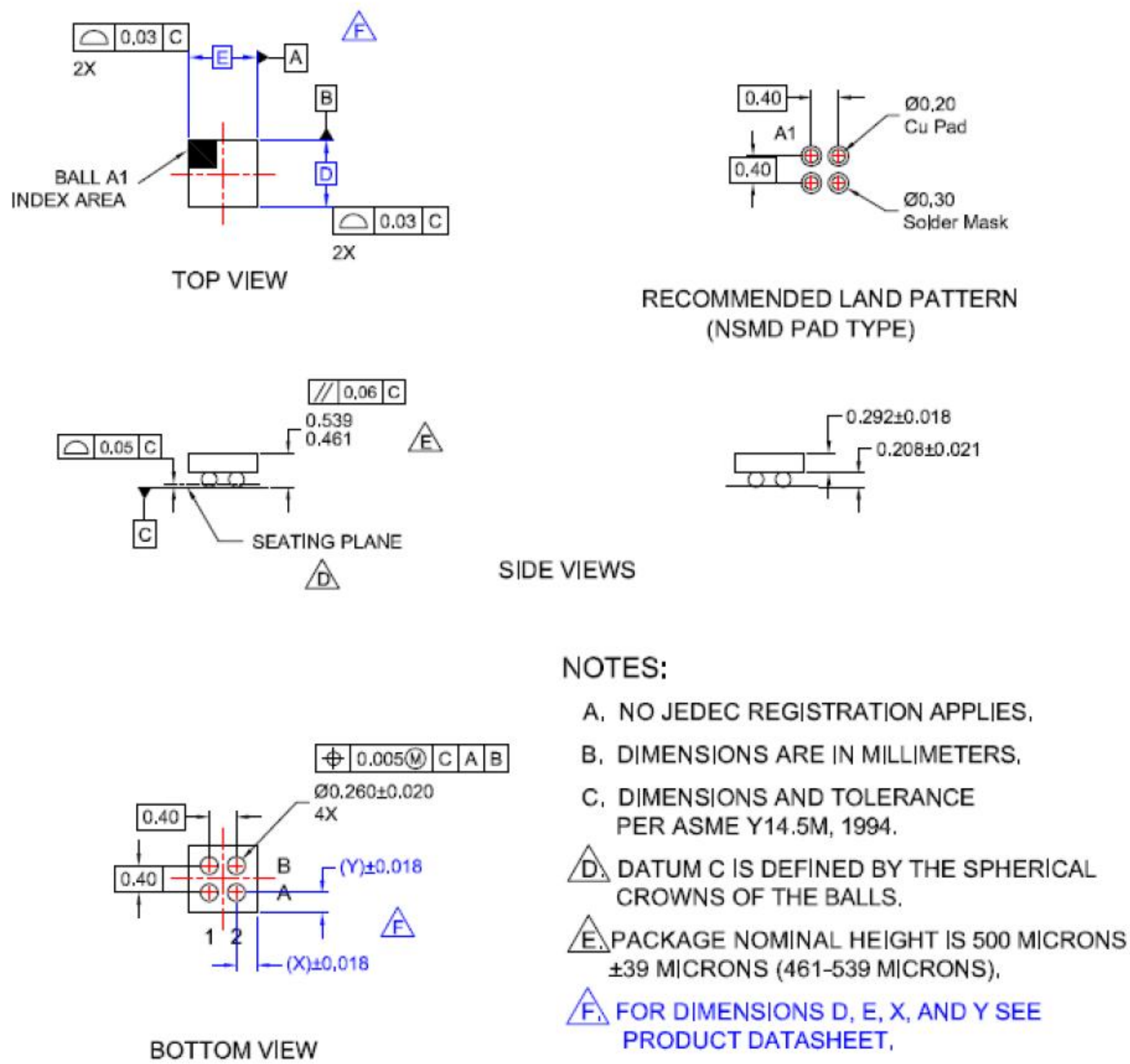


Figure 24. Official FSC Drawings

Product-Specific Dimensions

Product	D	E	X	Y
FDZ2040L	0.8 ± 0.03 mm	0.8 ± 0.03 mm	0.21 mm	0.21 mm

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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