FAN7191-F085, FAD7191

600 V / 4.5 A, High and Low Side Automotive Gate Driver IC

ON Semiconductor®

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SOIC8
CASE 751EB

SOIC14
CASE 751EF

Description

The FAN7191 / FAD7191 is a monolithic high− and low−side gate−driver IC, which can drive high speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse driving capability and minimum cross−conduction.

ON Semiconductor's high−voltage process and common−mode noise canceling technique provide stable operation of high−drivers under high dV/dt noise circumstances. An advanced level−shift circuit allows high−side gate driver operation up to V_S = −9.8 V (typical) for V_{BS} = 15 V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop features make this device suitable for controlling direct injection actuators and for use in many automotive DC−DC converter and motor control applications.

Features

- Floating Channel for Bootstrap Operation to +600 V
- 4.5 A Sourcing and 4.5 A Sinking Current Driving Capability
- Common−Mode dV/dt Noise Cancelling Circuit
- Built−in Under−Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- Output In−phase with Input
- 14−SOP with Separate Signal and Power Ground for Enhanced Noise Immunity
- 14−SOP with Increased Clearance for High Voltage Applications
- Automotive Applications, AEC Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Electric and Hybrid Electric Vehicles
- 48 V Mild Hybrid Vehicles
- Automotive High Voltage DC−DC converters
- Motor Control (Fans, Pumps, Compressors)
- Advanced Fuel Injection Systems
- Starter/Alternator
- Electric Power Steering
- MOSFET and IGBT Driver Applications

ORDERING INFORMATION

Part Number	Package	Shipping
FAN7191MX−F085	8−SOP (751EB)	2500 / Tape & Reel
FAD7191M1X	14−SOP (751EF)	2500 / Tape & Reel

Typical Application Circuit

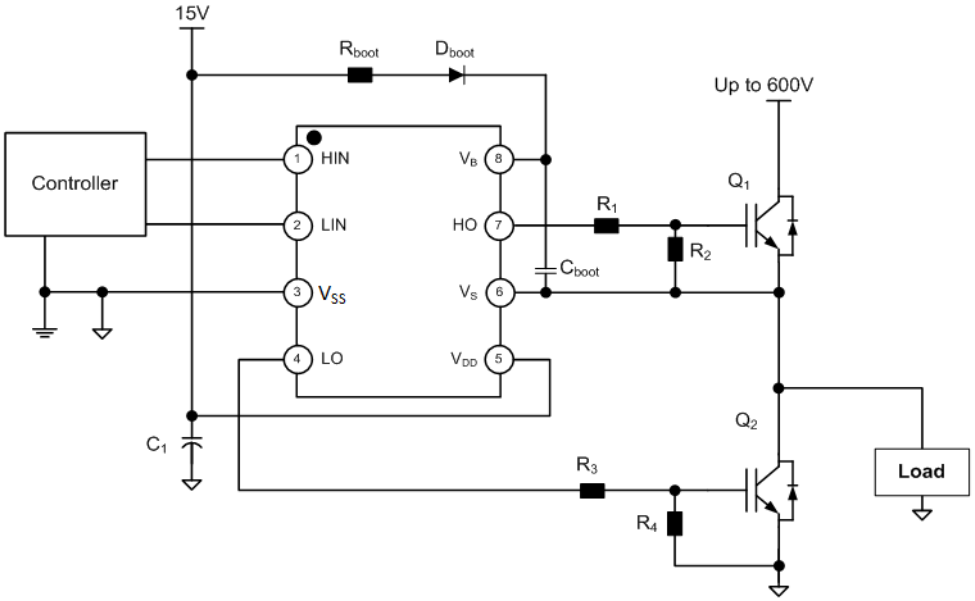


Figure 1. Half−Bridge Application Circuit (8−SOP)

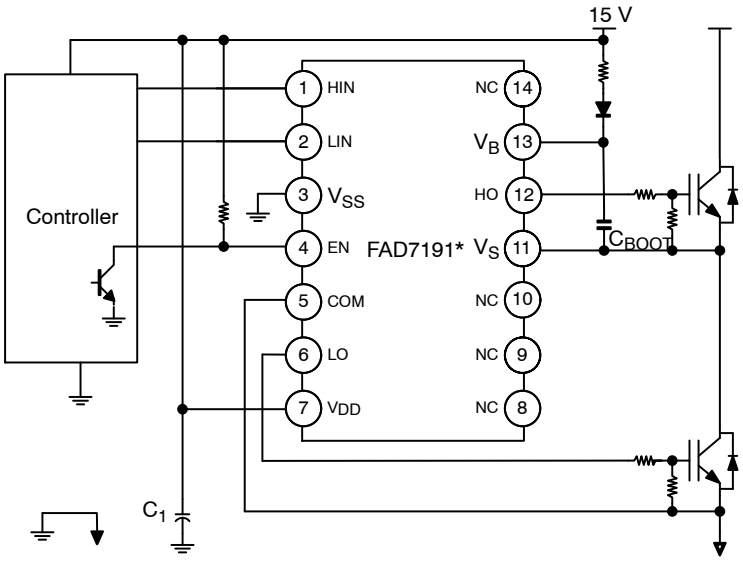


Figure 2. Half−Bridge Application Circuit (14−SOP)

INTERNAL BLOCK DIAGRAM

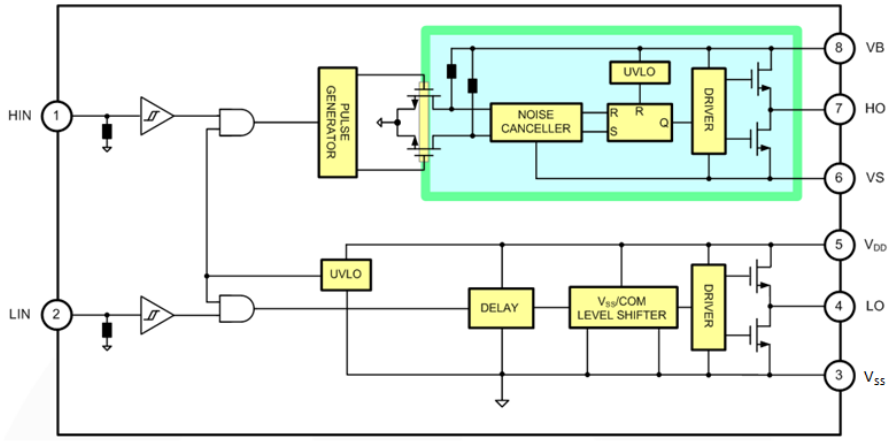


Figure 3. Functional Block Diagram (8−SOP)

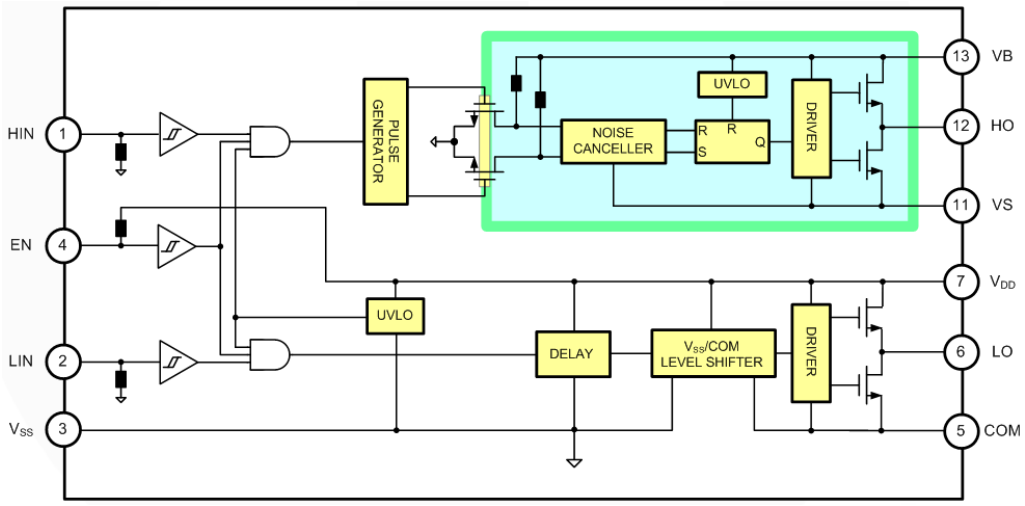


Figure 4. Functional Block Diagram (14−SOP)

Pin Assignment

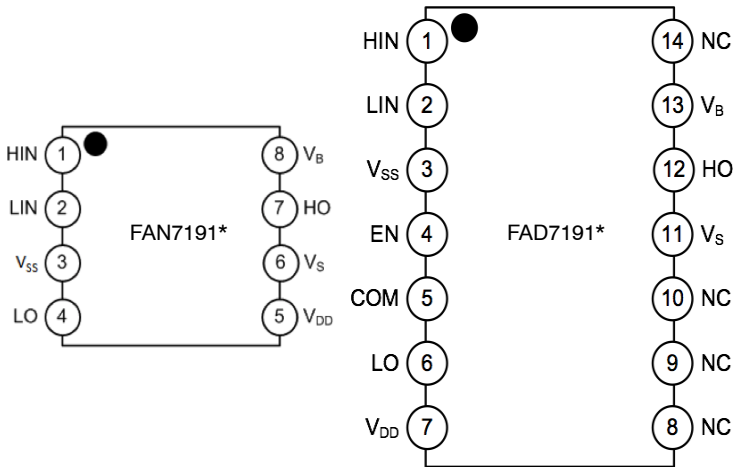


Figure 5. Pin Assignments (Top View)

Table 1. PIN DEFINITIONS

8−Pin	14−Pin	Name	Description
1	1	HIN	Logic Input for High−Side Gate Driver Output
2	2	LIN	Logic Input for Low−Side Gate Driver Output
3	3	V_{SS}	Logic Ground, Power ground for 8−SOP
	4	EN	Enable Input (Internal Pull Up)
	5	COM	Power Ground for 14−SOP, Low−side Driver Return
4	6	LO	Low−Side Driver Output
5	7	V_{DD}	Low−Side and Logic Power Supply Voltage
6	11	V_S	High−Side Floating Supply Return
7	12	HO	High−Side Driver Output
8	13	V_B	High−Side Floating Supply
	8, 9, 10, 14	NC	No Connect

Table 2. ABSOLUTE MAXIMUM RATINGS
(T_A = −40°C to 125°C, unless otherwise specified. V_B, V_{DD} and V_{IN} are referenced to V_{SS})

Symbol	Parameter			Min.	Max.	Unit
V_S	High−side offset voltage VS			V_B − 25	V_B + 0.3	V
V_B	High−side floating supply voltage VB			−0.3	625	V
V_{HO}	High−side floating output voltage			V_S − 0.3	V_B + 0.3	V
V_{DD}	Low−side and logic−fixed supply voltage			−0.3	25	V
COM	Power Ground (14−SOP)			V_{DD} − 25	V_{DD} + 0.3	V
V_{IN}	Logic Input voltage (HIN, LIN, EN)			−0.3	V_{DD} + 0.3	V
V_{LO}	Low−Side Output Voltage LO (8−SOP)			V_{SS} − 0.3	V_{DD} + 0.3	V
	Low−Side Output Voltage LO (14−SOP)			COM − 0.3	V_{DD} + 0.3	V
T_{pulse} (Note 4)	Minimum Pulse Width			80		ns
$d_{VS/dt}$	Allowable offset voltage slew rate				50	V/ns
P_D (Note 1, 2, 3)	Power Dissipation, T_A = 25°C		8−SOP		0.625	W
			14−SOP		0.80	W
θ_{JA} (Note 1, 2)	Thermal Resistance, junction−to−ambient		8−SOP		200	°C/W
			14−SOP		156	°C/W
T_J	Junction temperature				+150	°C
T_S	Storage temperature			−55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	8−SOP		3000	V
			14−SOP		2000	
		Charged Device Model, JESD22−C101			2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Mounted on 76.2 × 114.3 × 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards: JESD51−2: Integral circuits thermal test method environmental conditions − natural convection. JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages.
3. P_D is the power that raises T_J to 150°C for T_A = 25°C. P_D to be derated at higher ambient temperature.
4. Minimum input pulse width that guarantee to produce an output pulse. Valid for turn on and turn off pulse width.

Table 3. RECOMMENDED OPERATING CONDITIONS (V_S, V_{DD} and V_{IN} are referenced to V_{SS})

Symbol	Parameter	Min.	Max.	Unit
V_B	High−side floating supply voltage	V_S + 10	V_S + 22	V
V_S	High−side Floating Supply Offset Voltage	6 − V_{BS}	600	V
V_{HO}	High−side Output Voltage	V_S	V_B	V
V_{DD}	Low−side and Logic Supply voltage	10	22	V
V_{LO}	Low−side output voltage (8−SOP)	0	V_{DD}	V
	Low−side output voltage (14−SOP)	COM	V_{DD}	V
V_{IN}	Logic input voltage (HIN, LIN, EN)	0	V_{DD}	V
COM	Power Ground (14−SOP)	V_{DD} − 22	V_{DD}	V
T_A	Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, V_S = V_{SS} = COM, T_A = −40°C to 125°C, unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM (or V_{SS} in case of 8−SOP). V_S and COM (V_{SS} for 8−SOP) are applicable to the respective outputs HO and LO)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION (V_{DD} AND V_{BS})						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under−Voltage Positive−going Threshold		7.8	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under−Voltage Negative Going Threshold		7.2	8.3	9.1	
V_{DDHYS}	V_{DD} supply under−voltage lockout hysteresis			0.5		
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600 V			50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V		45	110	
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN} = 0 V or 5 V		75	150	
I_{PBS}	Operating V_{BS} Supply Current	f_{IN} = 20 kHz, RMS value (See Figure 26)		400	800	μA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN} = 20 kHz, RMS value (See Figure 26)		400	800	
LOGIC INPUT SECTION (HIN, LIN, EN)						
V_{IH}	Logic “1” Input Voltage		2.5			V
V_{IL}	Logic “0” Input Voltage				1.2	
I_{IN+}	Logic “1” Input Bias Current (HIN/LIN)	V_{IN} = 5 V		25	50	μA
I_{IN-}	Logic “0” Input Bias Current (HIN/LIN)	V_{IN} = 0 V		1.0	2.0	
I_{EN+}	Enable High Input Bias Current	EN = 5 V	−100	−50	−10	
I_{EN-}	Enable Low Input Bias Current	EN = 0 V	−140	−75	−20	
R_{IN}	Input Pull−down Resistance		100	200		kΩ
GATE DRIVER OUTPUT SECTION (HO, LO)						
V_{OH}	High−level Output Voltage, V_{BIAS}−V_O	No Load			1.35	V
V_{OL}	Low−level Output Voltage, V_O	No Load			35	mV
I_{O+} (Note 5)	Output HIGH, Short−circuit Pulsed Current	V_O = 0 V, V_{IN} = 5 V with PW < 10μs	3.5	4.5		A
I_{O-} (Note 5)	Output LOW Short−circuit Pulsed Current	V_O = 15 V, V_{IN} = 0 V with PW < 10 μs	3.5	4.5		
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO	V_{BS} = 15V		−9.8	−9.0	V
COM−V_{SS} (Note 5)	Allowable COM−V_{SS} ground offset	14−SOP, V_{DD} = 15 V, V_{SS} = 0 V	−7.0			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Parameters guaranteed by design.

Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, V_S = V_{SS} = COM = 0 V, T_A = −40°C to 125°C, C_{LOAD} = 1000 pF unless otherwise specified)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn−on Propagation Delay	V_S = 0 V		140	200	ns
t_{off}	Turn−off Propagation Delay	V_S = 0 V		140	200	ns
MT	Delay Matching				55	ns
t_r	Turn−on Rise Time			25	50	ns
t_f	Turn−off Fall Time			25	50	ns

Typical Characteristics

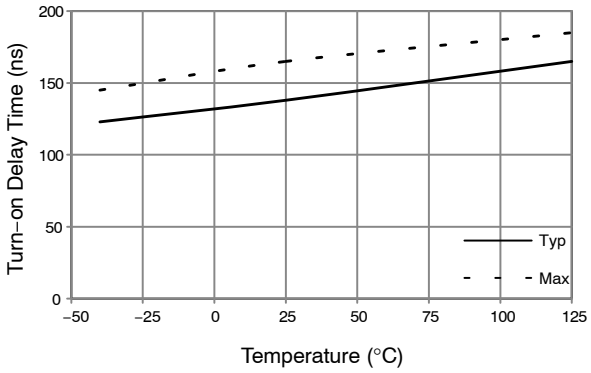


Figure 6. Turn−on Propagation Delay vs. Temperature

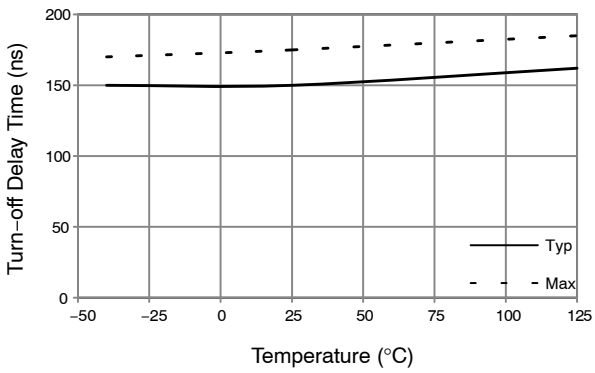


Figure 7. Turn−off Propagation Delay vs. Temperature

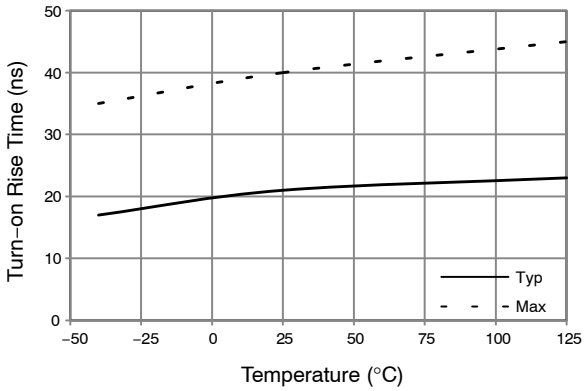


Figure 8. Turn−on Rise Time vs. Temperature

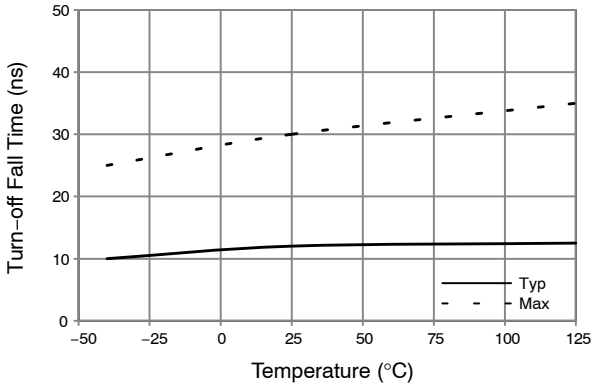


Figure 9. Turn−off Fall Time vs. Temperature

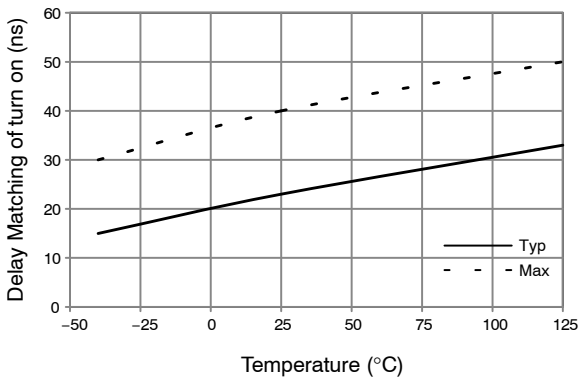


Figure 10. Turn-on Delay Matching vs. Temperature

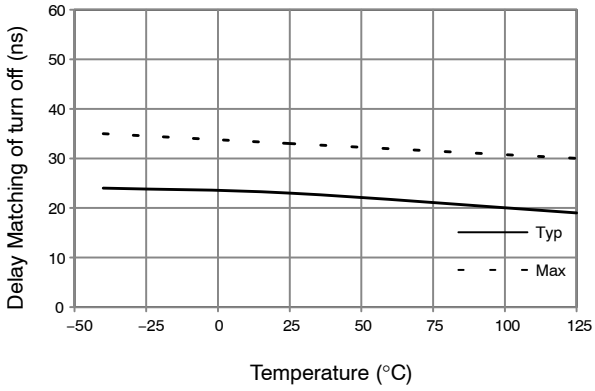


Figure 11. Turn-off Delay Matching vs. Temperature

Typical Characteristics (continued)

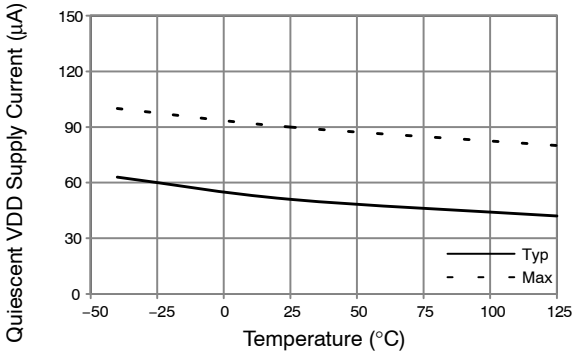


Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

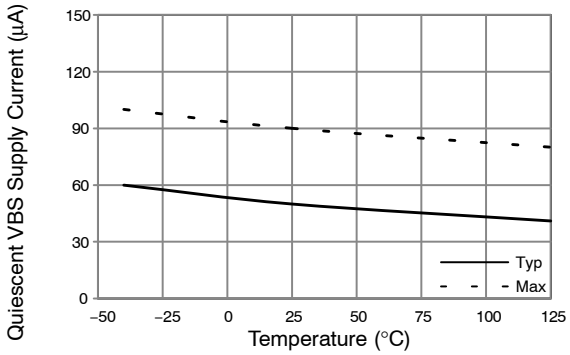


Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

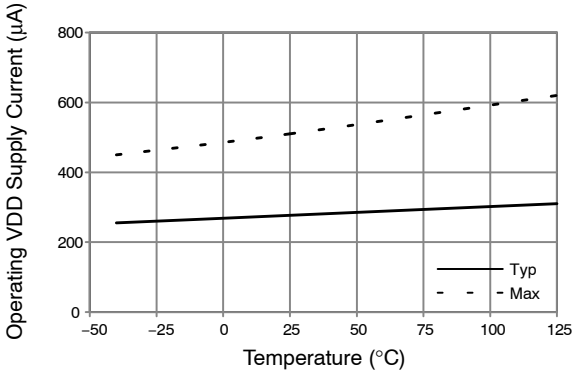


Figure 14. Operating V_{DD} Supply Current vs. Temperature

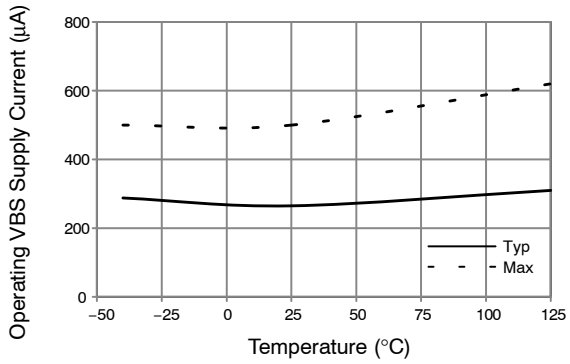


Figure 15. Operating V_{BS} Supply Current vs. Temperature

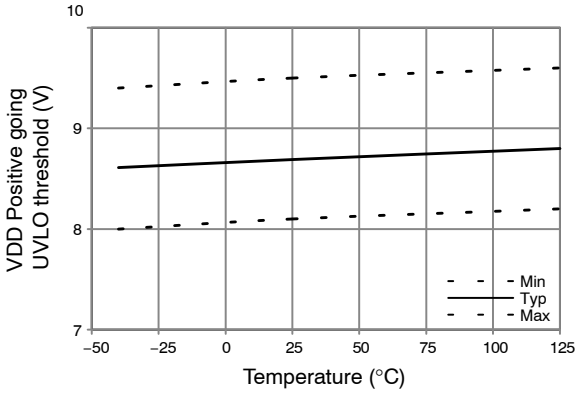


Figure 16. V_{DD} UVLO+ vs. Temperature

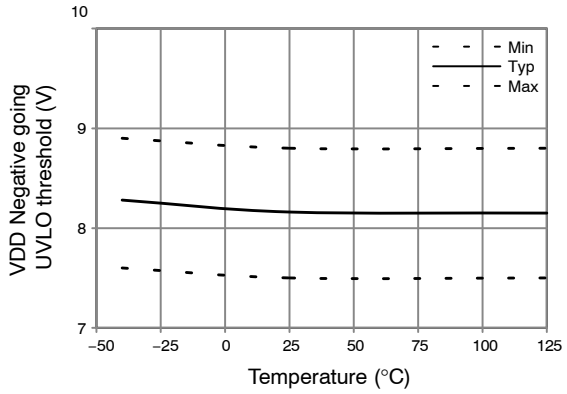


Figure 17. V_{DD} UVLO− vs. Temperature

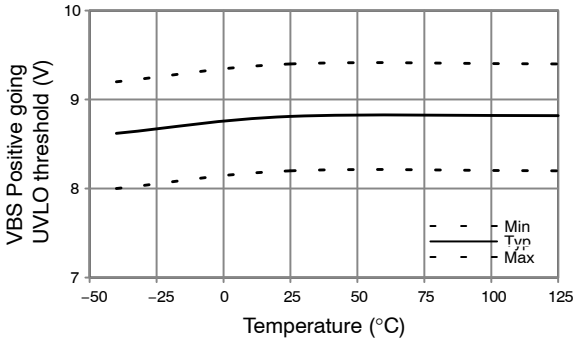


Figure 18. V_{BS} UVLO+ vs. Temperature

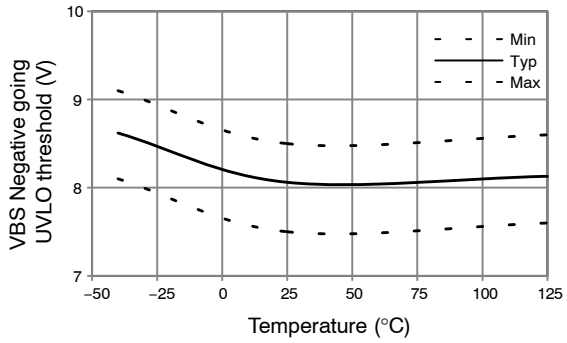


Figure 19. V_{BS} UVLO− vs. Temperature

Typical Characteristics (continued)

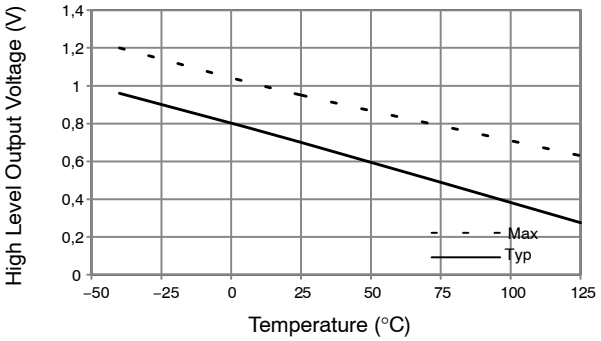


Figure 20. High−Level Output Voltage vs. Temperature

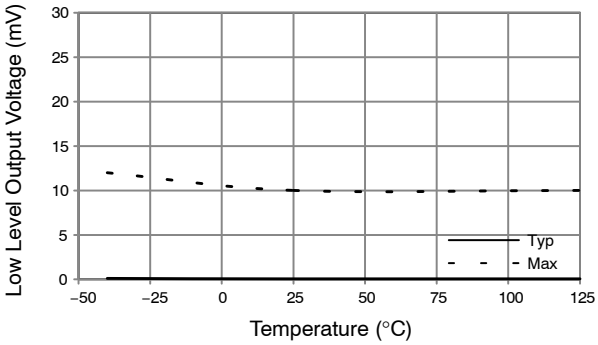


Figure 21. Low−Level Output Voltage vs. Temperature

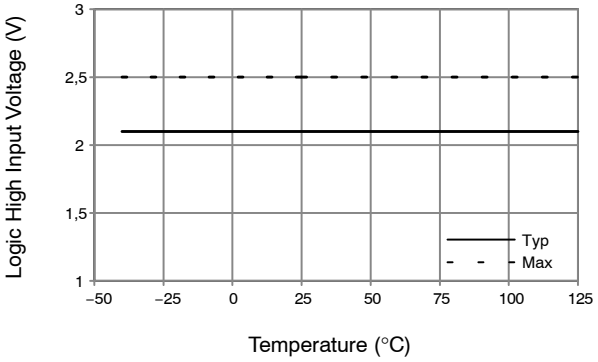


Figure 22. Logic High Input Voltage vs. Temperature

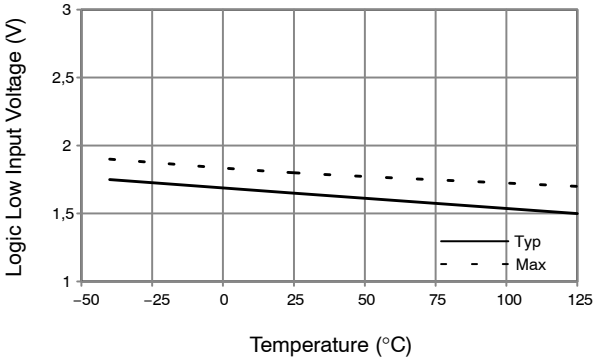


Figure 23. Logic Low Input Voltage vs. Temperature

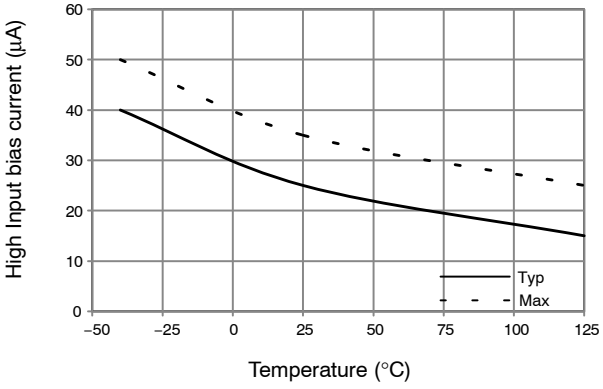


Figure 24. Logic “1” Input Bias Current vs. Temperature

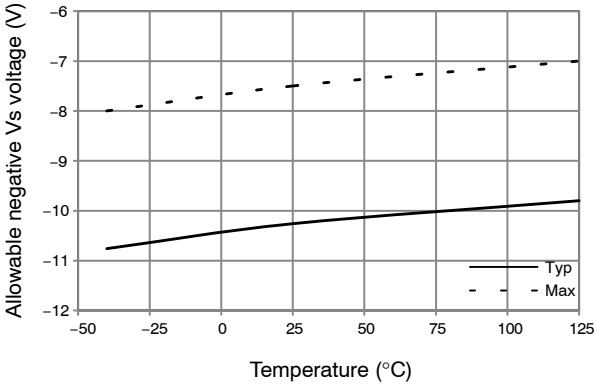


Figure 25. Allowable Negative VS Voltage vs. Temperature

Switching Time Definitions

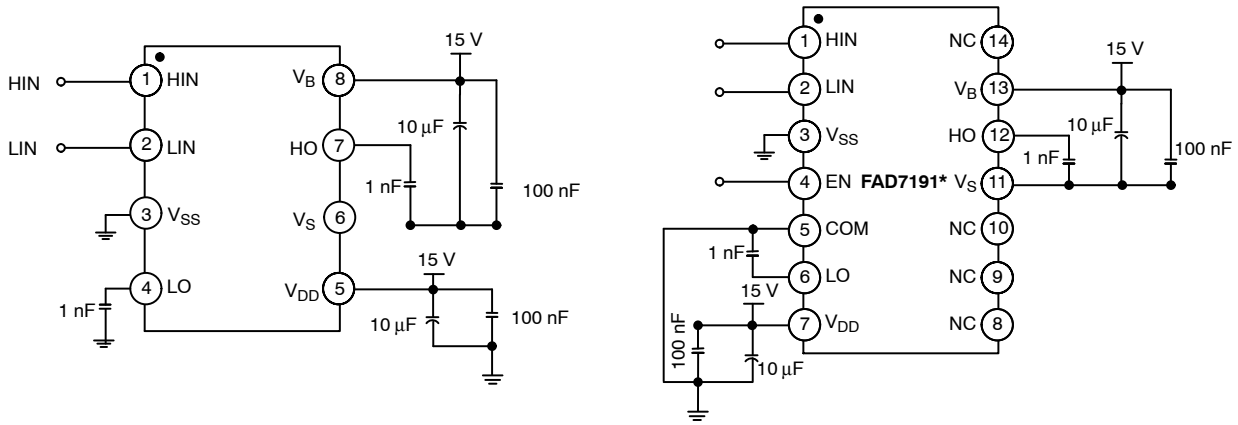


Figure 26. Switching Time Test Circuit

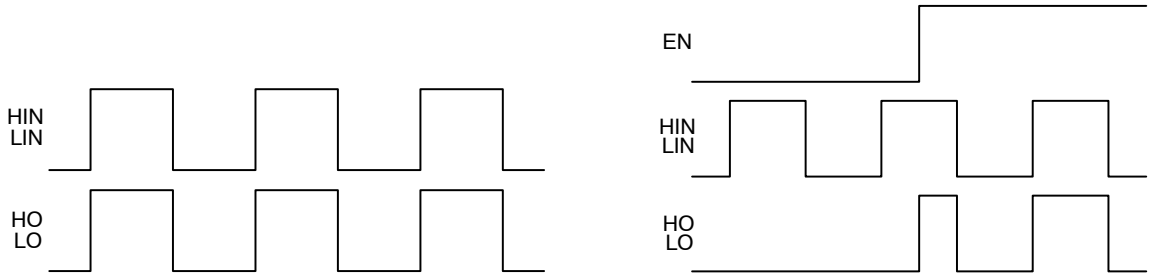


Figure 27. Input / Output Timing Diagram

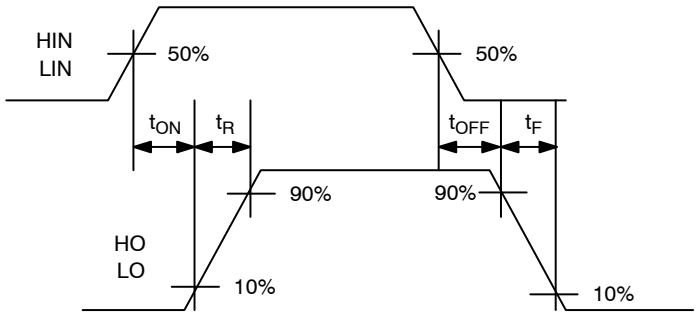


Figure 28. Switching Time Waveform Definitions

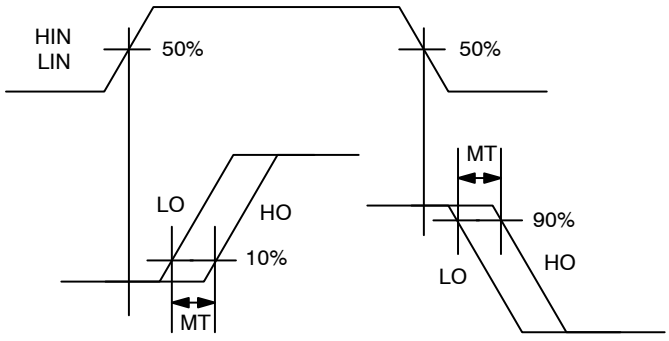
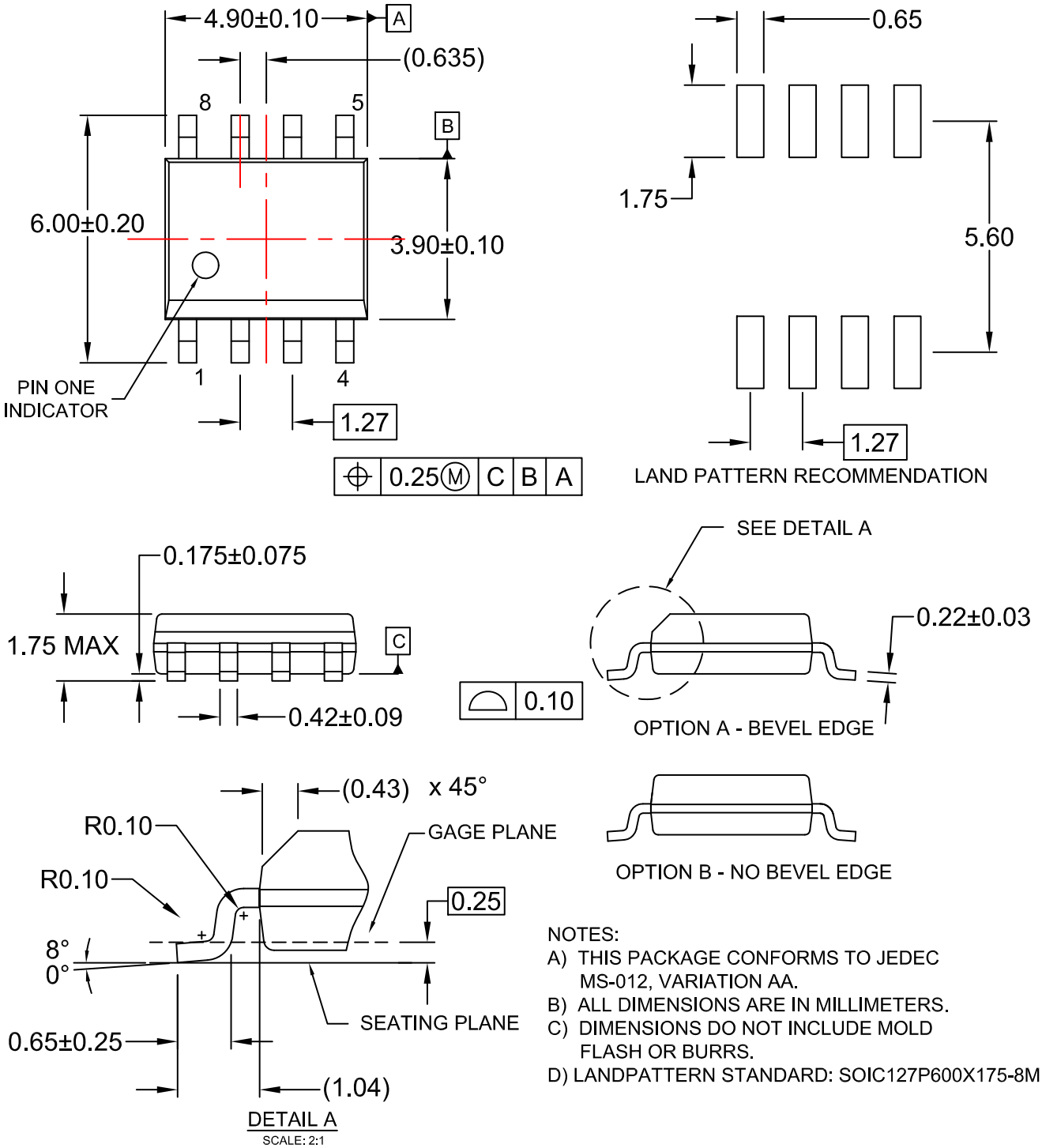


Figure 29. Delay Matching Waveform Definition

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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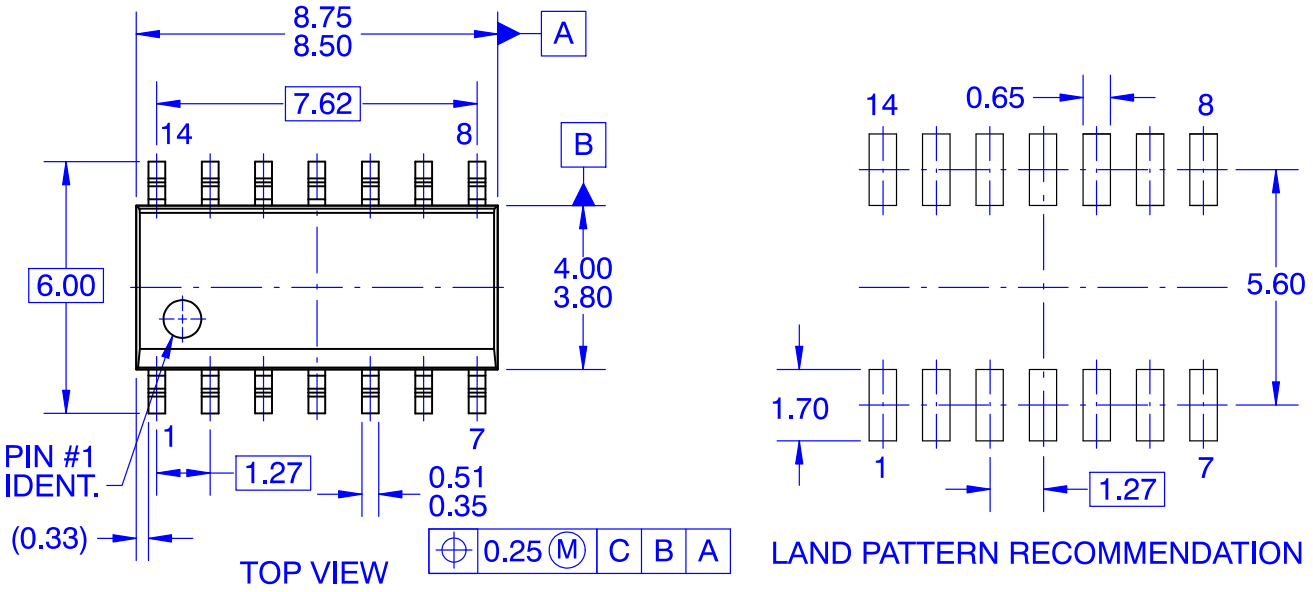
STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**SOIC8**		**PAGE 1 OF 2**

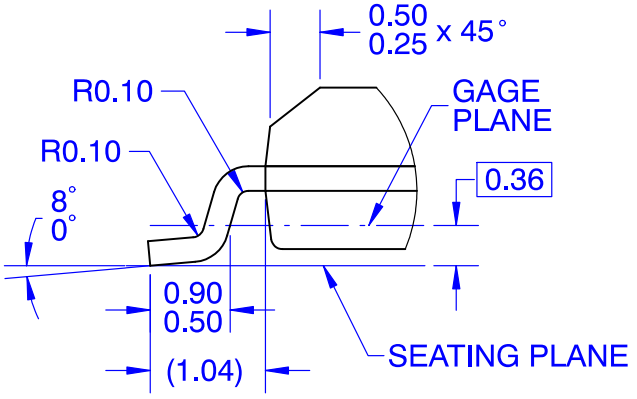
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD M08A TO ON SEMICONDUCTOR. REQ. BY B. MARQUIS.	30 SEP 2016
A	CORRECTED DIMENSIONAL ERROR IN DETAIL A. REQ. BY H. ALLEN.	24 AUG 2017

SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:
A. CONFORMS TO JEDEC MS–012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145–14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

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