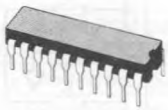
SGS-THOMSON MICROELECTRONICS

ETC5067
ETC5064

SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

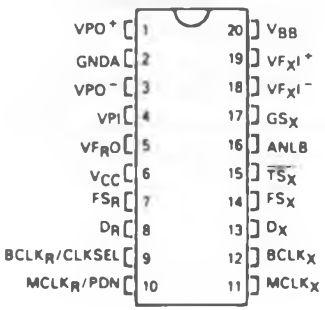
- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
  - Receive push-pull power amplifiers
- μ -LAW ETC5064
- A-LAW ETC5067
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY



DIP20
(Ceramic) J
(Plastic) N

ORDER CODES : ETC5067J
ETC5064J
ETC5067N
ETC5064N

PIN CONNECTIONS



DESCRIPTION

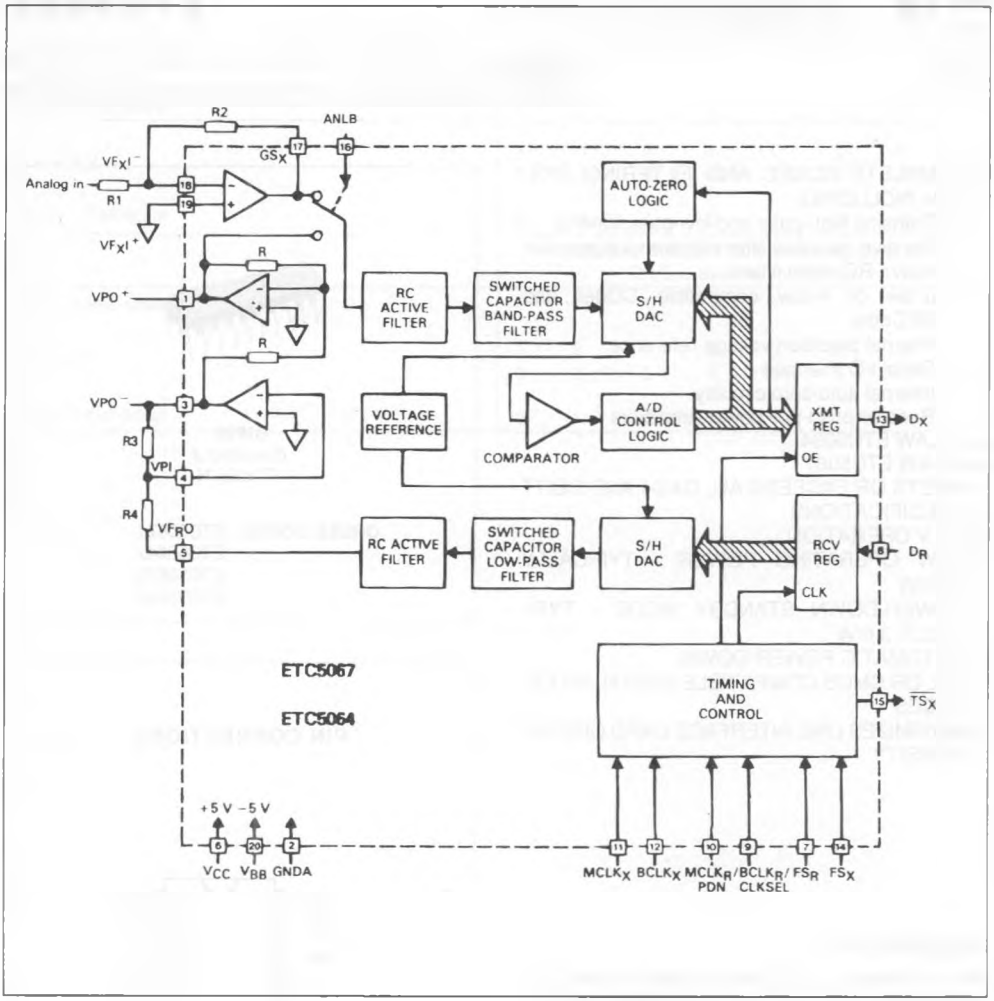
The ETC5064 (μ-law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in figure 1, and a serial PCM interface.

The devices are fabricated using double poly CMOS process.

Similar to the ETC505X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600 Ω load.

Also included is an Analog Loopback switch and $\overline{TS}_X$ output.

Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type*	N°	Description
VPO^+	O	1	The Non-inverting Output of the Receive Power Amplifier
GNDA	GND	2	Analog Ground. All signals are referenced to this pin.
VPO^-	O	3	The Inverting Output of the Receive Power Amplifier
VPI	I	4	Inverting Input to the Receive Power Amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter.
V_{CC}	S	6	Positive Power Supply Pin. V_{CC} = + 5 V + 5 %
FS_R	I	7	Receive Frame Sync Pulse which enable $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 2 and 3 for timing details.
D_R	I	8	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	9	The bit Clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	10	Receive Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	11	Transmit Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	12	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	13	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	14	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 2 and 3 for timing details.
$\overline{TS_X}$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used.
ANLB	I	16	Analog Loopback Control Input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier. The input has an internal* pull down.
GS_X	O	17	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	18	Inverting input of the transmit input amplifier.
VF_XI^+	I	19	Non-inverting input of the transmit input amplifier.
V_{BB}	S	20	Negative Power Supply Pin. V_{BB} = – 5 V ± 5 %

* I : Input, O : Output, S : Power Supply.

TRI-STATE ® is a trademark of National Semiconductor Corp.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC 5067	ETC 5064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5067, or 1.536 MHz 1.544 MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 KHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 4. Based on the transmit frame sync, FS_X, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulses must be kept low for a minimum of 160 ns (see fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eight rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 5. The low noise and wide band-width allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active prefilter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067) or μ-law (ETC5064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5067) or μ-law (ETC5064) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface tranformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5 V peak output signal from the receive filter up ± 3.3 V peak into an unbalanced 300 Ω load, or 4.0 V into an unbalanced 15 k load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio, as shown in figure 5. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12 mW of power.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN} V_{OUT}	Voltage at Any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temeperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C : all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		–	–	0.6	V
V_{IH}	Input High Voltage		2.2	–	–	V
V_{OL}	Output Low Voltage					V
	I_L = 3.2 mA	D_X	–	–	0.4	
	I_L = 3.2 mA, Open Drain	$\overline{TS_X}$	–	–	0.4	
V_{OH}	Output High Voltage					V
	I_H = – 3.2 mA	D_X	2.4	–	–	
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs, except $BCLK_R$)		– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except ANLB		– 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE)					µA
	(GNDA ≤ V_O ≤ V_{CC})	D_X	– 10	–	10	

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_iXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_iXA	Input Resistance (– 2.5 ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)		–	1	3	Ω
R_LXA	Load Resistance	GS_X	10	–	–	kΩ
C_LXA	Load Capacitance	GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000	–	–	V/V
F_UXA	Unity Gain Bandwidth		1	2	–	MHz
$V_{OS}XA$	Offset Voltage		– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio		60	–	–	dB
PSRRXA	Power Supply Rejection Ratio		60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO + ± 2.5 V)		10	–	–	kΩ
C_LRF	Load Capacitance		–	–	25	pF
VOS_RO	Output DC Offset Voltage		– 200	–	200	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100	–	100	nA
RIPI	Input Resistance (– 1.0 V ≤ VPI ≤ 1.0 V)	10	–	–	MΩ
VIOS	Input Offset vOltage	– 25	–	– 25	mV
ROP	Output Resistance (inverting unity-gain at VPO $^+$ or VPO $^-$)	–	1	–	Ω
F_C	Unity-gain Bandwidth, Open Loop (VPO $^-$)	–	400	–	kHz
C_LP	Load Capacitance (VPO $^+$ or VPO $^-$ to GNDA) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$	 – – –	 – – –	 100 500 1000	pF
GAp $^+$	Gain VPO $^-$ to VPO $^+$ to GNDA, Level at VPO $^-$ = 1.77 Vrms (+ 3 dBm0)	–	– 1	–	V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB} (VPO $^-$ connected to VPI) 0 kHz – 4 kHz 0 kHz – 50 kHz	 60 36	 – –	 – –	dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	1.5	mA
$I_{BB}0$	Power-down Current	–	0.05	0.3	mA
$I_{CC}1$	Active Current	–	7.0	10.0	mA
$I_{BB}1$	Active Current	–	7.0	10.0	mA

ALL TIMING SPECIFICATIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clocks $MCLK_X$ and $MCLK_R$ Depends on the device used and the $BCLK_R$/CLKSEL pin.		– – –	1.536 2.048 1.544	– – –	MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)		160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)		160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{SBFM}	Set-up Time from $BCLK_X$ High to $MCKL_X$ Falling Edge (first bit clock after the leading edge of FS_X)		100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)		80	–	–	ns

Note : For short frame sync. timing FS_X and FS_R must go high while their respective bit clocks are high.

ALL TIMING SPECIFICATIONS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100	–	–	ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20	–	165	ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid (Load = 150 pF plus 2 LSTTL loads)	0	–	150	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	50	–	–	ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0	–	–	ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80	–	–	ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100	–	–	ns
t_{XDP}	Delay Time TS_X Low (load = 150 pF plus 2 LSTTL loads)	–	–	140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160	–	–	ns

Note : 1. For short frame sync. timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 2 : 64 k bits/s TIMING DIAGRAM (see next page for complete timing).

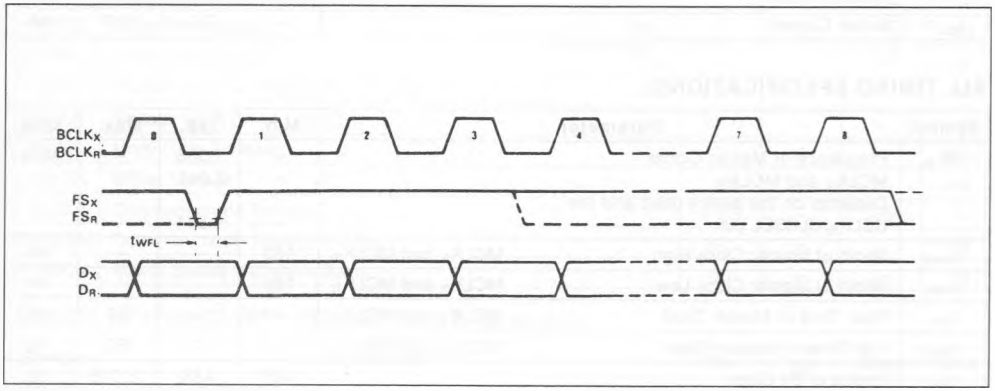


Figure 3 : Short Frame Sync Timing.

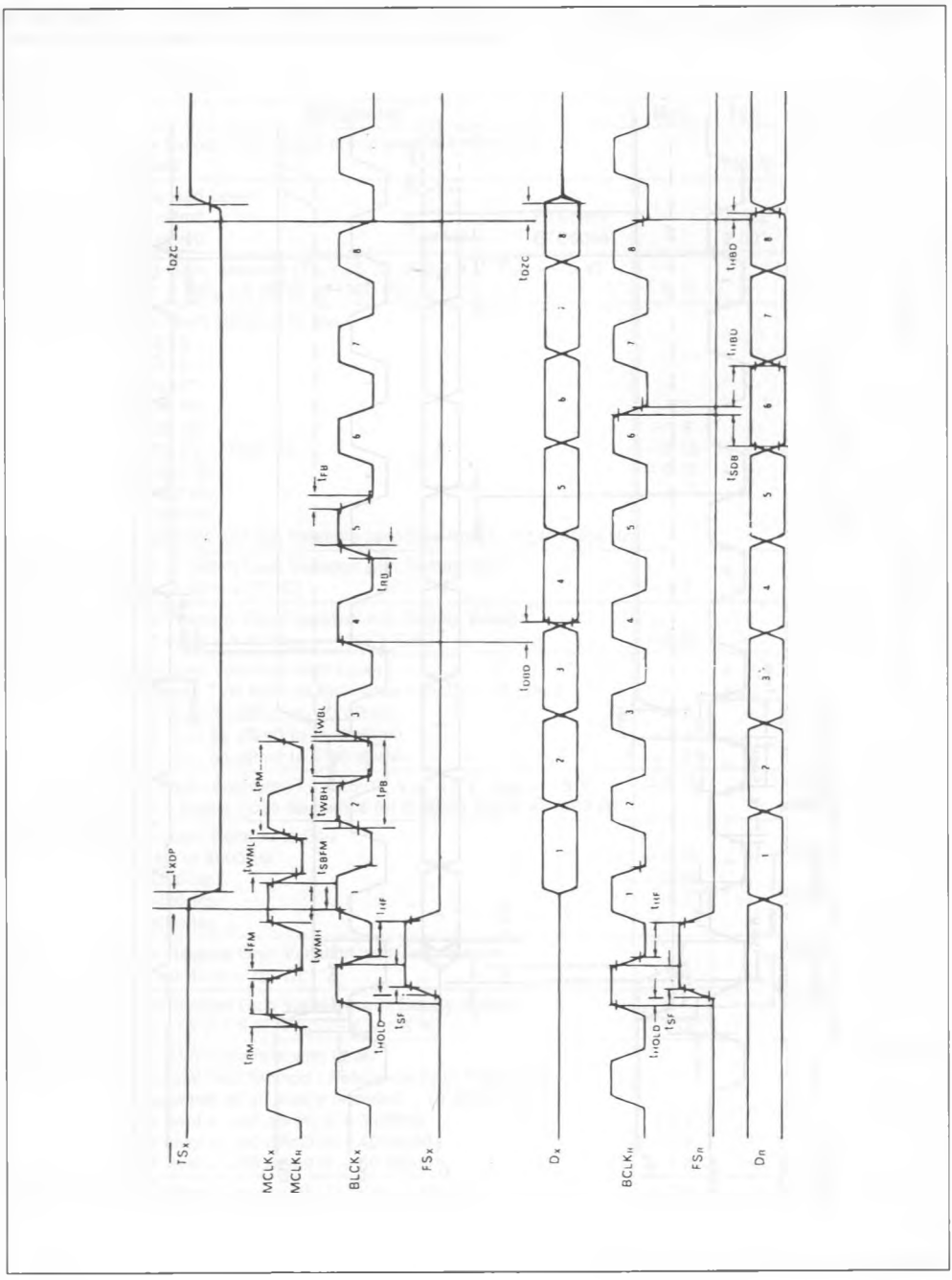
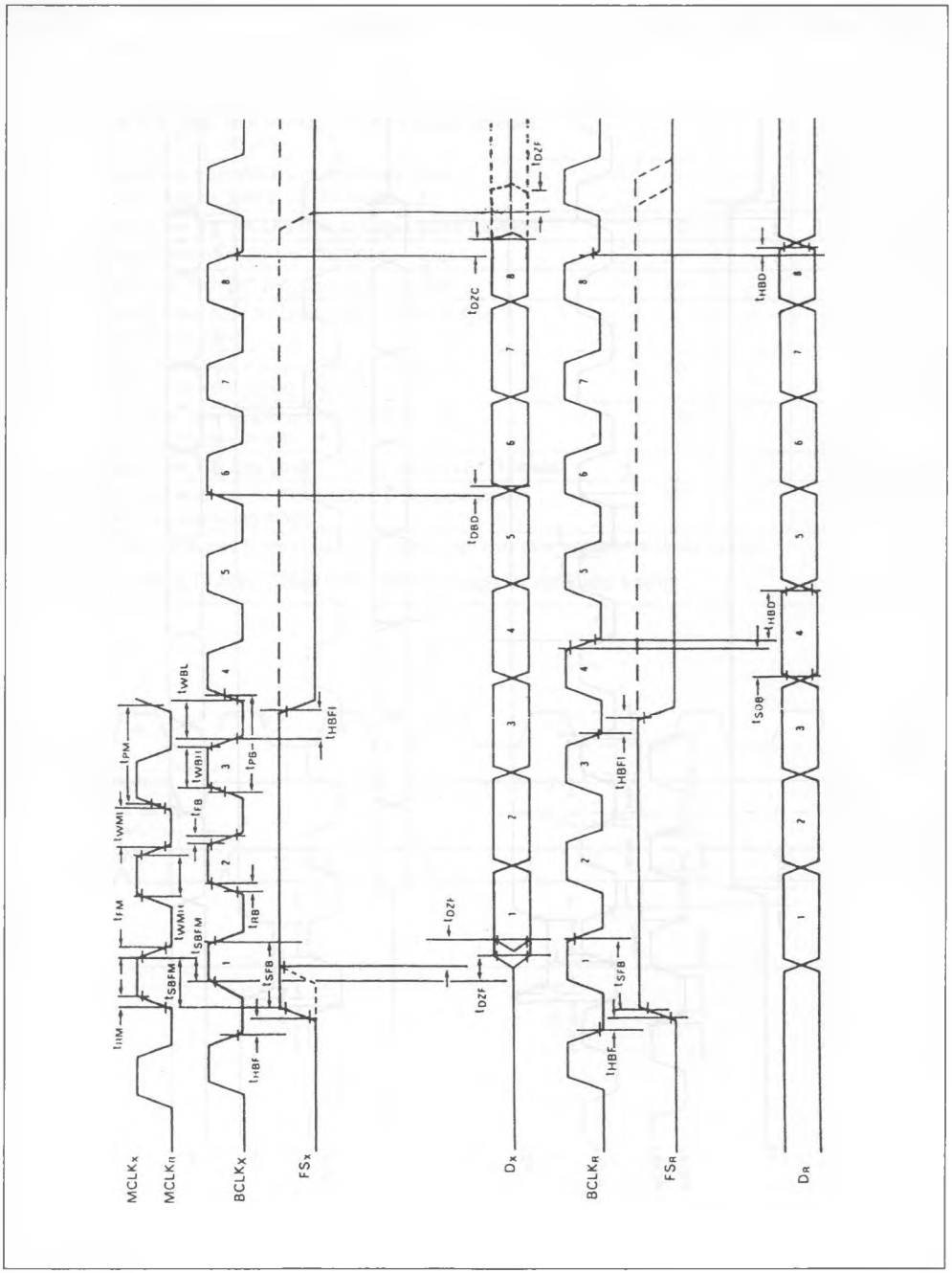


Figure 4 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS

(all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %,GNDA = 0 v, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.14 dBm0 ETC5067 3.17 dBm0 ETC5064	– –	2.492 2.501	– –	V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, measure response from O Hz to 4000 Hz	 – – – – 2.8 – 1.8 – 0.15 – 0.35 – 0.7 – –	 – – – – – – – – – –	 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1	–	0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI^+ = – 40 dBm0 to + 3 dBm0 VF_XI^+ = – 50 dBm0 to – 40 dBm0 VF_XI^+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f= 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.7 –	 – – – –	 0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1	–	0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VF_RO R_L = 10 kΩ	– 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5067, $VF_XI^+ = 0$ V)	–	– 74	– 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5067, PCM Code Equals Positive Zero)	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5064, $VFXI^+ = 0$ V)	–	12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted (ETC5064, PCM Code Equals Alternating Positive and Negative Zero)	–	8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{CC} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI^+, measure individual image signals at VF_R0				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 32	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method)					dBp
	Transmit or Receive Half-channel					
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 level for better than ± 0.1 dB linearity over the range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-).				Vrms
	R_L = 600 Ω	3.3	–	–	
	R_L = 1200 Ω	3.5	–	–	
	R_L = 30 kΩ	4.0	–	–	
S/Dp	Signal/Distortion R_L = 600 Ω, 0 dBm0	50	–	–	dB

Notes : 1. Measured by extrapolation from the distortion test result.
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

	A–Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	10101010	10000000
V_{IN} (at GS_X) = 0 V	11010101 01010101	11111111 01111111
V_{IN} (at GS_X) = – Full-scale	00101010	00000000

APPLICATIONS INFORMATION

POWER SUPPLIES

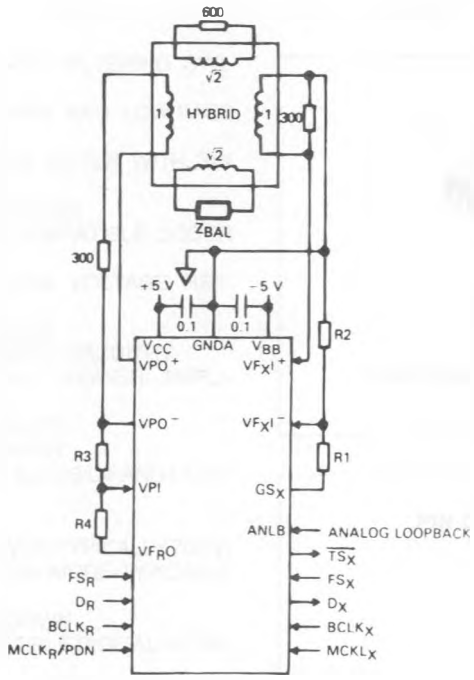
While the pins of the ETC5060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

For best performance either, $\overline{TS}$ x should be grounded if not used.

Figure 5 : Typical Asynchronous Application.



Notes : 1. Transmit Gain = 20 x log $\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) ≥ 10 kΩ.

2. Receive gain = 20 x log $\left(\frac{2 \times R3}{R4}\right)$ · R4 ≤ 10 kΩ.