

# DSP56367

## 24-Bit Audio Digital Signal Processor

The DSP56367 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56367 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Symphony™ DSP family, as shown in [Figure 1](#). This design provides a two-fold performance increase over Freescale's popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56367 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.8 V and 100 million instructions per second (MIPS) using an internal 100 MHz clock at 1.5 V.

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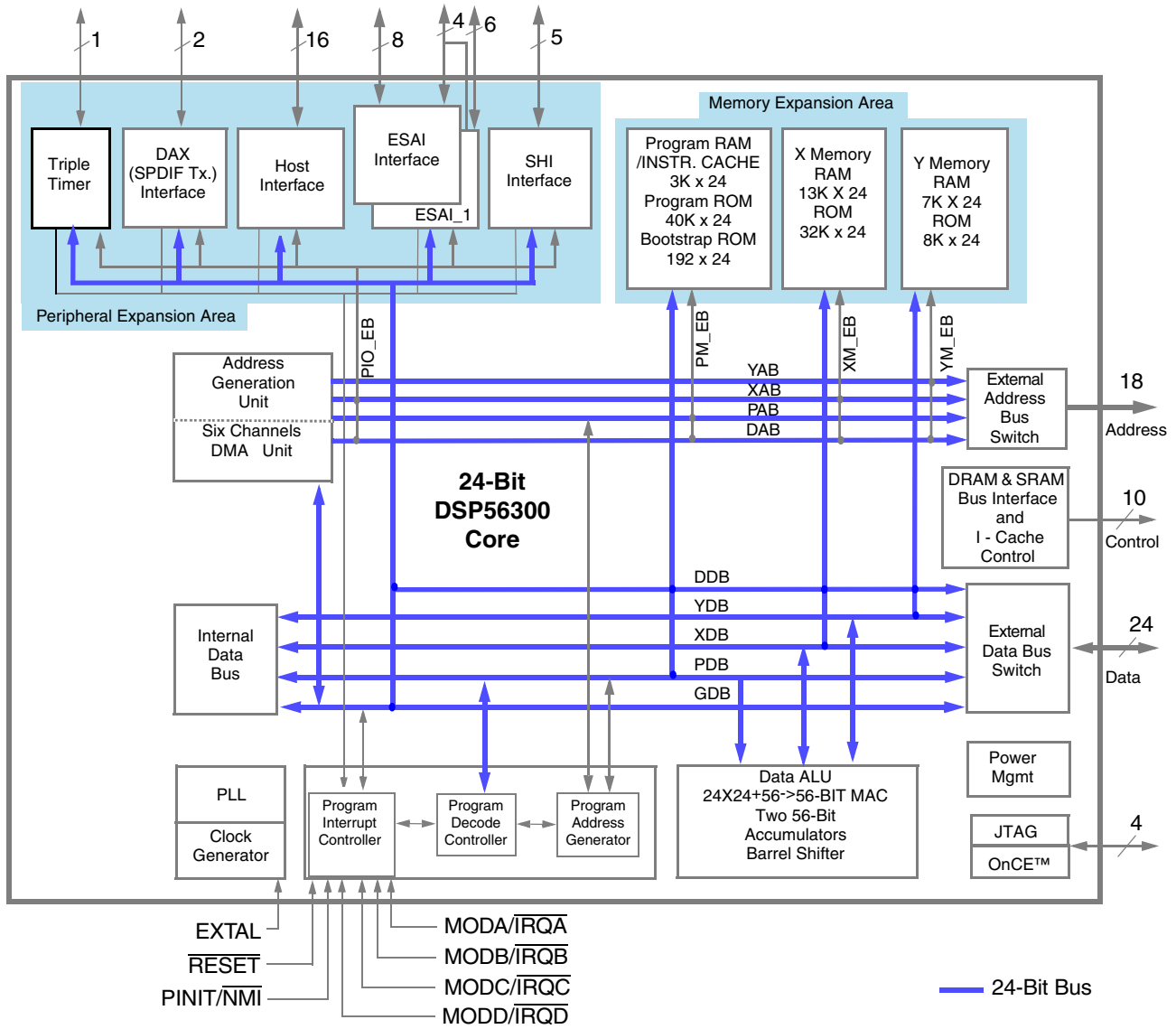


Figure 1 DSP56367 Block Diagram

## DSP56367 Features

- DSP56300 modular chassis
  - 150 Million Instructions Per Second (MIPS) with an 150 MHz clock at internal logic supply (QVCC<sub>L</sub>) of 1.8V.
  - 100 Million Instructions Per Second (MIPS) with an 100 MHz clock at internal logic supply (QVCC<sub>L</sub>) of 1.5V.
  - Object Code Compatible with the 56K core.
  - Data ALU with a 24 × 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
  - Program Control with position independent code support and instruction cache support.

- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider ( $2^i$ :  $i = 0$  to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.
- On-chip Memory Configuration
  - $7K \times 24$  Bit Y-Data RAM and  $8K \times 24$  Bit Y-Data ROM.
  - $13K \times 24$  Bit X-Data RAM and  $32K \times 24$  Bit X-Data ROM.
  - $40K \times 24$  Bit Program ROM.
  - $3K \times 24$  Bit Program RAM and  $192 \times 24$  Bit Bootstrap ROM. 1K of Program RAM may be used as Instruction Cache or for Program ROM patching.
  - $2K \times 24$  Bit from Y Data RAM and  $5K \times 24$  Bit from X Data RAM can be switched to Program RAM resulting in up to  $10K \times 24$  Bit of Program RAM.
- Off-chip memory expansion
  - External Memory Expansion Port.
  - Off-chip expansion up to two  $16M \times 24$ -bit word of Data memory.
  - Off-chip expansion up to  $16M \times 24$ -bit word of Program memory.
  - Simultaneous glueless interface to SRAM and DRAM.
- Peripheral modules
  - Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or slave. I<sup>2</sup>S, Sony, AC97, network and other programmable protocols.
  - Serial Audio Interface I(ESAI\_1): up to 4 receivers and up to 6 transmitters, master or slave. I<sup>2</sup>S, Sony, AC97, network and other programmable protocols  
The ESAI\_1 shares four of the data pins with ESAI\_0, and ESAI\_1 does NOT support HCKR and HCKT (high speed clocks)
  - Serial Host Interface (SHI): SPI and I<sup>2</sup>C protocols, multi master capability, 10-word receive FIFO, support for 8, 16 and 24-bit words.
  - Byte-wide parallel Host Interface (HDI08) with DMA support.
  - Triple Timer module.
  - Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
  - Pins of unused peripherals (except SHI) may be programmed as GPIO lines.
- Split power supply
  - QVCC and PVCC require 1.8 and 1.5 volt supply.
  - Other supply pins DVCC, QVCC, AVCC, CVCC and SVCC require 3.3 volts supply.
- 144-pin plastic LQFP package. (*Note: The AA3 pin is not bonded out in the 144-pin plastic LQFP package.*)

# Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56367 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

**Table 1-1 DSP56367 Documentation**

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56367 User Manual	Detailed description of the 56367 24-bit digital signal processor (DSP), its memory, operating modes, and peripheral modules	DSP56367UM

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