Product Brief

DSP56364

24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

The DSP56364 is a low-cost, high-performance DSP optimized for cost-sensitive consumer audio applications. The DSP56364 provides a cost-effective silicon solution for applications such as Dolby ProLogic A/V receivers, televisions, and minisystems, in addition to automotive and portable applications. The DSP56364 has sufficient MIPS resources to simultaneously support a variety of audio software algorithms such as Dolby Pro Logic, soundfield processing, 3D virtual surround, graphic/parametric equalization, and spectrum analysis.

The DSP56364 is a member of the DSP56300 Motorola Symphony™ DSP family and utilizes the single-instruction-per-clock-cycle DSP56300 core while retaining DSP56000 code compatibility. The DSP56364 contains audio-specific peripherals as shown in **Figure 1** and is offered in a 100 MHz/MIPS version at a nominal 3.3 V..

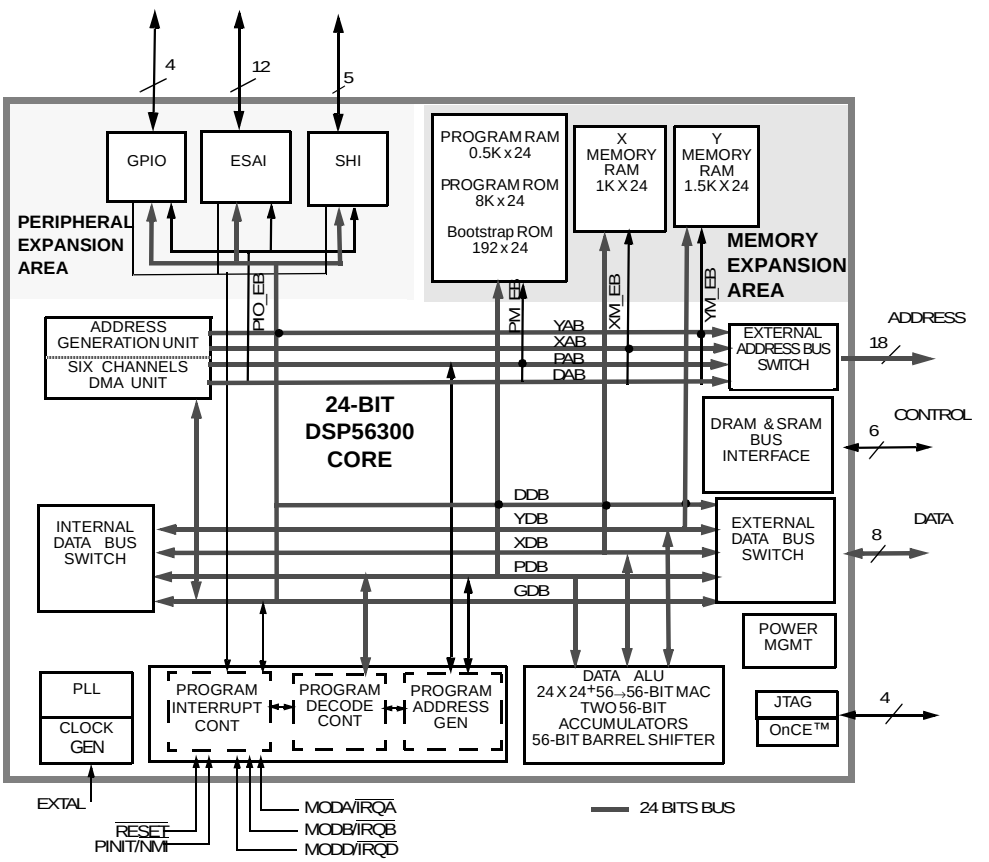

Figure 1 DSP56364 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FEATURES

- Digital Signal Processing Core
  - 100 Million Instructions Per Second (MIPS) with an 100 MHz clock at a nominal 3.3 V
  - Object code compatible with the DSP56000 core with highly parallel instruction set
  - Data Arithmetic Logic Unit (Data ALU)
  - Program Control Unit (PCU)
  - Direct Memory Access (DMA)
  - Software programmable PLL-based frequency synthesizer for the core clock
  - Hardware debugging support: On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP), and Address Trace mode
- On-Chip Memories
  - Modified Harvard architecture allows simultaneous access to program and data memories
  - Program ROMs that may be factory programmed with data/program provided by the application developer
  - 8K x 24 Bit Program ROM
  - 192 x 24-bit bootstrap ROM
  - .5K/1.25K x 24 Bit Program RAM
  - 1.5K/.75K x 24 Bit Y-Data RAM
  - 1K x 24 Bit X-Data RAM
- Off-Chip Memory Expansion
  - Memory expansion up to 2-256K x 8-bit word memory for P, X, and Y memory when using SRAM
  - Memory expansion up to 2-16M x 8-bit word memory for P, X, and Y memory when using DRAM
  - Chip Select Logic for glueless interface to SRAMs
  - On-chip DRAM Controller for glueless interface to DRAMs
- Peripheral and Support Circuits
  - Enhanced Serial Audio Interface (ESAI) includes:
    - 6 serial data lines, 4 selectable as receive or transmitt and 2 transmitt only.
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
    - Asynchronous and synchronous operation

  - Serial Host Interface (SHI) features:
    - SPI and I^2C protocols
    - Ten-word receive FIFO
    - Support for 8-, 16-, and 24-bit words.
  - On-chip peripheral registers memory mapped in data memory space
- Reduced Power Dissipation
  - Very low power (3.3 V) CMOS design
  - Wait and Stop low-power standby modes
  - Fully-static logic, operation frequency down to 0 Hz (DC)
  - Optimized power management circuitry Package

Package

- 100-pin plastic TQFP package.
- 112-pin QFP package

UMENTATION

Table 1 lists the documents that provide a complete description of the DSP56364 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information)..

Table 1 DSP56364 Chip Documentation

Topic	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set	DSP56300FM/AD
DSP56364 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56364	DSP56364UM/AD
DSP56364 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56364/D

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