Bus LVDS 3.3/5.0V Single Transceiver

Check for Samples: DS92LV010AEP

FEATURES

- **Bus LVDS Signaling (BLVDS)**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**
- **Lite Bus Loading 5pF Typical**
- **Glitch Free Power Up/Down (Driver Disabled)**
- **3.3V or 5.0V Operation**
- **±1V Common Mode Range**
- **±100mV Receiver Sensitivity**
- **High Signaling Rate Capability (above 100 Mbps)**
- **Low Power CMOS Design**
- **Product Offered in 8 Lead SOIC Package**

APPLICATIONS

- **Selected Military Applications**
- **Selected Avionics Applications**

DESCRIPTION

The DS92LV010AEP is one in a series of transceivers designed specifically for the high speed, low power proprietary bus backplane interfaces. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. To minimize bus loading the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility as 4 separate lines are provided (DIN, DE, $\overline{RE}$, and ROUT). The device also features flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10 mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 Ohms.

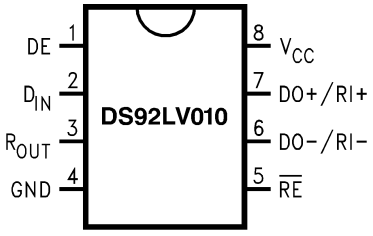
The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is ±100mV over a ±1V common mode range and translates the low voltage differential levels to standard (CMOS/TTL) levels.

ENHANCED PLASTIC

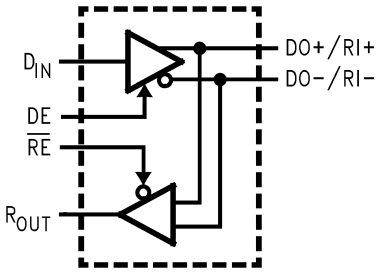
- Extended Temperature Performance of -40°C to +85°C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

Connection Diagram



See Package Number D

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_{CC})	6.0 V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3 to (V_{CC} + 0.3) V
Driver Input Voltage (DIN)	−0.3 to (V_{CC} + 0.3) V
Receiver Output Voltage (R_{OUT})	−0.3 to (V_{CC} + 0.3) V
Bus Pin Voltage (DO/RI±)	−0.3 to + 3.9 V
Driver Short Circuit Current	Continuous
ESD (HBM 1.5 kΩ, 100 pF)	>2.0 kV
Maximum Package Power Dissipation at 25°C SOIC	1025 mW
Derate SOIC Package	8.2 mW/°C
Storage Temperature Range	−65 to +150 °C
Lead Temperature (Soldering, 4 sec.)	260 °C

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.
(2) "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Supply Voltage (V_{CC})	4.5	5.5	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	−40	+85	°C

DC Electrical Characteristics[1][2][3]

T_A = −40°C to +85°C unless otherwise noted, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, Figure 1		DO+/RI+, DO−/RI−	140	250	360	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	30	mV
V_{OS}	Offset Voltage				1	1.25	1.65	V
ΔV_{OS}	Offset Magnitude Change					5	50	mV
I_{OSD}	Output Short Circuit Current	V_O = 0V, DE = V_{CC}				−12	−20	mA
V_{OH}	Voltage Output High	V_{ID} = +100 mV	I_{OH} = −400 µA	R_{OUT}	2.8	3		V
		Inputs Open			2.8	3		V
		Inputs Shorted			2.8	3		V
		Inputs Terminated, R_L = 27Ω			2.8	3		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −100 mV				0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, V_{ID} = +100 mV			−5	−35	−85	mA
V_{TH}	Input Threshold High	DE = 0V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
I_{IN}	Input Current	DE = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.
(2) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."
(3) All typicals are given for V_{CC} = +3.3V or 5.0 V and T_A = +25°C, unless otherwise stated.

DC Electrical Characteristics[1][2][3] (continued)

T_A = −40°C to +85°C unless otherwise noted, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{IH}	Minimum Input High Voltage		DIN, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA		−1.5	−0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC} , R_L = 27Ω	V_{CC}		13	20	mA
I_{CCR}		DE = $\overline{RE}$ = 0V			5	8	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}			3	7.5	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V, R_L = 27Ω			16	22	mA
C_{output}	Capacitance @ BUS Pins		DO+/RI+, DO−/RI−		5		pF

DC Electrical Characteristics[1][2][3]

T_A = −40°C to +85°C unless otherwise noted, V_{CC} = 5.0V ± 0.5V

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, Figure 1		DO+/RI+, DO−/RI−	145	270	390	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	30	mV
V_{OS}	Offset Voltage				1	1.35	1.65	V
ΔV_{OS}	Offset Magnitude Change					5	50	mV
I_{OSD}	Output Short Circuit Current	V_O = 0V, DE = V_{CC}				−12	−20	mA
V_{OH}	Voltage Output High	V_{ID} = +100 mV	I_{OH} = −400 µA	R_{OUT}	4.3	5.0		V
		Inputs Open			4.3	5.0		V
		Inputs Shorted			4.3	5.0		V
		Inputs Terminated, R_L = 27Ω			4.3	5.0		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −100 mV				0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, V_{ID} = +100 mV			−35	−90	−130	mA
V_{TH}	Input Threshold High	DE = 0V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
I_{IN}	Input Current	DE = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			DIN, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V				±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V				±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC}, R_L = 27Ω		V_{CC}		17	25	mA
I_{CCR}		DE = $\overline{RE}$ = 0V				6	10	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}				3	8	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V, R_L = 27Ω				20	25	mA
C_{output}	Capacitance @ BUS Pins			DO+/RI+, DO−/RI−		5		pF

(1) All typicals are given for V_{CC} = +3.3V or 5.0 V and T_A = +25°C, unless otherwise stated.
(2) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."
(3) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.

AC Electrical Characteristics[1][2]

T_A = −40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	R_L = 27Ω, Figure 2, Figure 3 C_L = 10 pF	1.0	3.0	5.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		1.0	2.8	5.0	ns
t_{SKD}	Differential SKEW $\|t_{PHLD} - t_{PLHD}\|$			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, Figure 4, Figure 5 C_L = 10 pF	0.5	4.5	9.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.5	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	Figure 6, Figure 7 C_L = 10 pF	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	5.5	10.0	ns
t_{SKD}	Differential SKEW $\|t_{PHLD} - t_{PLHD}\|$			0.5	2.0	ns
t_r	Rise Time			1.5	4.0	ns
t_f	Fall Time			1.5	4.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, Figure 8, Figure 9 C_L = 10 pF See[3]	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	5.0	7.0	ns
t_{PZH}	Enable Time Z to High		2.0	7.0	13.0	ns
t_{PZL}	Enable Time Z to Low		2.0	6.0	10.0	ns

(1) Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, tr, tf ≤ 6.0ns (0%–100%) on control pins and ≤ 1.0ns for RI inputs.

(2) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

(3) For receiver TRI-STATE delays, the switch is set to V_{CC} for t_{PZL}, and t_{PLZ} and to GND for t_{PZH}, and t_{PHZ}.

AC Electrical Characteristics[1][2]

T_A = −40°C to +85°C, V_{CC} = 5.0V ± 0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	R_L = 27Ω, Figure 2, Figure 3 C_L = 10 pF	0.5	2.7	4.5	ns
t_{PLHD}	Differential Prop. Delay Low to High		0.5	2.5	4.5	ns
t_{SKD}	Differential SKEW $\|t_{PHLD} - t_{PLHD}\|$			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, Figure 4, Figure 5 C_L = 10 pF	0.5	3.0	7.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	4.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.0	9.0	ns

(1) Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, tr, tf ≤ 6.0ns (0%–100%) on control pins and ≤ 1.0ns for RI inputs.

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AC Electrical Characteristics[1][2] (continued)

T_A = −40°C to +85°C, V_{CC} = 5.0V ± 0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	Figure 6, Figure 7 C_L = 10 pF	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	4.6	10.0	ns
t_{SKD}	Differential SKEW $\|t_{PHLD} - t_{PLHD}\|$			0.4	2.0	ns
t_r	Rise Time			1.2	2.5	ns
t_f	Fall Time			1.2	2.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, Figure 8, Figure 9 C_L = 10 pF See[3]	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	4.0	6.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	9.0	ns
t_{PZL}	Enable Time Z to Low		2.0	5.0	7.0	ns

(3) For receiver TRI-STATE delays, the switch is set to V_{CC} for t_{PZL}, and t_{PLZ} and to GND for t_{PZH}, and t_{PHZ}.

Test Circuits and Timing Waveforms

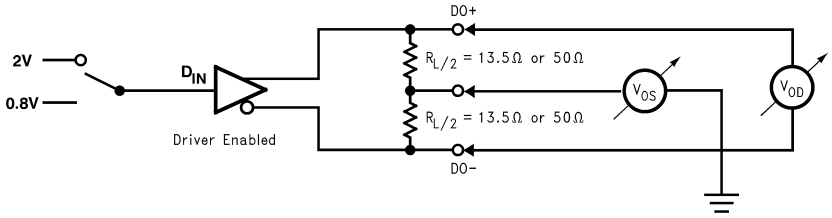

Figure 1. Differential Driver DC Test Circuit

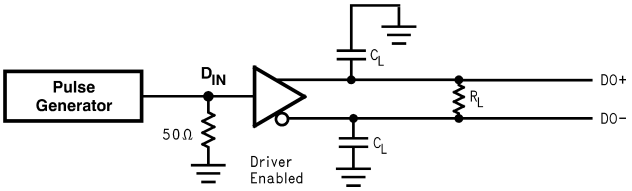

Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

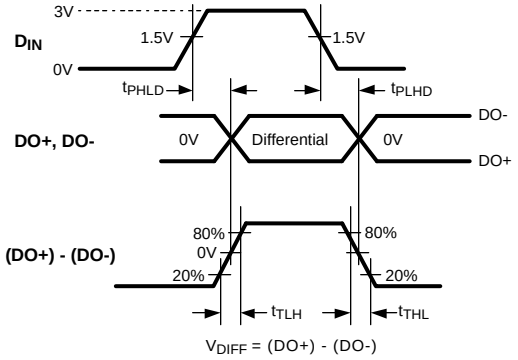

Figure 3. Differential Driver Propagation Delay and Transition Time Waveforms

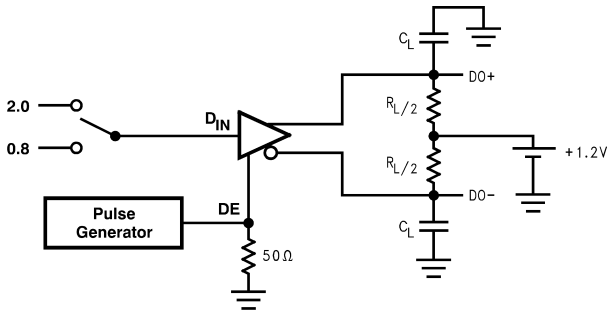

Figure 4. Driver TRI-STATE Delay Test Circuit

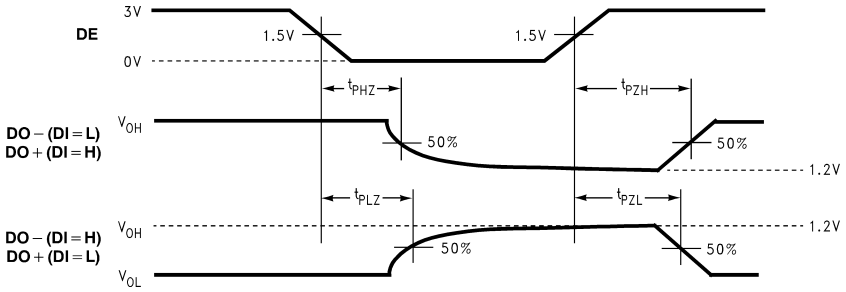

Figure 5. Driver TRI-STATE Delay Waveforms

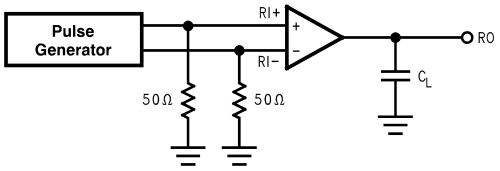

Figure 6. Receiver Propagation Delay and Transition Time Test Circuit

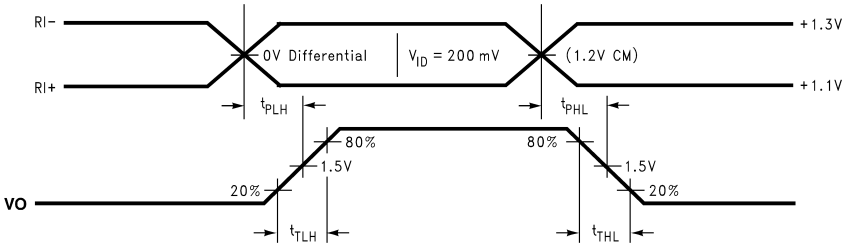

Figure 7. Receiver Propagation Delay and Transition Time Waveforms

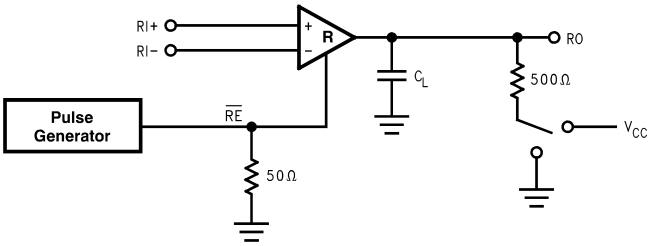

Figure 8. Receiver TRI-STATE Delay Test Circuit

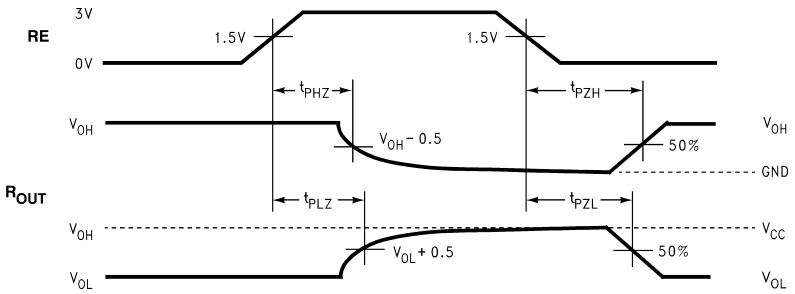

Figure 9. Receiver TRI-STATE Delay Waveforms TRI-STATE Delay Waveforms

TYPICAL BUS APPLICATION CONFIGURATIONS

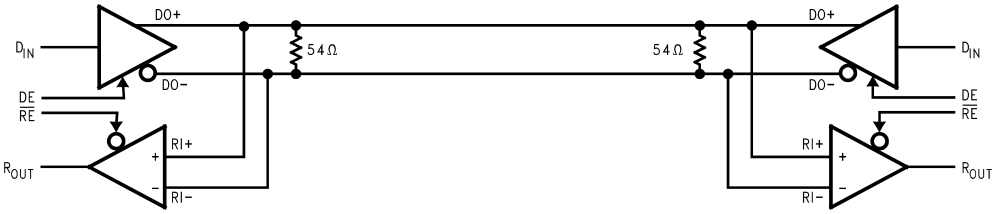

Figure 10. Bi-Directional Half-Duplex Point-to-Point Applications

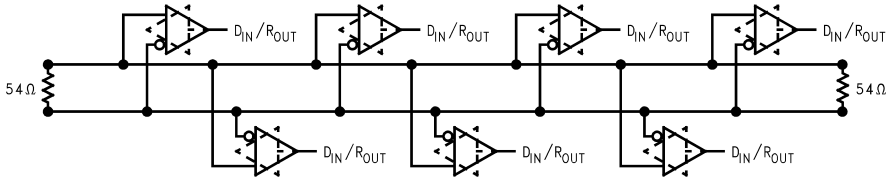

Figure 11. Multi-Point Bus Applications

APPLICATION INFORMATION

There are a few common practices which should be implied when designing PCB for BLVDS signaling. Recommended practices are:

- Use at least 4 layer PCB board (BLVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (BLVDS port side) connector as possible.
- Bypass each BLVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1 µF, and 0.01 µF in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused LVDS receiver inputs open (floating)

Table 1. Functional Table(1)

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

(1) L = Low state, H = High state

Table 2. Transmitter Mode(1)

INPUTS		OUTPUTS	
DE	DI	DO+	DO−
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z

(1) X = High or Low logic state, Z = High impedance state
L = Low state, H = High state

Table 3. Receiver Mode(1)

INPUTS		OUTPUT
$\overline{RE}$	(RI+)-(RI−)	
L	L (< −100 mV)	L
L	H (> +100 mV)	H
L	100 mV > & > −100 mV	X
H	X	Z

(1) X = High or Low logic state, Z = High impedance state
L = Low state, H = High state

Table 4. DEVICE PIN DESCRIPTION

Pin Name	Pin #	Input/Output	Description
DIN	2	I	TTL Driver Input
DO±/RI±	6, 7	I/O	LVDS Driver Outputs/LVDS Receiver Inputs
R_{OUT}	3	O	TTL Receiver Output
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V_{CC}	8	NA	Power Supply

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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