National Semiconductor

ADVANCE INFORMATION

DS90LV032
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 100 Mbps (50 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032 accepts low voltage (350 mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100Ω) input Failsafe. Receiver output will be High for all failsafe conditions.

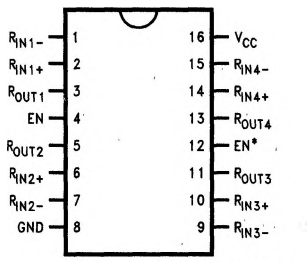
The DS90LV032 and companion line driver (DS90LV031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interface applications.

Features

- 3.3V power supply design
- > 100 Mbps (50 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- Ultra low power dissipation
- TBD ps maximum differential skew (3.3V, 25°C)
- TBD ns maximum propagation delay
- Industrial operating temperature range (−40°C to +85°C)
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C32A, MB570 (PECL), 41LF (PECL), and DS90C032
- Supports OPEN, short and terminated input failsafe
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard

Connection Diagram

Dual-In-Line



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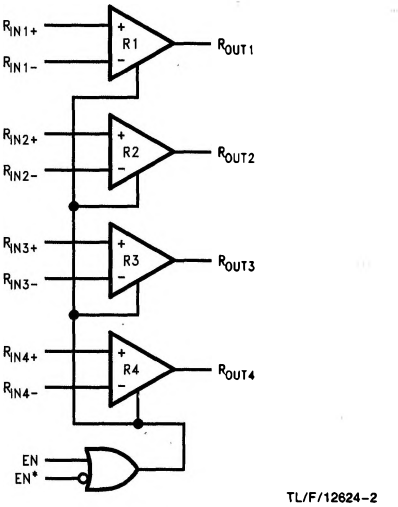
Order Number
DS90LV032TM
See NS Package Number M16A

Functional Diagram and Truth Tables



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RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Failsafe OPEN/SHORT or Terminated	H