

DS90CR563/DS90CR564 LVDS 18-Bit Color Flat Panel Display (FPD) Link—65 MHz

General Description

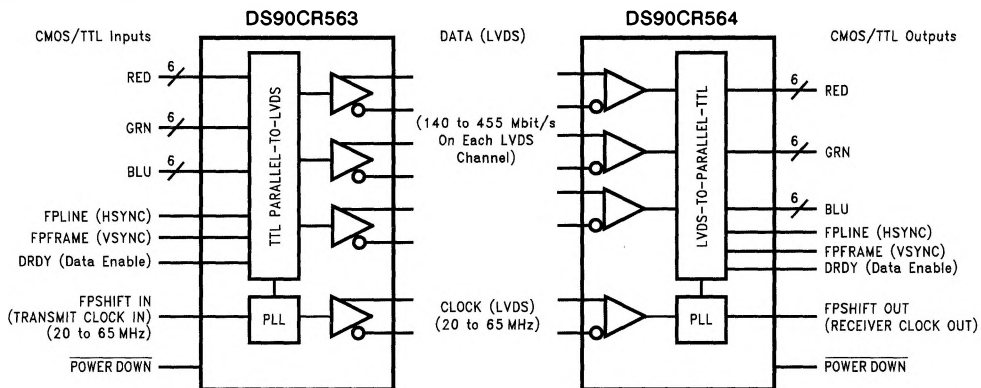
The DS90CR563 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR564 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 171 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 171 Mbytes/s bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

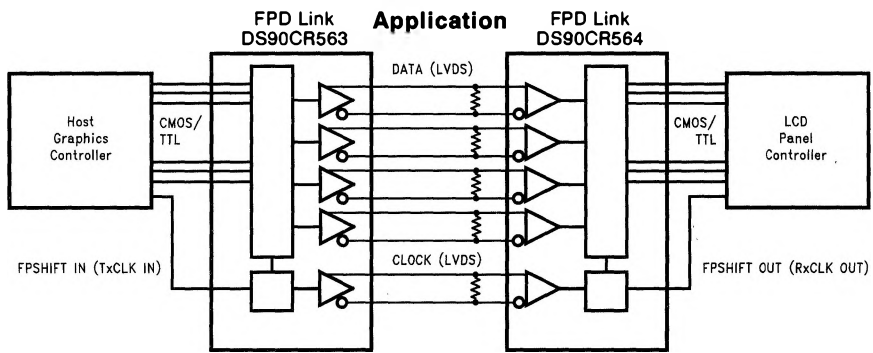
Block Diagrams



TL/F/12617-1

Order Number DS90CR563MTD
See NS Package Number MTD48

Order Number DS90CR564MTD
See NS Package Number MTD48



TL/F/12617-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.3V to +6V
CMOS/TTL Input Voltage	-0.3V to ($V_{CC} + 0.3V$)
CMOS/TTL Output Voltage	-0.3V to ($V_{CC} + 0.3V$)
LVDS Receiver Input Voltage	-0.3V to ($V_{CC} + 0.3V$)
LVDS Driver Output Voltage	-0.3V to ($V_{CC} + 0.3V$)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C

Maximum Power Dissipation @ 25°C

MTD48 (TSSOP) Package:

DS90CR563 TBD W

DS90CR564 TBD W

Package Derating:

DS90CR563 TBD W/°C above +25°C

DS90CR564 TBD W/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	-10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V	
V_{IL}	Low Level Input Voltage		GND		0.8	V	
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4$ mA	3.8	4.9		V	
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA		0.1	0.3	V	
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V	
I_{IN}	Input Current	$V_{IN} = V_{CC}, GND, 2.5V$ or 0.4V		±5.1	±10	μA	
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$			-120	mA	
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV	
ΔV_{OD}	Change in V_{OD} between Complementary Output States				35	mV	
V_{CM}	Common Mode Voltage		1.1	1.25	1.375	V	
ΔV_{CM}	Change in V_{CM} between Complementary Output States				35	mV	
V_{OH}	High Level Output Voltage				1.3	V	
V_{OL}	Low Level Output Voltage		0.9	1.07		V	
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$		-2.9	-5	mA	
I_{OZ}	Output TRI-STATE® Current	Power Down = 0V, $V_{OUT} = 0V$ or V_{CC}		±1	±10	μA	
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV	
V_{TL}	Differential Input Low Threshold			-100		mV	
I_{IN}	Input Current	$V_{IN} = +2.4V$	$V_{CC} = 5.5V$			±10	μA
		$V_{IN} = 0V$				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 5.0V$ and $T_A = +25^\circ C$.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD rating: HBM (1.5 kΩ, 100 pF)

PLL $V_{CC} \geq 1000V$

All other pins $\geq 2000V$

EIAJ (0Ω, 200 pF) $\geq 150V$

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
TRANSMITTER SUPPLY CURRENT							
I _{CC} TW	Transmitter Supply Current, Worst Case	R _L = 100Ω, C _L = 5 pF, Worst Case Pattern (Figures 1, 3)	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
			f = 65 MHz		TBD	TBD	mA
I _{CC} TG	Transmitter Supply Current, 16 Grayscale	R _L = 100Ω, C _L = 5 pF, 16 Grayscale Pattern (Figures 2, 3)	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
			f = 65 MHz		TBD	TBD	mA
I _{CC} TZ	Transmitter Supply Current, Power Down	Power Down = Low		1	10	μA	

RECEIVER SUPPLY CURRENT

I _{CC} RW	Receiver Supply Current, Worst Case	C _L = 8 pF, Worst Case Pattern (Figures 1, 4)	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
			f = 65 MHz		TBD	TBD	mA
I _{CC} RG	Receiver Supply Current, 16 Grayscale	C _L = 8 pF, 16 Grayscale Pattern (Figures 2, 4)	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
			f = 65 MHz		TBD	TBD	mA
I _{CC} RZ	Receiver Supply Current, Power Down	Power Down = Low		1	10	μA	

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
LLHT	LVDS Low-to-High Transition Time (Figure 3)		0.75	1.5	ns	
LHLT	LVDS High-to-Low Transition Time (Figure 3)		0.75	1.5	ns	
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4)		3.5	6.5	ns	
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4)		2.7	6.5	ns	
TCIT	TxCLK IN Transition Time (Figure 5)			8	ns	
TCCS	TxOUT Channel-to-Channel Skew (Note A) (Figure 6)			350	ps	
TSSPW	TxSub-Symbol Pulse Width (Figure 6)	f = 65 MHz	1.7	2.1	2.5	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)			700	ps	
TCIP	TxCLK IN Period (Figure 7)	15	T	50	ns	
TCIH	TxCLK IN High Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 7)	f = 65 MHz	TBD		ns	

Note A: This limit based on bench characterization.**Note B:** This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
THTC	TxIN Hold to TxCLK IN (Figure 7)		2.5	2		ns
RCOP	RxCLK OUT Period (Figure 8)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 8)	f = 65 MHz	TBD			ns
RCOL	RxCLK OUT Low Time (Figure 8)	f = 65 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 8)	f = 65 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 8)	f = 65 MHz	TBD			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V _{CC} = 5.0V (Figure 9)		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V _{CC} = 5.0V (Figure 10)		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 11)				10	ms
RPLLS	Receiver Phase Lock Loop Set (Figure 12)				10	ms

AC Timing Diagrams

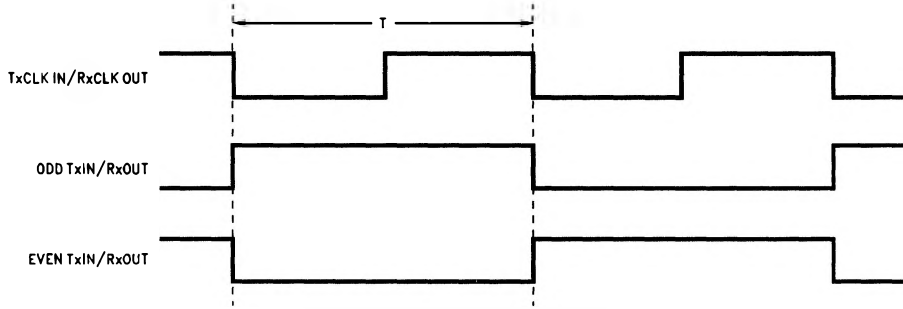


FIGURE 1. "Worst Case" Test Pattern

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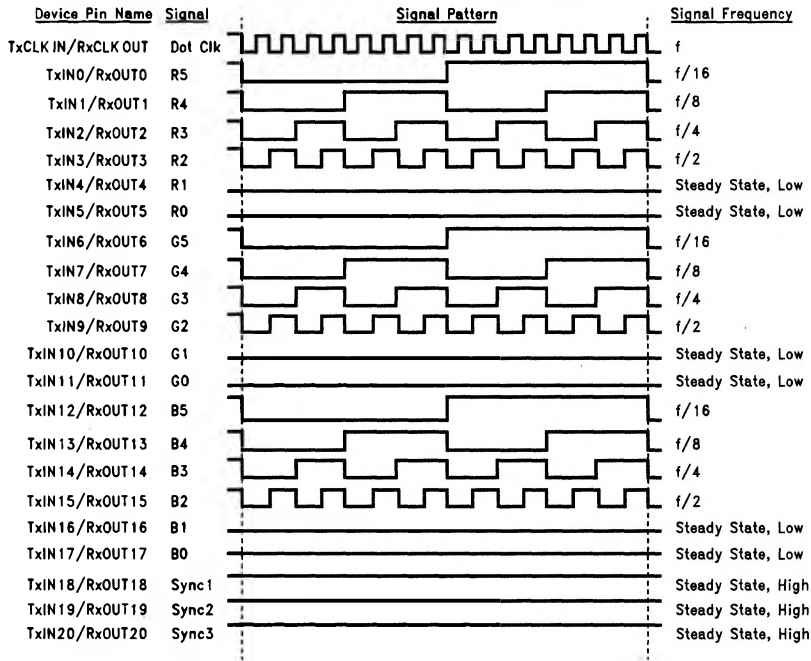


FIGURE 2. "16 Grayscale" Test Pattern

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Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: Figure 1 and Figure 2 show a rising edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

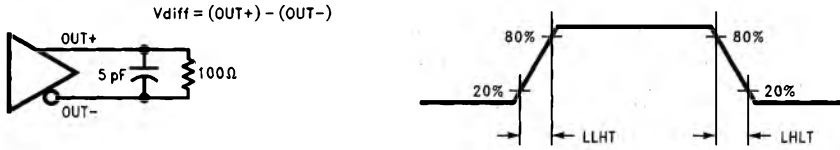


FIGURE 3. DS90CR563 (Transmitter) LVDS Output Load and Transition Times

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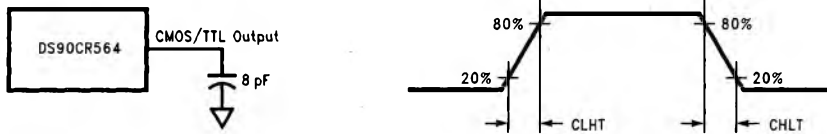


FIGURE 4. DS90CR564 (Receiver) CMOS/TTL Output Load and Transition Times

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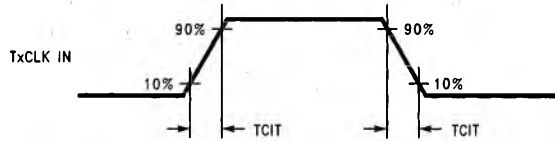
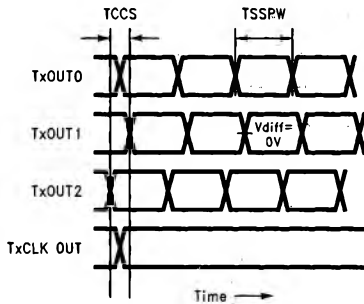


FIGURE 5. DS90CR563 (Transmitter) Input Clock Transition Time

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- Note 1: Measurements at $V_{diff} = 0V$
- Note 2: TCSS measured between earliest and latest LVDS edges.
- Note 3: TxCLK Differential Low \rightarrow High Edge

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FIGURE 6. DS90CR563 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

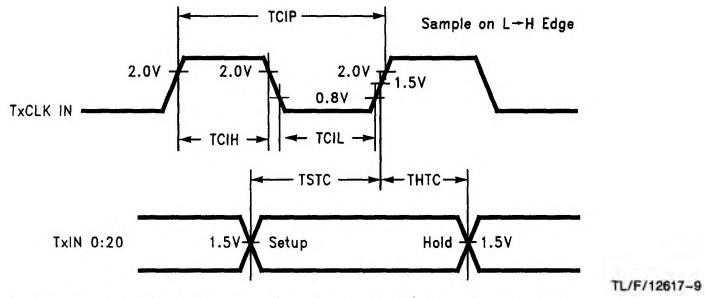


FIGURE 7. DS90CR563 (Transmitter) Setup/Hold and High/Low Times

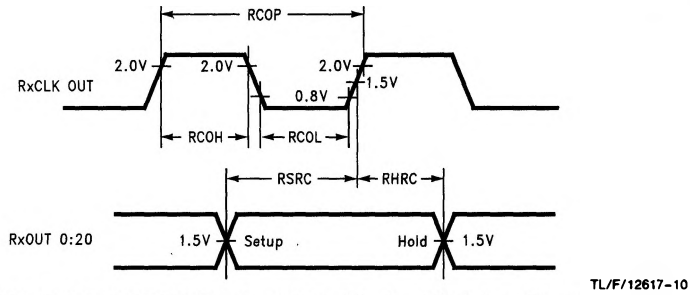


FIGURE 8. DS90CR564 (Receiver) Setup/Hold and High/Low Times

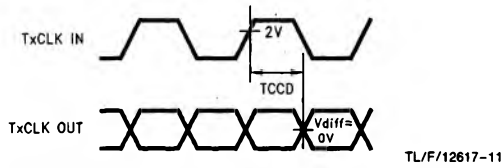


FIGURE 9. DS90CR563 (Transmitter) Clock In to Clock Out Delay

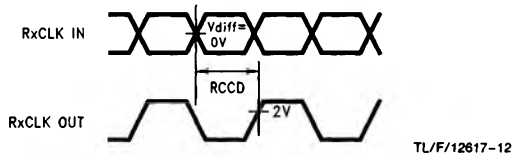


FIGURE 10. DS90CR564 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

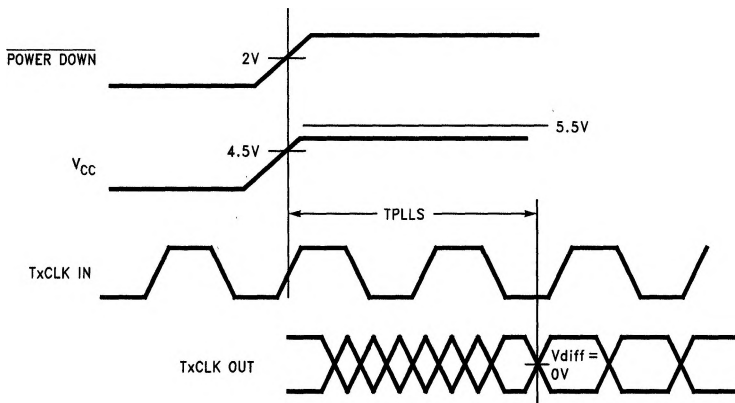


FIGURE 11. DS90CR563 (Transmitter) Phase Lock Loop Set Time

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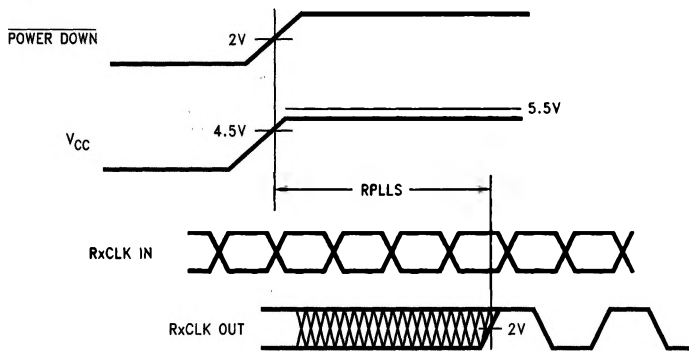


FIGURE 12. DS90CR564 (Receiver) Phase Lock Loop Set Time

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AC Timing Diagrams (Continued)

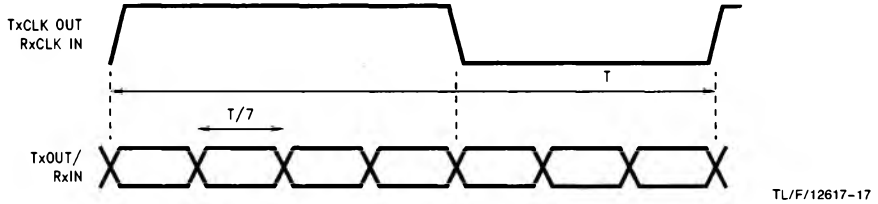


FIGURE 13. Seven Bits of LVDS in One Clock Cycle

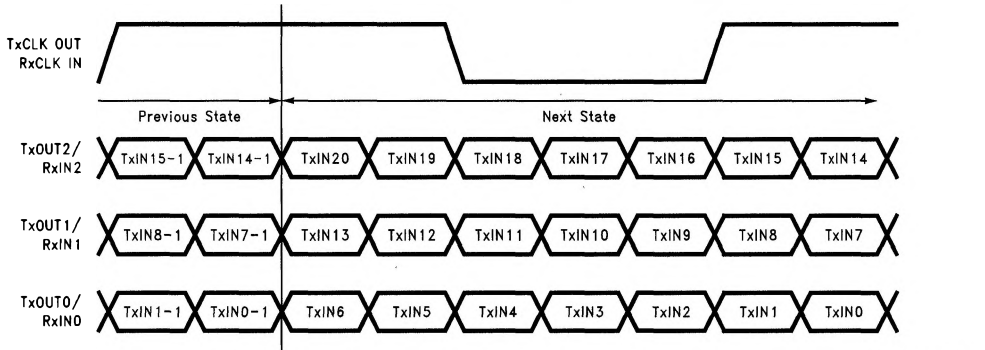


FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS (DS90CR563)

DS90CR563 Pin Descriptions—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY) (also referred to as HSYNC, VSYNC, Data Enable)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT-	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
PWR DOWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V _{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V _{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V _{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR564 Pin Descriptions—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN-	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY) (also referred to as HSYNC, VSYNC, Data Enable)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN-	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The rising edge acts as data strobe
PWR DOWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V _{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V _{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V _{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

Connection Diagrams

DS90CR563

TxIN4	1	48	TxIN3
V _{CC}	2	47	TxIN2
TxIN5	3	46	GND
TxIN6	4	45	TxIN1
GND	5	44	TxIN0
TxIN7	6	43	N/C
TxIN8	7	42	LVDS GND
V _{CC}	8	41	TxOUT0-
TxIN9	9	40	TxOUT0+
TxIN10	10	39	TxOUT1-
GND	11	38	TxOUT1+
TxIN11	12	37	LVDS V _{CC}
TxIN12	13	36	LVDS GND
V _{CC}	14	35	TxOUT2-
TxIN13	15	34	TxOUT2+
TxIN14	16	33	TxCLK OUT-
GND	17	32	TxCLK OUT+
TxIN15	18	31	LVDS GND
TxIN16	19	30	PLL GND
TxIN17	20	29	PLL V _{CC}
V _{CC}	21	28	PLL GND
TxIN18	22	27	PWR DWN
TxIN19	23	26	TxCLK IN
GND	24	25	TxIN20

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DS90CR564

RxOUT17	1	48	V _{CC}
RxOUT18	2	47	RxOUT16
GND	3	46	RxOUT15
RxOUT19	4	45	RxOUT14
RxOUT20	5	44	GND
N/C	6	43	RxOUT13
LVDS GND	7	42	V _{CC}
RxIN0-	8	41	RxOUT12
RxIN0+	9	40	RxOUT11
RxIN1-	10	39	RxOUT10
RxIN1+	11	38	GND
LVDS V _{CC}	12	37	RxOUT9
LVDS GND	13	36	V _{CC}
RxIN2-	14	35	RxOUT8
RxIN2+	15	34	RxOUT7
RxCLK IN-	16	33	RxOUT6
RxCLK IN+	17	32	GND
LVDS GND	18	31	RxOUT5
PLL GND	19	30	RxOUT4
PLL V _{CC}	20	29	RxOUT3
PLL GND	21	28	V _{CC}
PWR DWN	22	27	RxOUT2
RxCLK OUT	23	26	RxOUT1
RxOUT0	24	25	GND

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