

DS90CR218A +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link - 12 MHz to 85 MHz

Check for Samples: [DS90CR218A](#)

FEATURES

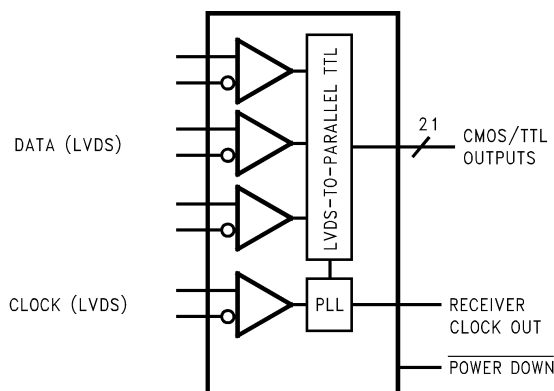
- 12 to 85 MHz Shift Clock Support
- 50% Duty Cycle on Receiver Output Clock
- Low Power Consumption
- $\pm 1\text{V}$ Common-mode Range (Around +1.2V)
- Narrow Bus Reduces Cable Size and Cost
- Up to 1.785 Gbps Throughput
- Up to 223 Mbytes/sec Bandwidth
- 345 mV (typ) Swing LVDS Devices for Low EMI
- PLL Requires No External Components
- Rising Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 48-Lead TSSOP Package

DESCRIPTION

The DS90CR218A receiver deserializes three input LVDS data streams into 21 bits of CMOS/TTL output data. When operating at the maximum input clock rate of 85 MHz, the LVDS data is received at 595 Mbps per data channel for a total data throughput of 1.785 Gbit/sec (233 Mbytes/sec).

The narrow bus and LVDS signalling of the DS90CR218A is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Block Diagram



**Figure 1. DS90CR218A Top View
See Package Number DGG-48 (TSSOP)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Connection Diagrams

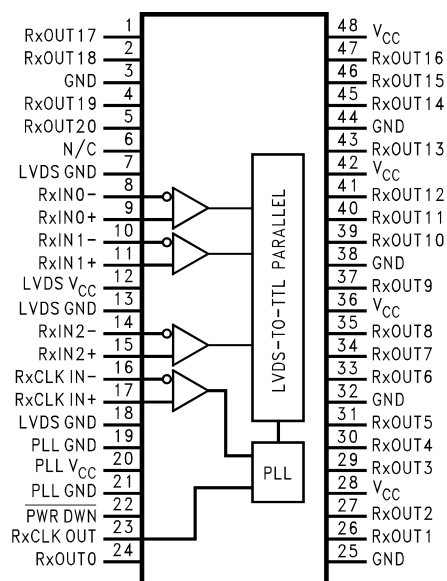


Figure 2. DS90CR218A

Typical Application

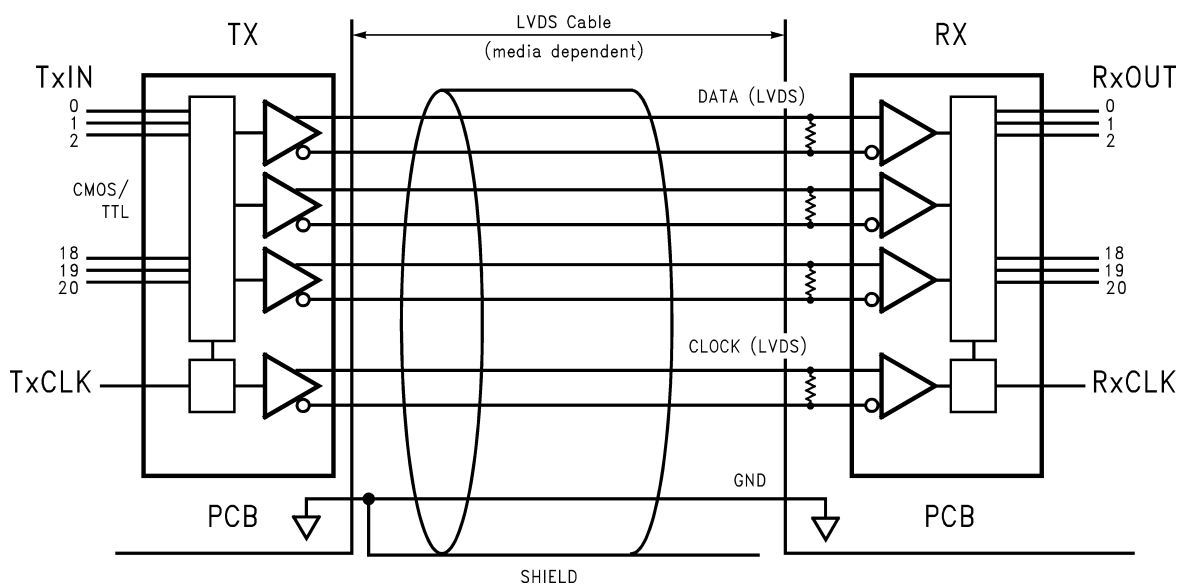


Figure 3. Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | |
|---|---------------------|------------------------------|
| Supply Voltage (V_{CC}) | | –0.3V to +4V |
| CMOS/TTL Input Voltage | | –0.5V to ($V_{CC} + 0.3V$) |
| CMOS/TTL Output Voltage | | –0.3V to ($V_{CC} + 0.3V$) |
| LVDS Receiver Input Voltage | | –0.3V to ($V_{CC} + 0.3V$) |
| Junction Temperature | | +150°C |
| Storage Temperature Range | | –65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | | +260°C |
| Maximum Package Power Dissipation @ +25°C TSSOP Package | DS90CR218A | 1.89 W |
| Package Derating | | 15 mW/°C above +25°C |
| ESD Rating | (HBM, 1.5kΩ, 100pF) | > 7kV |
| | (EIAJ, 0Ω, 200pF) | > 700V |
| Latch Up Tolerance @ 25°C | | > ±300mA |

- (1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|--|-----|-----|-----|------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | –10 | +25 | +70 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage (V_{CC}) | | | 100 | mV _{PP} |

Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|---------------------------------|---|---|------------|-------|-----------------|-------|----|
| CMOS/TTL DC SPECIFICATIONS | | | | | | | |
| V _{IH} | High Level Input Voltage | | 2.0 | | V _{CC} | V | |
| V _{IL} | Low Level Input Voltage | | GND | | 0.8 | V | |
| V _{OH} | High Level Output Voltage | I _{OH} = -0.4 mA | 2.7 | 3.3 | | V | |
| V _{OL} | Low Level Output Voltage | I _{OL} = 2 mA | | 0.06 | 0.3 | V | |
| V _{CL} | Input Clamp Voltage | I _{CL} = -18 mA | | -0.79 | -1.5 | V | |
| I _{IN} | Input Current | V _{IN} = 0.4V, 2.5V or V _{CC} | | +1.8 | +15 | μA | |
| | | V _{IN} = GND | -10 | 0 | | μA | |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V | | -60 | -120 | mA | |
| LVDS RECEIVER DC SPECIFICATIONS | | | | | | | |
| V _{TH} | Differential Input High Threshold | V _{CM} = +1.2V | | | +100 | mV | |
| V _{TL} | Differential Input Low Threshold | | -100 | | | mV | |
| I _{IN} | Input Current | V _{IN} = +2.4V, V _{CC} = 3.6V | | | ±10 | μA | |
| | | V _{IN} = 0V, V _{CC} = 3.6V | | | ±10 | μA | |
| RECEIVER SUPPLY CURRENT | | | | | | | |
| I _{CCRW} | Receiver Supply Current ⁽²⁾ Worst Case | C _L = 8 pF, Worst Case Pattern Figure 4 Figure 5 | f = 33 MHz | | 49 | 60 | mA |
| | | | f = 40 MHz | | 53 | 65 | mA |
| | | | f = 66 MHz | | 78 | 100 | mA |
| | | | f = 85 MHz | | 90 | 115 | mA |

(1) Typical values are given for $V_{CC} = 3.3V$ and $T_A = +25°C$.

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Electrical Characteristics⁽¹⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|---|---|-----|-----|-----|-------|
| I _{CCRZ} | Receiver Supply Current ⁽²⁾ Power Down | PWR DWN = Low Receiver Outputs Stay Low during Powerdown Mode | | 140 | 400 | μA |

Receiver Switching Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | | Min | Typ | Max | Units |
|--------|--|------------|-------|-------|-------|-------|
| CLHT | CMOS/TTL Low-to-High Transition Time Figure 5 | | | 2.0 | 3.5 | ns |
| CHLT | CMOS/TTL High-to-Low Transition Time Figure 5 | | | 1.8 | 3.5 | ns |
| RSPos0 | Receiver Input Strobe Position for Bit 0 Figure 11 | f = 85 MHz | 0.49 | 0.84 | 1.19 | ns |
| RSPos1 | Receiver Input Strobe Position for Bit 1 | | 2.17 | 2.52 | 2.87 | ns |
| RSPos2 | Receiver Input Strobe Position for Bit 2 | | 3.85 | 4.20 | 4.55 | ns |
| RSPos3 | Receiver Input Strobe Position for Bit 3 | | 5.53 | 5.88 | 6.23 | ns |
| RSPos4 | Receiver Input Strobe Position for Bit 4 | | 7.21 | 7.56 | 7.91 | ns |
| RSPos5 | Receiver Input Strobe Position for Bit 5 | | 8.89 | 9.24 | 9.59 | ns |
| RSPos6 | Receiver Input Strobe Position for Bit 6 | | 10.57 | 10.92 | 11.27 | ns |
| RSKM | RxIN Skew Margin ⁽²⁾ Figure 12 | f = 85 MHz | | 0.49 | | ns |
| | | f = 12MHz | | 2.01 | | ns |
| RCOP | RxCLK OUT Period Figure 6 | | 11.76 | T | 83.33 | ns |
| RCOH | RxCLK OUT High Time Figure 6 | f = 85 MHz | 4 | 5 | 6.5 | ns |
| RCOL | RxCLK OUT Low Time Figure 6 | | 3.5 | 5 | 6 | ns |
| RSRC | RxOUT Setup to RxCLK OUT Figure 6 | | 3.5 | | | ns |
| RHRC | RxOUT Hold to RxCLK OUT Figure 6 | | 3.5 | | | ns |
| RCCD | RxCLK IN to RxCLK OUT Delay @ 25°C, V _{CC} = 3.3V ⁽³⁾ Figure 7 | | 5.5 | 7 | 9.5 | ns |
| RPLLS | Receiver Phase Lock Loop Set Figure 8 | | | | 10 | ms |
| RPDD | Receiver Powerdown Delay Figure 10 | | | | 1 | μs |

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the receiver input setup and hold time (internal data sampling window). This margin do not take into account the Transmitter Pulse Position (TPPOS) variance and is measured using the ideal TPPOS. This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), Transmitter Pulse Position (TPPOS) variance, and source clock jitter less than 250 ps.

(3) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 217/287 transmitter and 218A/288A receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period.

AC Timing Diagrams

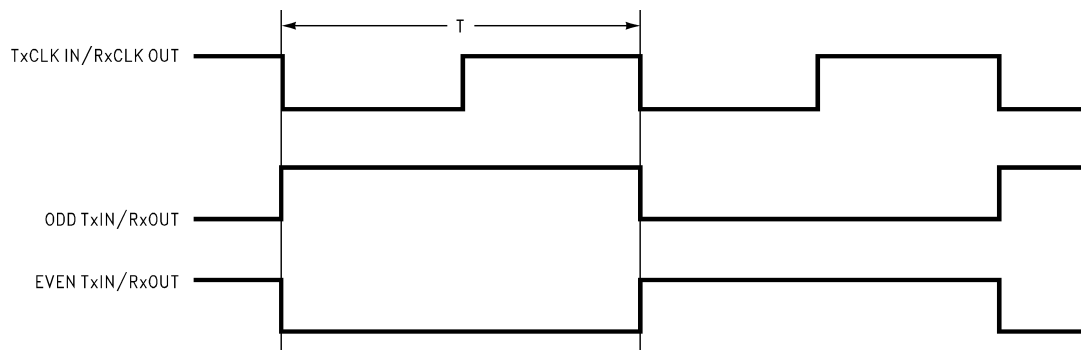


Figure 4. "Worst Case" Test Pattern

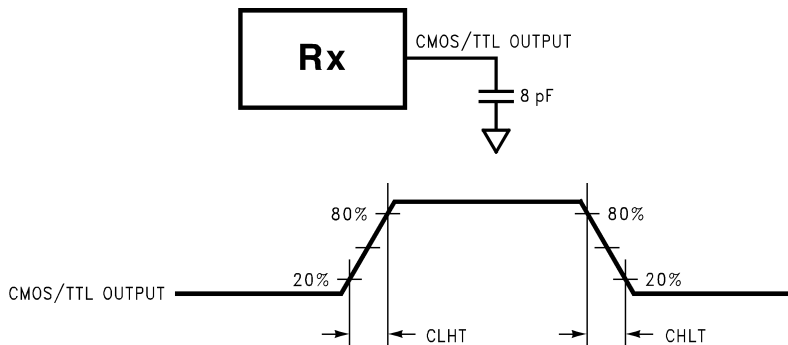


Figure 5. DS90CR218A (Receiver) CMOS/TTL Output Load and Transition Times

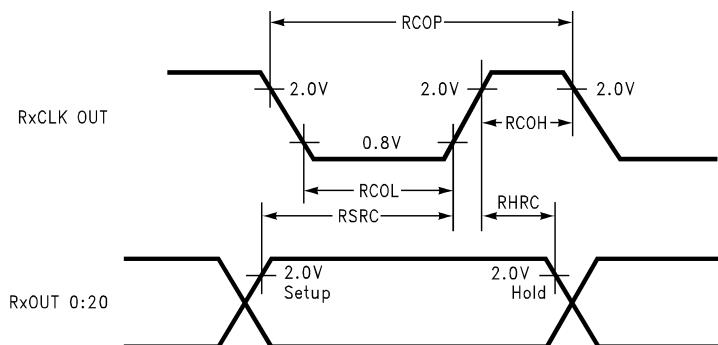


Figure 6. DS90CR218A (Receiver) Setup/Hold and High/Low Times

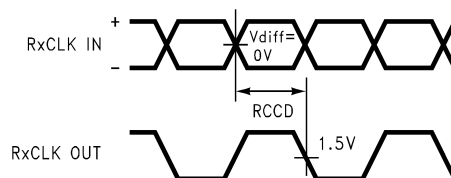


Figure 7. DS90CR218A (Receiver) Clock In to Clock Out Delay

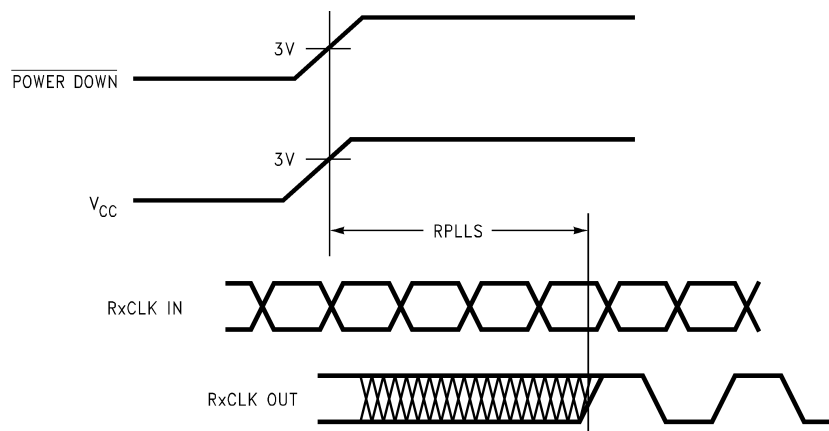


Figure 8. DS90CR218A (Receiver) Phase Lock Loop Set Time

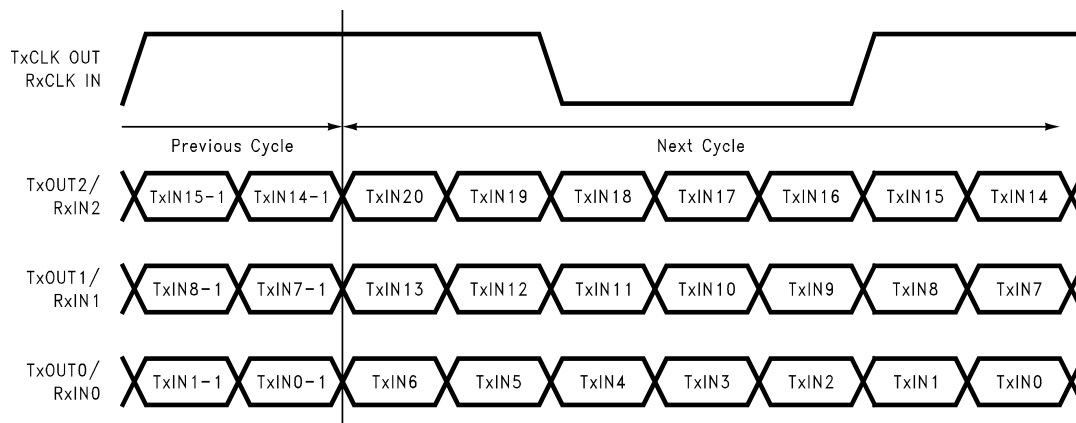


Figure 9. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

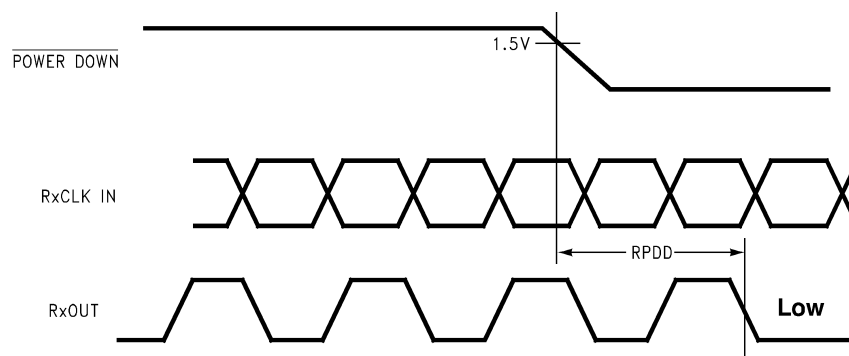


Figure 10. Receiver Powerdown Delay

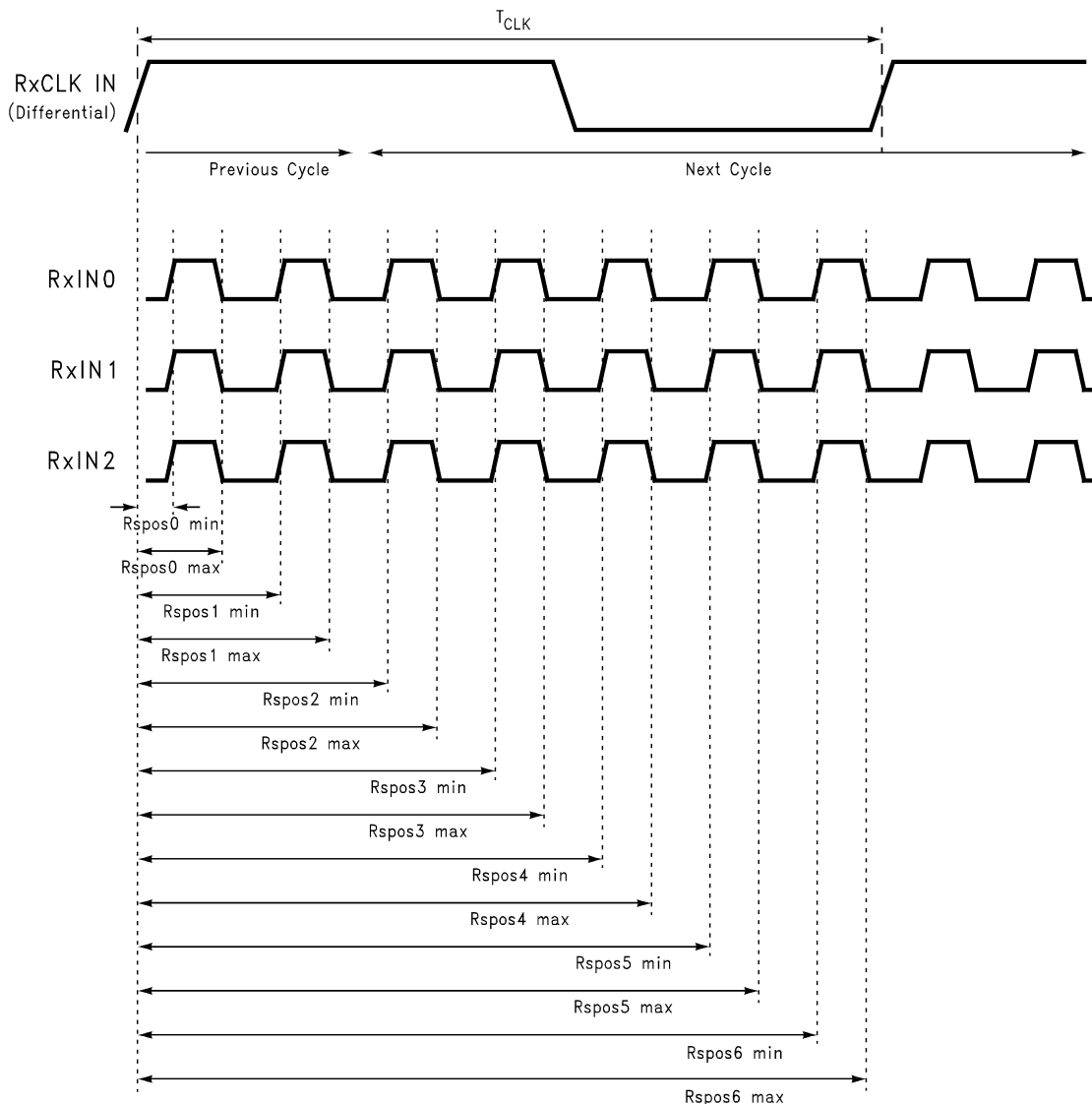
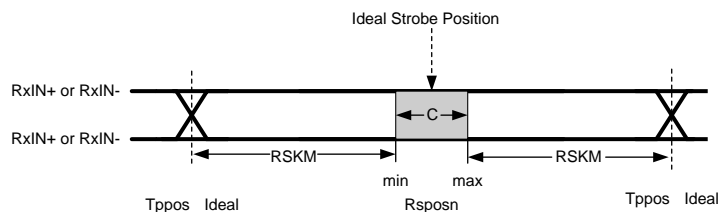


Figure 11. Receiver LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rsp0s (receiver input strobe position) min and max

Tppos Ideal — Calculated Transmitter output pulse position

RSKM \geq Cable Skew (type, length) + Source Clock Jitter (Cycle-to-cycle)⁽¹⁾ + ISI (Inter-symbol interference) + TPPOS variance (Tx dependent)⁽²⁾

Cable Skew—typically 10 ps–40 ps per foot, media dependent

(1) Cycle-to-cycle jitter is less than 250 ps at 85MHz

(2) ISI is dependent on interconnect length; may be zero

Figure 12. Receiver LVDS Input Skew Margin

APPLICATIONS INFORMATION

DS90CR218A PIN DESCRIPTIONS — Channel Link Receiver

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| RxIN+ | I | 3 | Positive LVDS differential data inputs. |
| RxIN- | I | 3 | Negative LVDS differential data inputs. |
| RxOUT | O | 21 | TTL level data outputs. |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input. |
| RxCLK IN- | I | 1 | Negative LVDS differential clock input. |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT. |
| PWR DWN | I | 1 | TTL level input. When asserted (low input) the receiver outputs are low. |
| V _{CC} | I | 4 | Power supply pins for TTL outputs. |
| GND | I | 5 | Ground pins for TTL outputs. |
| PLL V _{CC} | I | 1 | Power supply for PLL. |
| PLL GND | I | 2 | Ground pin for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | I | 3 | Ground pins for LVDS inputs. |

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of 1.785 Gbit/s. Additional applications information can be found in the following National Interface Application Notes:

| AN = #### | Topic |
|-----------|---|
| AN-1041 | Introduction to Channel Link |
| AN-1108 | Channel Link PCB and Interconnect Design-In Guidelines |
| AN-1109 | Multi-Drop Channel-Link Operation |
| AN-806 | Transmission Line Theory |
| AN-905 | Transmission Line Calculations and Differential Impedance |
| AN-916 | Cable Information |

CABLES

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 90ps (@ 85 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common-mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

RECEIVER FAILSAFE FEATURE

These receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, data outputs will all be HIGH; if the clock input is also floating/terminated, data outputs will remain in the last valid state. A floating/terminated clock input will result in a HIGH clock output.

BOARD LAYOUT

To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high-speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

UNUSED INPUTS

All unused outputs at the RxOUT outputs of the receiver must then be left floating.

TERMINATION

Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. Figure 13 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

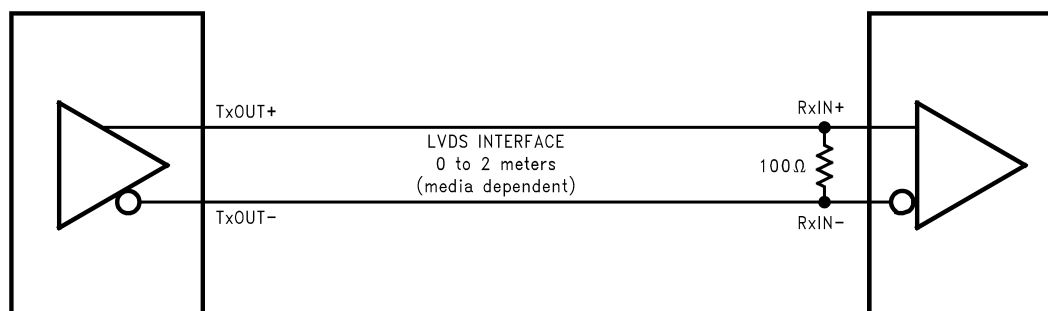


Figure 13. LVDS Serialized Link Termination

DECOUPLING CAPACITORS

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 μF , 0.01 μF and 0.001 μF . An example is shown in Figure 14. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

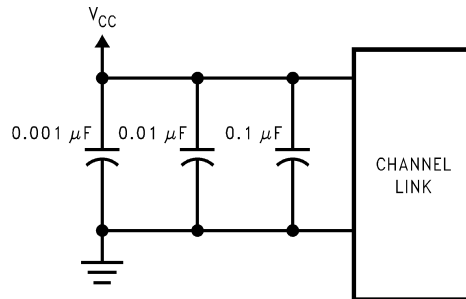


Figure 14. CHANNEL LINK Decoupling Configuration

CLOCK JITTER

The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 85 MHz clock has a period of 11.76 ns which results in a data bit width of 1.68 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

COMMON-MODE vs. DIFFERENTIAL MODE NOISE MARGIN

The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common-mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a $\pm 1.0\text{V}$ shifting of the center point due to ground potential differences and common-mode noise.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| DS90CR218AMTD/NOPB | ACTIVE | TSSOP | DGG | 48 | 38 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CR218AMTD >B | Samples |
| DS90CR218AMTDX/NOPB | ACTIVE | TSSOP | DGG | 48 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CR218AMTD >B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90CR218AMTDX/NOPB | TSSOP | DGG | 48 | 1000 | 330.0 | 24.4 | 8.6 | 13.2 | 1.6 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90CR218AMTDX/NOPB | TSSOP | DGG | 48 | 1000 | 358.0 | 343.0 | 63.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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