+3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link -65 MHz
+3.3VLVDS Transmitter 18-Bit Flat Panel Display (FPD) Link -65 MHz

Check for Samples: DS90C363A, DS90CF363A

FEATURES

- **20 to 65 MHz shift clock support**
- **Rejects > ± 3ns Jitter from VGA chip with less than 225ps output Jitter at 65MHz (TJCC)**
- **Best-in-Class Set and Hold Times on TxINPUTs**
- **Tx power consumption <130 mW (typ) at 65MHz Grayscale**
- **>50% Less Power Dissipation than BiCMOS Alternatives**
- **Tx Power-down mode <200µW (max)**
- **ESD rating >7 kV (HBM), >500V (EIAJ)**
- **Supports VGA, SVGA, XGA and Dual Pixel SXGA**
- **Narrow bus reduces cable size and cost**
- **Up to 1.3 Gbps throughput**
- **Up to 170 Megabytes/sec bandwidth**
- **345 mV (typ) swing LVDS devices for low EMI**
- **PLL requires no external components**
- **Compatible with TIA/EIA-644 LVDS standard**
- **Low profile 48-lead TSSOP package**
- **Improved replacement for:**
  - **SN75LVDS85 — DS90C363A**
  - **SN75LVDS84 — DS90CF363A**

DESCRIPTION

The DS90C363A/DS90CF363A transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbytes/sec. The DS90C363A transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. The DS90CF363A is fixed as a Falling edge strobe transmitter. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF364) without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Block Diagram

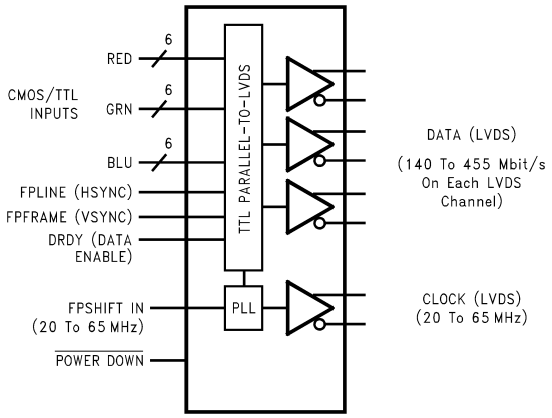


Figure 1. DS90C363A/DS90CF363A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})		−0.3V to +4V
CMOS/TTL Input Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration		Continuous
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		+260°C
Maximum Package Power Dissipation Capacity at 25°C	TSSOP Package	1.98 W
Power Dissipation Derating		16 mW/°C above +25°C
ESD Rating	HBM, 1.5 kΩ, 100 pF	> 7 kV
	EIAJ, 0Ω, 200 pF	> 500V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}
TxCLKIN frequency	18		68	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (1)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current , Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 2 Figure 5)	f = 32.5 MHz		31	43	mA
			f = 37.5 MHz		33	45	mA
			f = 65 MHz		39	52	mA
ICCTG	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 3 Figure 5)	f = 32.5 MHz		23	35	mA
			f = 37.5 MHz		28	40	mA
			f = 65 MHz		33	45	mA
ICCTZ	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE under Power Down Mode			10	55	µA

(1) V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
TCIT	TxCLK IN Transition Time (Figure 6)			5	ns
TCIP	TxCLK IN Period (Figure 7)	14.7	T	55.6	ns
TCIH	TxCLK IN High Time (Figure 7)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 7)	0.35T	0.5T	0.65T	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
LLHT	LVDS Low-to-High Transition Time (Figure 5)			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5)			0.75	1.5	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)(1)	f = 65 MHz	−0.30	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.90	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.10	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.30	6.60	6.80	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.50	8.80	9.00	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.70	11.00	11.20	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.90	13.20	13.40	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)(1)	f = 40 MHz	−0.35	0	0.35	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.22	3.57	3.92	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.79	7.14	7.49	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.36	10.71	11.06	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13.93	14.28	14.63	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.51	17.86	18.21	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.08	21.43	21.78	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)(1)	f = 32.5 MHz	−0.40	0	0.40	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		4.00	4.40	4.80	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		8.40	8.80	9.20	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		12.80	13.20	13.60	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		17.20	17.60	18.00	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		21.60	22.00	22.40	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		26.00	26.40	26.80	ns
TSTC	TxIN Setup to TxCLK IN (Figure 7)		2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 7)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay (Figure 8) T_A=25°C, V_{CC}=3.3V		3		5.5	ns
	TxCLK IN to TxCLK OUT Delay (Figure 8)		3		7.0	ns
TJCC	Transmitter Jitter Cycle-to-Cycle (Figure 13 Figure 14)(2)	f = 65 MHz		175	225	ps
		f = 40 MHz		240	380	ps
		f = 32.5 MHz		260	400	ps
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)				10	ms
TPDD	Transmitter Power Down Delay (Figure 11)				100	ns

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

(2) The Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. Output jitter is measured with a cycle-to-cycle jitter of 3ns applied to the input clock signal. A jitter event of 3ns, represents worse case jump in the clock edge from most Graphics controller VGA chips currently available. This parameter is used when calculating system margin (RSKM). See Figures 12, 13 and AN-1059.

AC Timing Diagrams

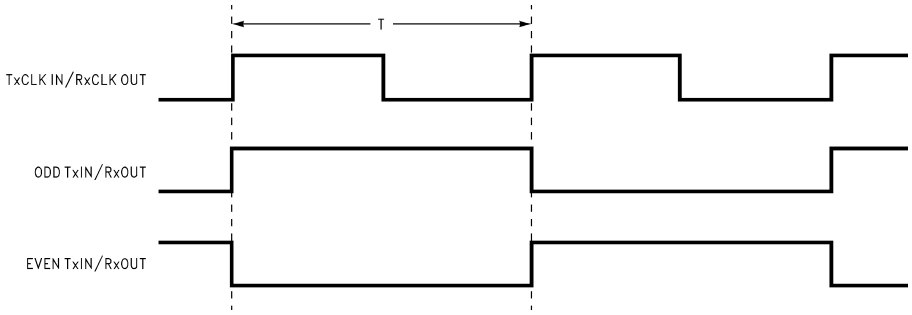
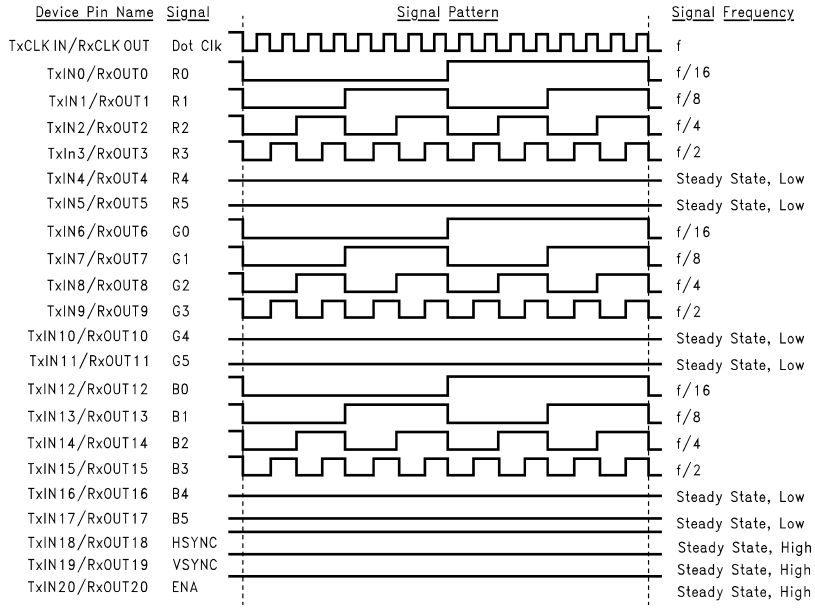


Figure 2. "Worst Case" Test Pattern



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

B. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

C. Figure 2 Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

D. Recommended pin to signal mapping. Customer may choose to define differently.

Figure 3. "16 Grayscale" Test Pattern

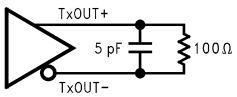


Figure 4. DS90C363A/DS90CF363A (Transmitter) LVDS Output Load

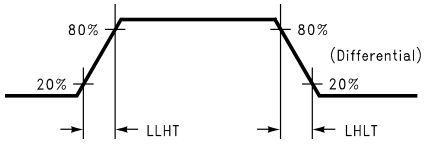


Figure 5. DS90C363A/DS90CF363A (Transmitter) LVDS Transition Times

AC Timing Diagrams (continued)

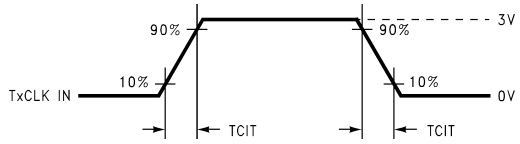


Figure 6. DS90C363A/DS90CF363A (Transmitter) Input Clock Transition Time

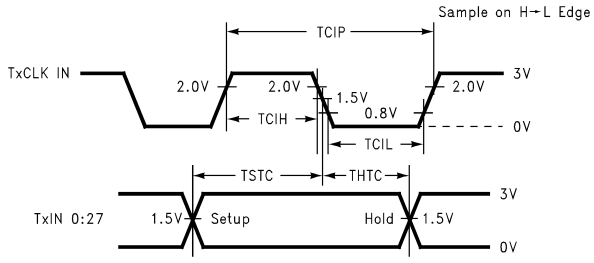


Figure 7. DS90C363A/DS90CF363A (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

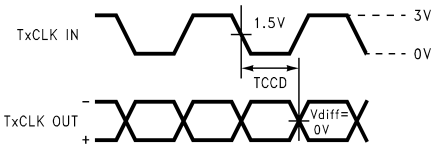


Figure 8. DS90C363A/DS90CF363A (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

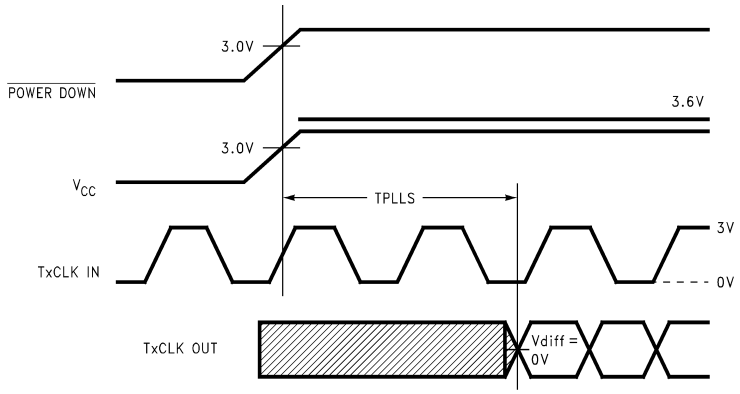


Figure 9. DS90C363A/DS90CF363A (Transmitter) Phase Lock Loop Set Time

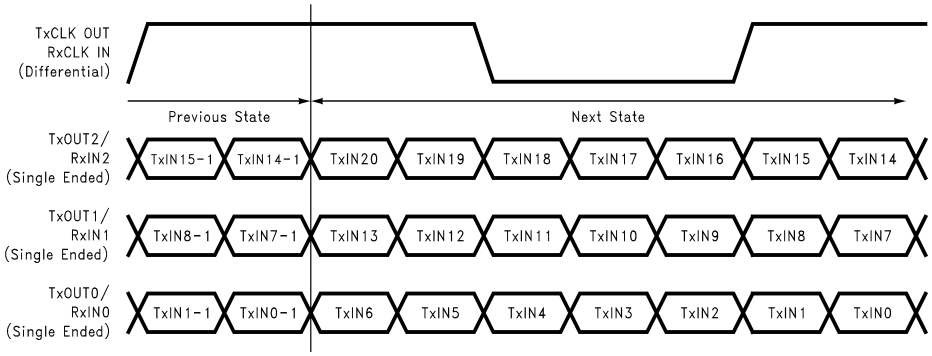


Figure 10. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

AC Timing Diagrams (continued)

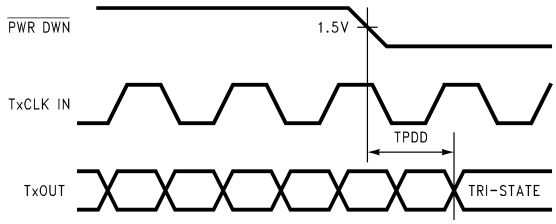


Figure 11. Transmitter Power Down Delay

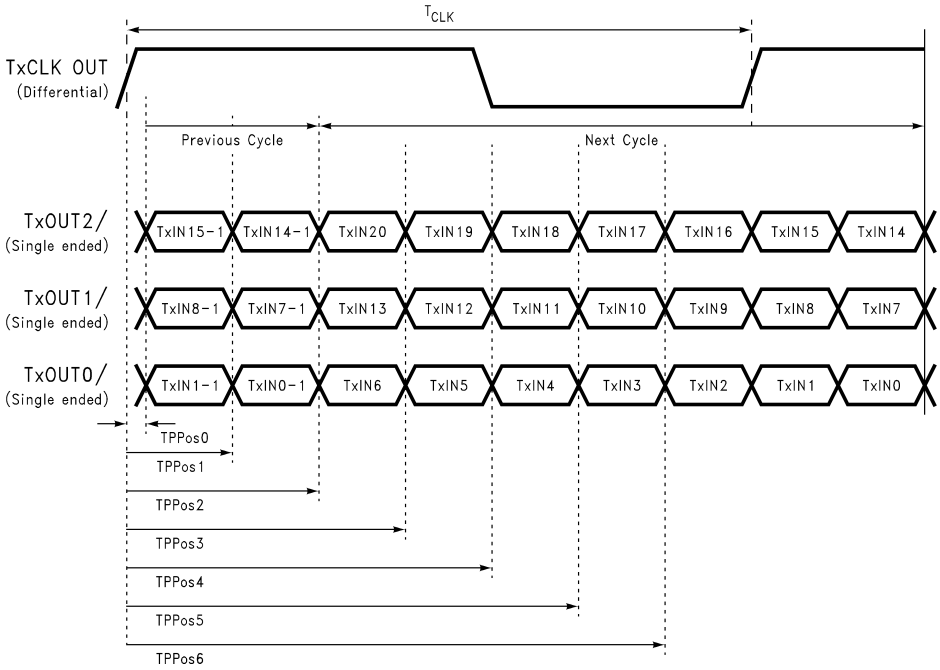


Figure 12. Transmitter LVDS Output Pulse Position Measurement

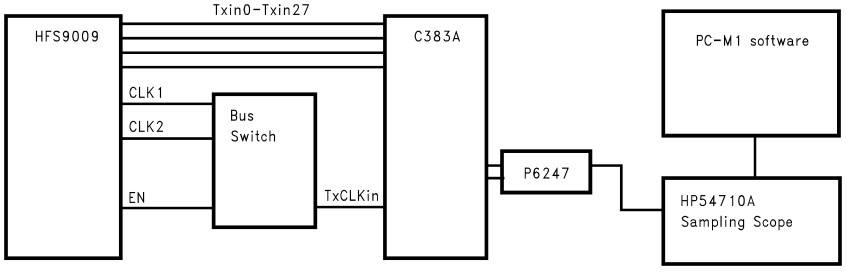


Figure 13. TJCC Test Setup

AC Timing Diagrams (continued)

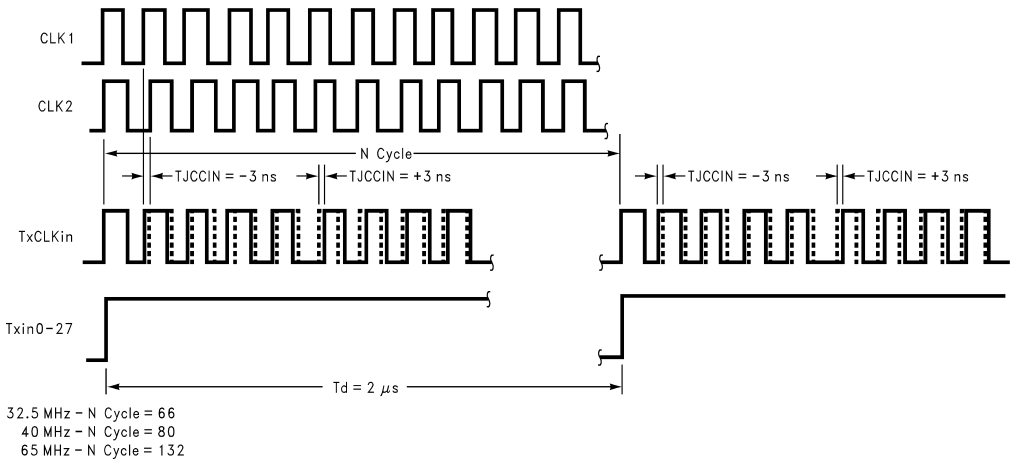


Figure 14. Timing diagram of the Input cycle-to-cycle clock jitter

PIN ASSIGNMENTS

Table 1. DS90C363A Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differentiaI data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See Applications Information section.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

Table 2. DS90CF363A Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See Applications Information section.
V_{CC}	I	4	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

APPLICATIONS INFORMATION

The DS90C363A/DS90CF363A are backward compatible with the DS90C363/DS90CF363 and are a pin-for-pin replacement. The device (DS90C363A/DS90CF363A) utilizes a different PLL architecture employing an internal 7X clock for enhanced pulse position control.

This device (DS90C363A/DS90CF363A) also features reduced variation of the TCCD parameter which is important for dual pixel applications. (See AN-1084) TCCD variation has been measured to be less than 250ps at 65MHz under normal operating conditions.

This device may also be used as a replacement for the DS90CF563 (5V, 65MHz) and DS90CF561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. The DS90C363A transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. To implement a falling edge device for the DS90C363A, the R_FB pin (pin 14) may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to Vcc implements a rising edge device.

TRANSMITTER CLOCK JITTER CYCLE-TO-CYCLE

Figures 12 and 13 illustrate the timing of the input clock relative to the input data. The input clock (TxCLKin) is intentionally shifted to the left −3ns and +3ns to the right when data (Txin0-27) is high. This 3ns of cycle-to-cycle clock jitter is repeated at a period of 2µs, which is the period of the input data (1µs high, 1µs low). At different operating frequencies the N Cycle is changed to maintain the desired 3ns cycle-to-cycle jitter at 2µs period.

TRANSMITTER INPUT CLOCK

The transmitter input clock must always be present when the device is enabled ($\overline{\text{PWR DOWN}}$ = HIGH). If the clock is stopped, the $\overline{\text{PWR DOWN}}$ pin must be used to disable the PLL. The $\overline{\text{PWR DOWN}}$ pin must be held low until after the input clock signal has been reapplied. This will ensure a proper device reset and PLL lock to occur.

POWER SEQUENCING AND POWERDOWN MODE

Outputs of the transmitter remain in TRI-STATE until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The transmitter input clock may be applied prior to powering up and enabling the transmitter. The transmitter input clock may also be applied after power up; however, the use of the $\overline{\text{PWR DOWN}}$ pin is required as described in the Transmitter Input Clock section. Do not power up and enable ($\overline{\text{PWR DOWN}}$ = HIGH) the transmitter without a valid clock signal applied to the TxCLK IN pin.

The FPD Link chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are controlled by a failsafe bias circuitry. The LVDS inputs are High-Z during initial power on and power off conditions. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

RECEIVER FAILSAFE FEATURE

The FPD Link receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be pulled to a HIGH state. This is the case if not all data channels are required in the application. Leave the extra channel's inputs open. This minimizes power dissipation and locks the unused channels outputs into a stable known (HIGH) state.

If a clock signal is present, data outputs will all be HIGH; if the clock input is also floating/terminated, data outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

Pin Diagram

DS90C363A

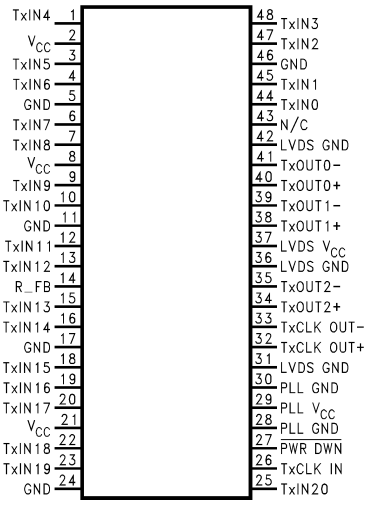


Figure 15. 48 Pin TSSOP - See Package Number DGG

DS90CF363A

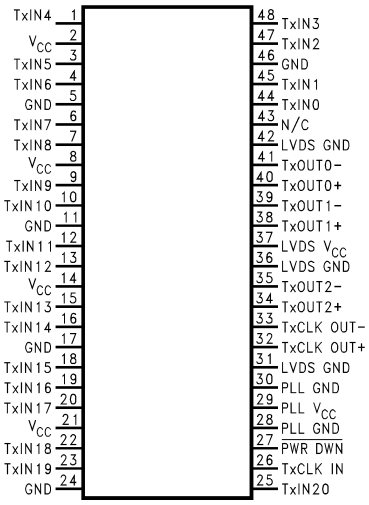


Figure 16. 48 Pin TSSOP - See Package Number DGG

Block Diagram

Figure 17. Typical Application

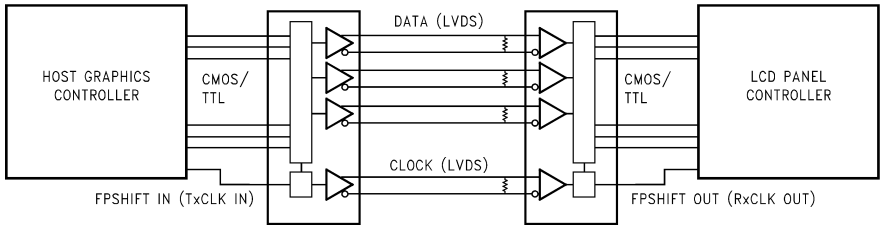


Table 3. Programmable Transmitter (DS90C363A)

Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

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