

# DS42MB100 4.25 Gbps 2:1/1:2 CML Mux/Buffer with Transmit Pre-Emphasis and Receive Equalization

 Check for Samples: [DS42MB100](#)

## FEATURES

- 2:1 Multiplexer and 1:2 Buffer
- 0.25 – 4.25 Gbps Fully Differential Data Paths
- Fixed Input Equalization
- Programmable Output Pre-Emphasis
- Independent Pre-Emphasis Controls
- Programmable Loopback Modes
- On-Chip Terminations
- HBM ESD Rating 6 kV on All Pins
- +3.3V Supply
- Lead-Less WQFN-36 Package
- -40°C to +85°C Operating Temperature Range

## APPLICATIONS

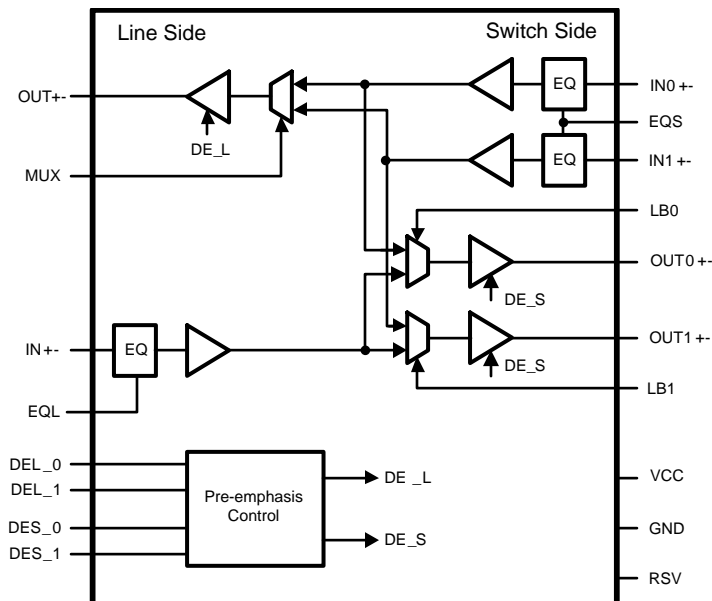
- Backplane Driver or Cable driver
- Redundancy and Signal Conditioning Applications
- CPRI/OBSAI

## DESCRIPTION

The DS42MB100 is a signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane redundancy or cable driving applications. Signal conditioning features include input equalization and programmable output pre-emphasis that enable data communication in FR4 backplane up to 4.25 Gbps. Each input stage has a fixed equalizer to reduce ISI distortion from board traces.

All output drivers have four selectable levels of Pre-emphasis to compensate for transmission losses from long FR4 backplane or cable attenuation reducing deterministic jitter. The Pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs are internally terminated with 100Ω differential terminating resistors. All driver outputs are internally terminated with 50Ω terminating resistors to  $V_{CC}$ .

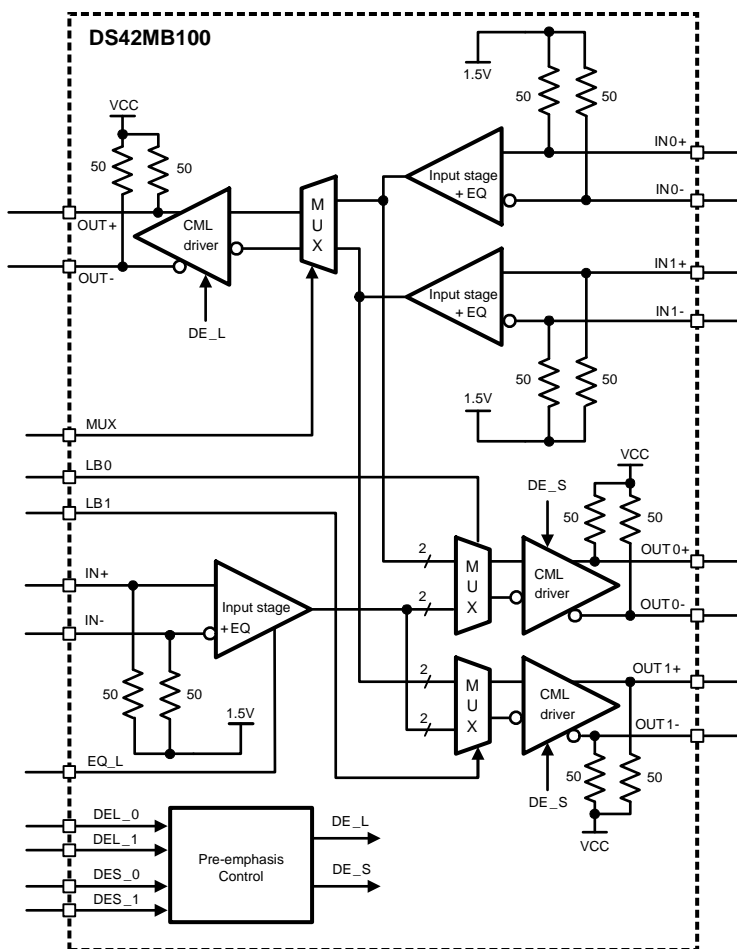
## Functional Block Diagram



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### Simplified Block Diagram



### PIN DESCRIPTIONS

Pin Name	Pin Number	I/O	Description
<b>LINE SIDE HIGH SPEED DIFFERENTIAL IO's</b>			
IN+ IN-	33 34	I	Inverting and non-inverting differential inputs at the line side. IN+ and IN- have an internal 50Ω connected to an internal reference voltage. See <a href="#">Figure 7</a> .
OUT+ OUT-	30 31	O	Inverting and non-inverting differential outputs at the line side. OUT+ and OUT- have an internal 50Ω connected to V <sub>CC</sub> .
<b>SWITCH SIDE HIGH SPEED DIFFERENTIAL IO's</b>			
OUT0+ OUT0-	3 4	O	Inverting and non-inverting differential outputs at the switch side. OUT0+ and OUT0- have an internal 50Ω connected to V <sub>CC</sub> .
OUT1+ OUT1-	22 21	O	Inverting and non-inverting differential outputs at the switch side. OUT1+ and OUT1- have an internal 50Ω connected to V <sub>CC</sub> .
IN0+ IN0-	6 7	I	Inverting and non-inverting differential inputs to the mux at the switch side. IN0+ and IN0- have an internal 50Ω connected to an internal reference voltage. See <a href="#">Figure 7</a> .
IN1+ IN1-	25 24	I	Inverting and non-inverting differential inputs to the mux at the switch side. IN1+ and IN1- have an internal 50Ω connected to an internal reference voltage. See <a href="#">Figure 7</a> .
<b>CONTROL (3.3V LVCMOS)</b>			
MUX	19	I	A logic low at MUX selects IN1±. MUX is internally pulled high. Default state for MUX is IN0±.
EQL	11		A logic low enables the input equalizer on the line side. EQL is internally pulled high. Default is with EQ disabled.
EQS	36	I	A logic low enables the input equalizer on the switch side. EQS is internally pulled high. Default is with EQ disabled.

**PIN DESCRIPTIONS (continued)**

Pin Name	Pin Number	I/O	Description
DEL_0 DEL_1	18 27	I	DEL_0 and DEL_1 select the output Pre-emphasis of the line side drivers (OUT±). DEL_0 and DEL_1 are internally pulled high.
DES_0 DES_1	10 1	I	DES_0 and DES_1 select the output Pre-emphasis of the switch side drivers (OUT0±, OUT1±). DES_0 and DES_1 are internally pulled high.
LB0	28	I	A logic low at LB0 enables the internal loopback path from IN0± to OUT0±. LB0 is internally pulled high.
LB1	26	I	A logic low at LB1 enables the internal loopback path from IN1± to OUT1±. LB1 is internally pulled high.
RSV	17	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.
<b>POWER</b>			
V <sub>CC</sub>	5, 13, 15, 23, 32	P	V <sub>CC</sub> = 3.3V ± 5%. Each V <sub>CC</sub> pin should be connected to the V <sub>CC</sub> plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V <sub>CC</sub> pin. It is recommended to have a 0.01 μF or 0.1 μF, X7R, size-0402 bypass capacitor from each V <sub>CC</sub> pin to ground plane.
GND	2, 8, 9, 12, 14, 16, 20, 29, 35	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	DAP is the metal contact at the bottom side, located at the center of the WQFN package. It should be connected to the GND plane with at least 16 via to lower the ground impedance and improve the thermal performance of the package.

**Functional Description**

The DS42MB100 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy up to 4.25 Gbps. Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB of transmission loss from a short backplane trace (about 10 inches backplane). The output driver has pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane, and minimize the deterministic jitter caused by the amplitude disparity. The DS42MB100 provides four steps of user-selectable Pre-emphasis ranging from 0, -3, -6 and -9 dB to handle different lengths of backplane. [Figure 1](#) shows a driver Pre-emphasis waveform. The Pre-emphasis duration is 188ps nominal, corresponds to 0.8 bit-width at 4.25 Gbps. The Pre-emphasis levels of switch-side and line-side can be individually programmed.

The high speed inputs are self-biased to about 1.3V and are designed for AC coupling allowing the DS42MB100 to be directly inserted into the datapath without any limitation. The ideal AC coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC coupling capacitor value ranges between 100 and 1000nF, some specifications with scrambled data may require a larger coupling capacitor for optimal performance. To reduce unwanted parasitics around and within the AC coupling capacitor, a body size of 0402 is recommended. [Figure 6](#) shows the AC coupling capacitor placement in an AC test circuit. The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL and CML.

**Table 1. Logic Table For Multiplex Controls**

MUX	Mux Function
0	MUX select switch input, IN1±.
1 (default)	MUX select switch input, IN0±.

**Table 2. Logic Table For Loopback Controls**

LB0	Loopback Function
0	Enable loopback from IN0± to OUT0±.
1 (default)	Normal mode. Loopback disabled.
LB1	Loopback Function
0	Enable loopback from IN1± to OUT1±.
1 (default)	Normal mode. Loopback disabled.

**Table 3. Line-Side Pre-Emphasis Controls**

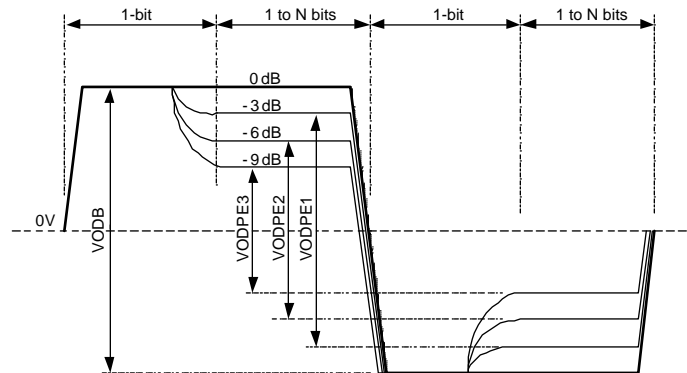
DEL_[1:0]	Pre-Emphasis Level in mV <sub>PP</sub> (VODB)	Pre-Emphasis Level in mV <sub>PP</sub> (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 Board Trace
0 0	1300	1300	0	10 inches
0 1	1300	920	-3	20 inches
1 0	1300	650	-6	30 inches
1 1 (default)	1300	461	-9	40 inches

**Table 4. Switch-Side Pre-Emphasis Controls**

DES_[1:0]	Pre-Emphasis Level in mV <sub>PP</sub> (VODB)	Pre-Emphasis Level in mV <sub>PP</sub> (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 Board Trace
0 0	1300	1300	0	10 inches
0 1	1300	920	-3	20 inches
1 0	1300	650	-6	30 inches
1 1 (default)	1300	461	-9	40 inches

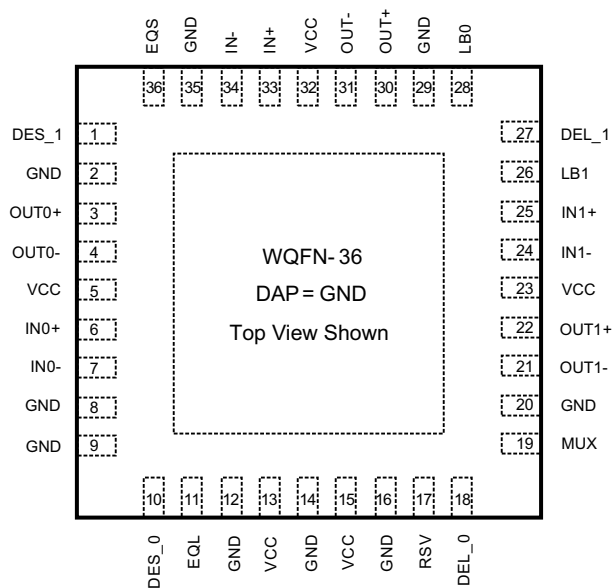
**Table 5. EQ Controls for the Line Switch Sides**

EQL or EQS	Equalizer Function
0	Enable equalization.
1 (default)	Normal mode. Equalization disabled.



**Figure 1. Driver Pre-Emphasis Differential Waveform (Showing All 4 Pre-Emphasis Steps)**

## Connection Diagram



**Figure 2. WQFN Package**  
See Package Number NJK0036A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	-0.3V to 4V
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
CML Input/Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature Soldering, 4 seconds	+260°C
Thermal Resistance, $\theta_{JA}$ <sup>(3)</sup>	26.2°C/W
Thermal Resistance, $\theta_{JC}$	3.3°C/W
Thermal Resistance, $\Phi_{JB}$	11.1°C/W
ESD Rating <sup>(4)</sup> HBM, 1.5 k $\Omega$ , 100 pF CDM MM	6 kV 1.25 kV 350V

- (1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Thermal resistances are based on having 16 thermal relief vias on the DAP pad under the 0 airflow condition.
- (4) ESD tests conform to the following standards:  
Human Body Model applicable standard: MIL-STD-883, Method 3015.7  
Machine Model applicable standard: JESD22-A115-A (ESD MM standard of JEDEC)  
Field-induced Charge Device Model: Applicable standard JESD22-C101-C (ESD FICDM standard of JEDEC)

## Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC-GND}$ )	3.135	3.3	3.465	V
Supply Noise Amplitude 10 Hz to 2 GHz			100	mV <sub>PP</sub>
Ambient Temperature	-40		85	°C
Case Temperature			100	°C

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ <sup>(1)</sup>	Max	Units
<b>LVCMOS DC SPECIFICATIONS</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC} + 0.3$	V
$V_{IL}$	Low Level Input Voltage		-0.3		0.8	V
$I_{IH}$	High Level Input Current	$V_{IN} = V_{CC}$	-10		10	μA
$I_{IL}$	Low Level Input Current	$V_{IN} = GND$	75	94	124	μA
$R_{PU}$	Pull-High Resistance			35		kΩ
<b>RECEIVER SPECIFICATIONS</b>						
$V_{ID}$	Differential Input Voltage Range <sup>(2)</sup>	AC Coupled Differential Signal Below 1.25 Gbps Between 1.25 Gbps–3.125 Gbps Above 3.125 Gbps This parameter is not tested at production.	100 100 100		1750 1560 1200	mV <sub>P-P</sub> mV <sub>P-P</sub> mV <sub>P-P</sub>
$V_{ICM}$	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground.		1.3		V
$R_{ITD}$	Input Differential Termination <sup>(3)</sup>	On-chip differential termination between IN+ or IN-.	84	100	116	Ω
<b>DRIVER SPECIFICATIONS</b>						
$V_{ODB}$	Output Differential Voltage Swing without Pre-Emphasis <sup>(4)</sup>	$R_L = 100\Omega \pm 1\%$ DES_1=DES_0=0 DEL_1=DEL_0=0 Driver Pre-emphasis disabled. Running K28.7 pattern at 4.25 Gbps. See Figure 6 for test circuit.	1100	1300	1500	mV <sub>P-P</sub>
$V_{PE}$	Output Pre-Emphasis Voltage Ratio $20 \cdot \log(V_{ODPE}/V_{ODB})$	$R_L = 100\Omega \pm 1\%$ Running K28.7 pattern at 4.25 Gbps DEX_[1:0]=00 DEX_[1:0]=01 DEX_[1:0]=10 DEX_[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See Figure 1 on waveform. See Figure 6 for test circuit.		0 -3 -6 -9		dB dB dB dB
$T_{PE}$	Pre-Emphasis Width	Tested at -9 dB Pre-emphasis level, DEX[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See Figure 5 on measurement condition.	125	188	250	ps
$R_{OTSE}$	Output Termination <sup>(3)</sup>	On-chip termination from OUT+ or OUT- to $V_{CC}$	42	50	58	Ω

(1) Typical parameters measured at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ , and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

(2) This parameter is guaranteed by design and/or characterization. It is not tested in production.

(3) IN+ and IN- are generic names refer to one of the many pairs of complimentary inputs of the DS42MB100. OUT+ and OUT- are generic names refer to one of the many pairs of the complimentary outputs of the DS42MB100. Differential input voltage  $V_{ID}$  is defined as  $|IN+ - IN-|$ . Differential output voltage  $V_{OD}$  is defined as  $|OUT+ - OUT-|$ .

(4) K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000} K28.5 pattern is a 20-bit repeating pattern of +K28.5 and -K28.5 code groups {110000 0101 001111 1010}

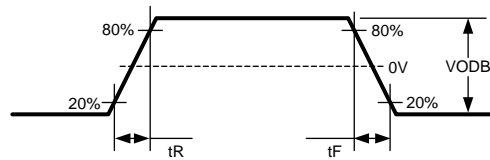
## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

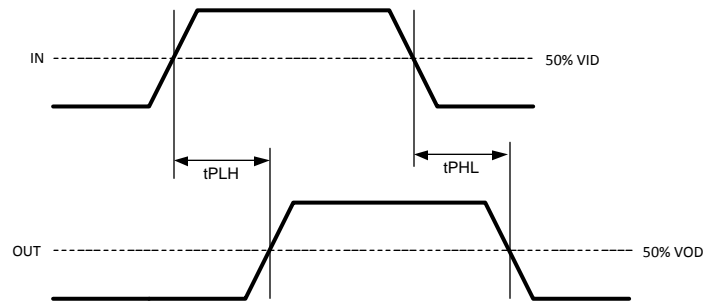
Parameter		Test Conditions	Min	Typ <sup>(1)</sup>	Max	Units
R <sub>OTD</sub>	Output Differential Termination	On-chip differential termination between OUT+ and OUT-		100		Ω
ΔR <sub>OTSE</sub>	Mis-Match in Output Termination Resistors	Mis-match in output terminations at OUT+ and OUT-			5	%
V <sub>OCM</sub>	Output Common Mode Voltage			2.7		V
<b>POWER DISSIPATION</b>						
P <sub>D</sub>	Power Dissipation	V <sub>DD</sub> = 3.3V @ 25°C All outputs terminated by 100Ω ±1%. DEL_[1:0]=0, DES_[1:0]=0 Running PRBS 2 <sup>7</sup> -1 pattern at 4.25 Gbps		0.45		W
<b>AC CHARACTERISTICS</b>						
t <sub>R</sub>	Differential Low to High Transition Time	Measured with a clock-like pattern at 4.25 Gbps, between 20% and 80% of the differential output voltage. Pre-emphasis disabled. Transition time is measured with fixture as shown in <a href="#">Figure 6</a> , adjusted to reflect the transition time at the output pins.		85		ps
t <sub>F</sub>	Differential High to Low Transition Time			85		ps
t <sub>PLH</sub>	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output.			1	ns
t <sub>PHL</sub>	Differential High to Low Propagation Delay				1	ns
t <sub>SKP</sub>	Pulse Skew	t <sub>PHL</sub> - t <sub>PLH</sub>			20	ps
t <sub>SKO</sub>	Output Skew <sup>(5)</sup>	Difference in propagation delay among data paths in the same device.			100	ps
t <sub>SKPP</sub>	Part-to-Part Skew	Difference in propagation delay between the same output from devices operating under identical condition.			100	ps
t <sub>SM</sub>	Mux Switch Time	Measured from V <sub>IH</sub> or V <sub>IL</sub> of the mux-control or loopback control to 50% of the valid differential output.		1.8	6	ns
RJ	Device Random Jitter <sup>(6)</sup>	See <a href="#">Figure 6</a> for test circuit. Alternating 1-0 pattern. EQ and pre-emphasis disabled. At 0.25 Gbps At 1.25 Gbps At 4.25 Gbps			2 2 2	psrms psrms psrms
DJ	Device Deterministic Jitter <sup>(7)</sup>	See <a href="#">Figure 6</a> for test circuit. EQ and pre-emphasis disabled Between 0.25 and 4.25Gbps with PRBS7 pattern for DS42MB100 @ -40°C to 85°C			35	pspp
DR	Data Rate <sup>(8)</sup>	Tested with alternating 1-0 pattern	0.25		4.25	Gbps

- (5) t<sub>SKO</sub> is the magnitude difference in the propagation delays among data paths. An example is the output skew among data paths from IN0± to OUT± and IN1± to OUT±. Another example is the output skew among data paths from IN± to OUT0± and IN± to OUT1±. t<sub>SKO</sub> also refers to the delay skew of the loopback paths of the same port and between similar data paths. An example is the output skew among data paths IN0± to OUT0± and IN1± to OUT1±.
- (6) Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation  $\sqrt{(R_{J_{OUT}})^2 - (R_{J_{IN}})^2}$ , where R<sub>J<sub>OUT</sub></sub> is the total random jitter measured at the output of the device in psrms, R<sub>J<sub>IN</sub></sub> is the random jitter of the pattern generator driving the device.
- (7) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ<sub>OUT</sub> - DJ<sub>IN</sub>), where DJ<sub>OUT</sub> is the total peak-to-peak deterministic jitter measured at the output of the device in pspp, DJ<sub>IN</sub> is the peak-to-peak deterministic jitter of the pattern generator driving the device.
- (8) This parameter is guaranteed by design and/or characterization. It is not tested in production.

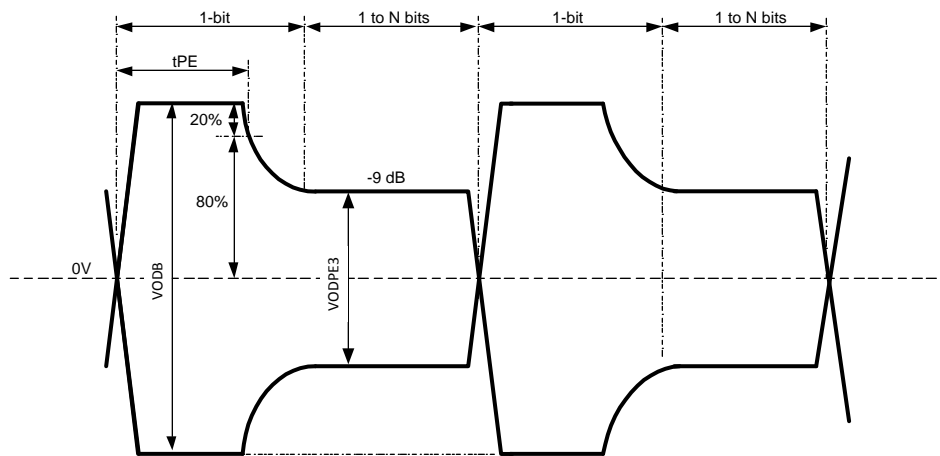
**TIMING DIAGRAMS**



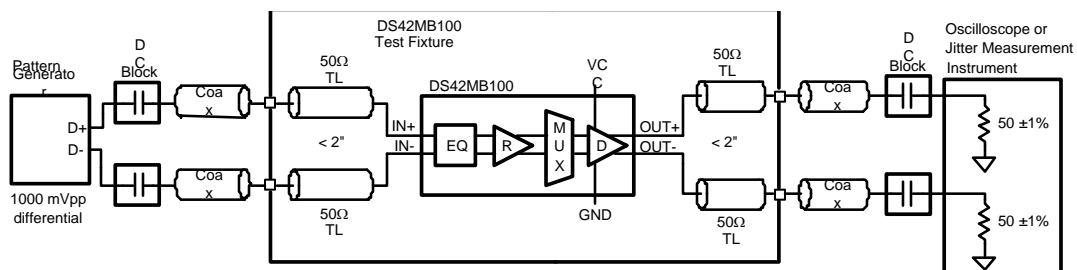
**Figure 3. Driver Output Transition Time**



**Figure 4. Propagation Delay From Input To Output**



**Figure 5. Test Condition For Output Pre-Emphasis Duration**



**Figure 6. AC Test Circuit**



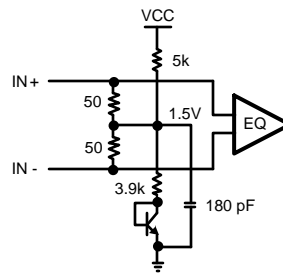


Figure 7. Receiver Input Termination and Bias Circuit

APPLICATION INFORMATION

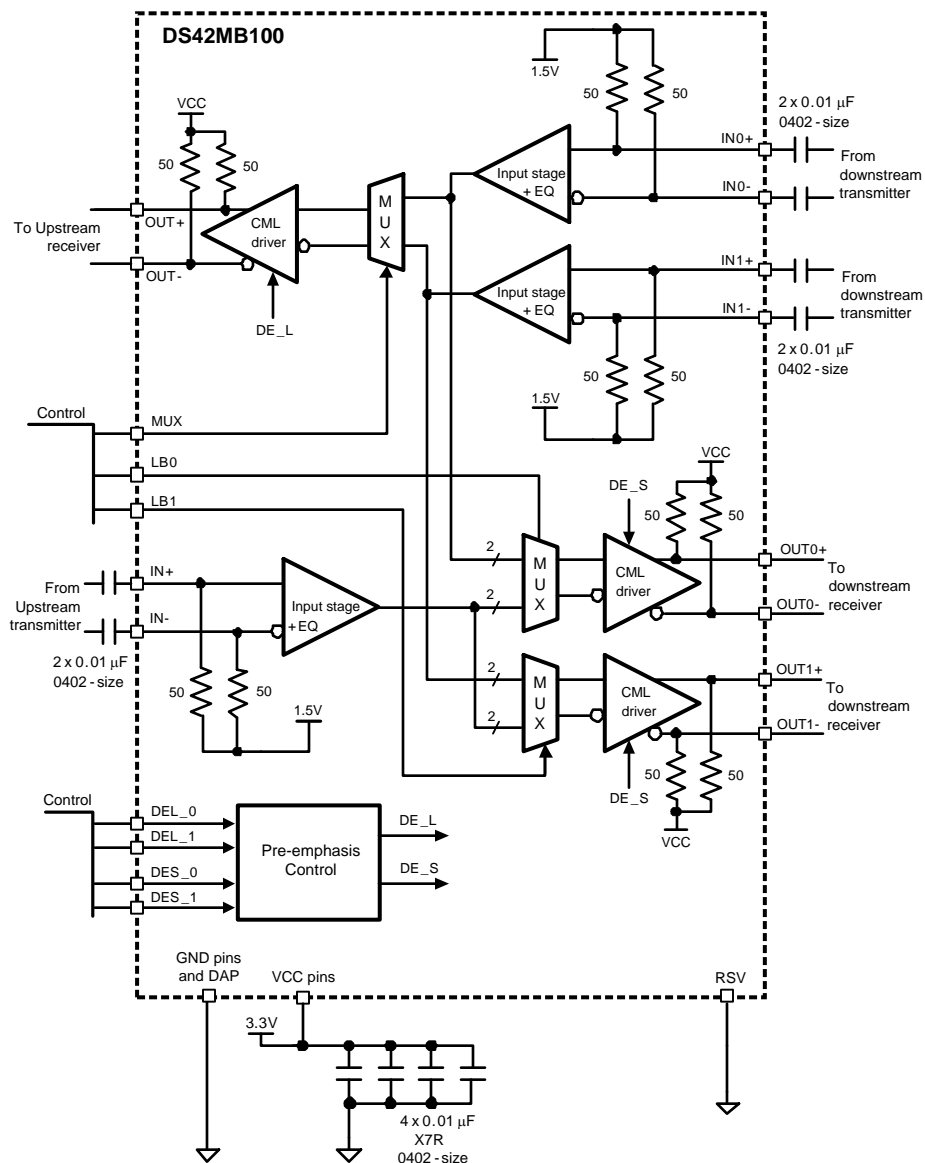


Figure 8. Application Diagram

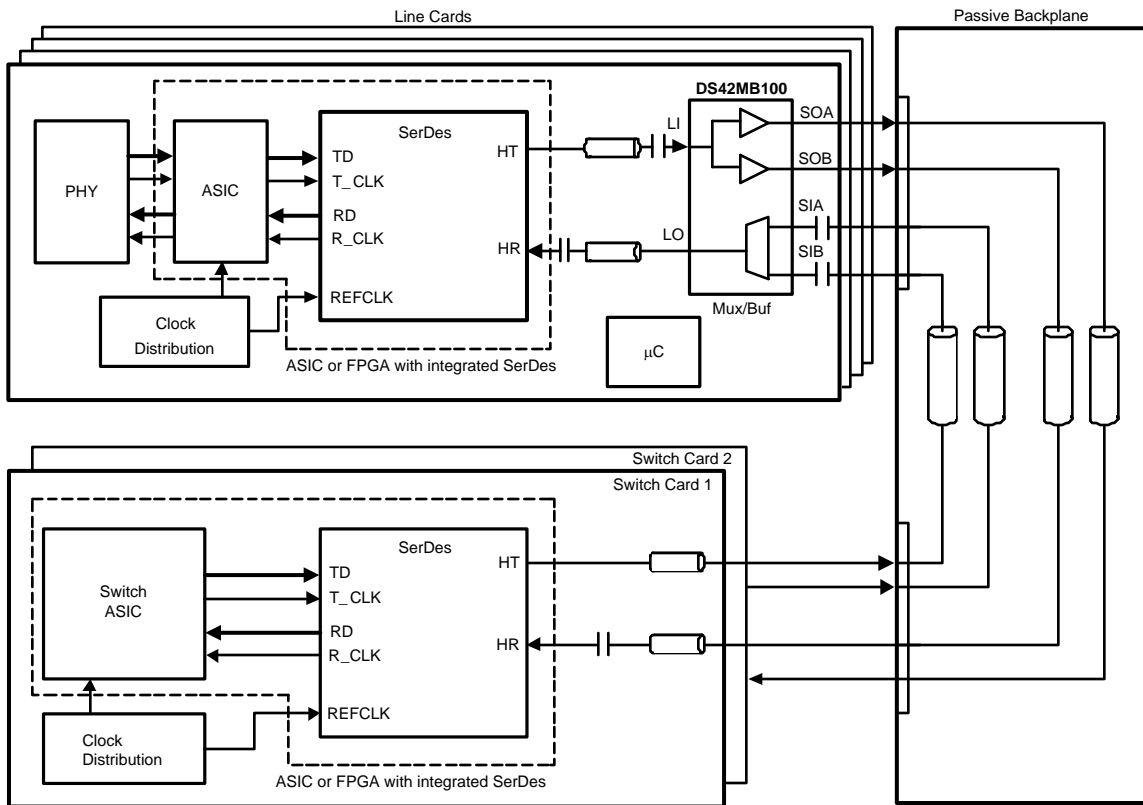




Figure 9. Network Switch System with Redundancy

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS42MB100TSQ/NOPB	ACTIVE	WQFN	NJK	36	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	42MB100	
DS42MB100TSQE/NOPB	ACTIVE	WQFN	NJK	36	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	42MB100	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS42MB100TSQ/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS42MB100TSQE/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

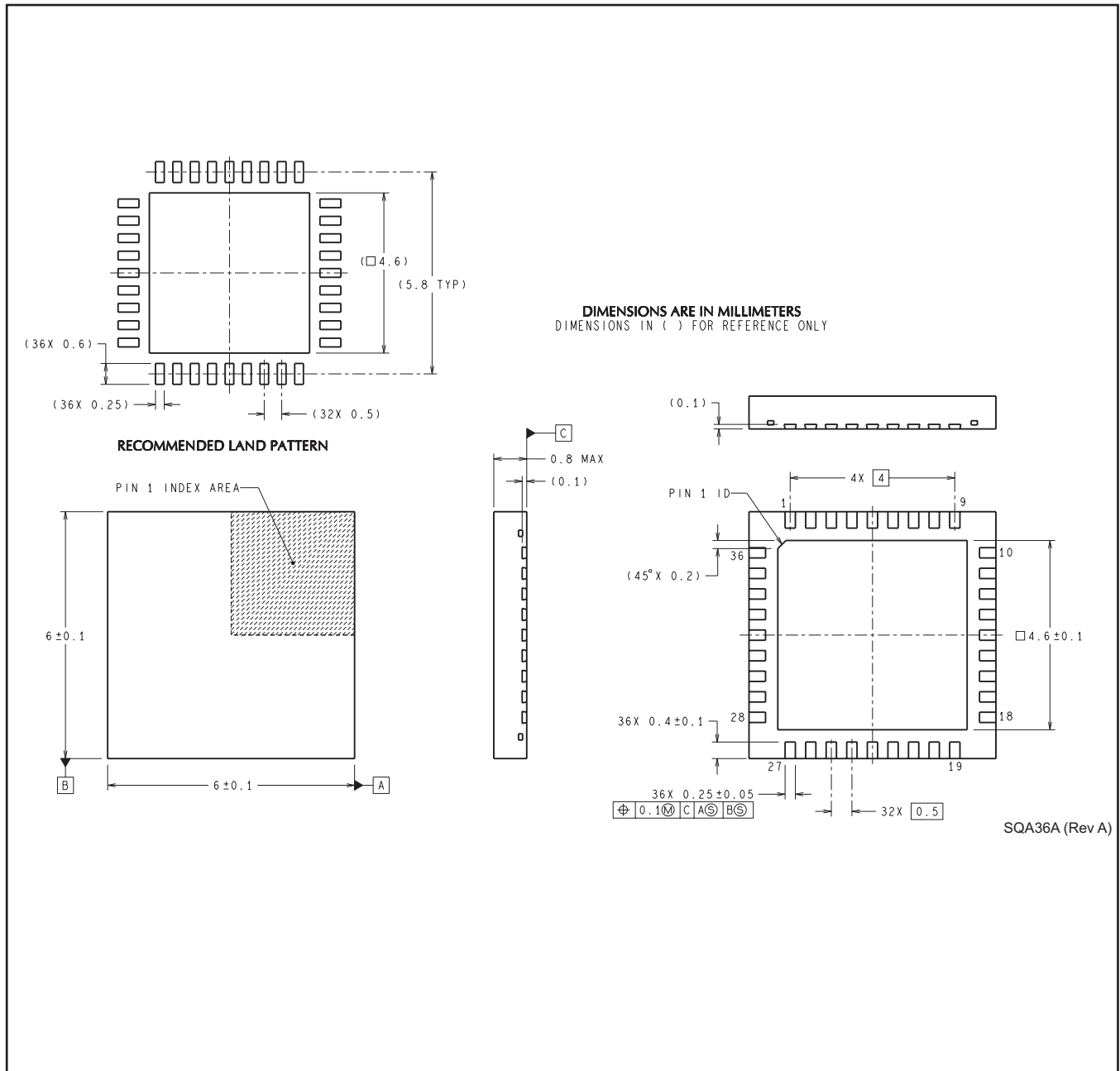
**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS42MB100TSQ/NOPB	WQFN	NJK	36	250	213.0	191.0	55.0
DS42MB100TSQE/NOPB	WQFN	NJK	36	250	213.0	191.0	55.0

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