DS3886A BTL 9-Bit Latching Data Transceiver

Check for Samples: DS3886A

FEATURES

- **Fast Propagation Delay (3ns typ)**
- **9-BIT BTL Latched Transceiver**
- **Driver Incorporates Edge Triggered Latches**
- **Receiver Incorporates Transparent Latches**
- **Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)**
- **Supports Live Insertion**
- **Glitch free Power-Up/Down Protection**
- **Typically Less than 5 pF Bus-port Capacitance**
- **Low Bus-Port Voltage Swing (typically 1V) at 80 mA**
- **Exceeds 2 KV ESD Testing (Human Body Model)**
- **Open Collector Bus-Port Outputs Allows Wired-OR Connection**
- **Controlled Rise and Fall Time to Reduce Noise Coupling to Adjacent Lines**
- **TTL Compatible Driver and Control Inputs**
- **Built in Bandgap Reference with Separate QV$_{CC}$ and QGND Pins for Precise Receiver Thresholds**
- **Individual Bus-port Ground Pins**
- **Product offered in PLCC and PQFP Package Styles**
- **Tight Skew (0.5 ns typical)**

DESCRIPTION

The DS3886A is a higher speed, lower power, pin compatible version of the DS3886.

The DS3886A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3886A is a BTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. The DS3886A incorporates an edge-triggered latch in the driver path which can be bypassed during fall-through mode of operation and a transparent latch in the receiver path. Utilization of the DS3886A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3886A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with it's collector to isolate the transistor output capacitance from the bus, thus reducing the bus loading in the inactive state. The combined output capacitance of the driver output and receiver input is less than 5pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by Texas Instruments, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QV$_{CC}$ and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE and fully TTL compatible.

The DS3886A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V$_{CC}$ pin. The DS3886A also provides glitch free power up/down protection during power sequencing.

DESCRIPTION CONTINUED

The DS3886A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two Logic V_{CC} pins on the DS3886A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the T/$\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} +0.5V.

There are three different types of ground pins on the DS3886A; the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3886A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power up/down sequencing.

The DS3886A is offered in the 44-pin PQFP high density package style.

Connection Diagram

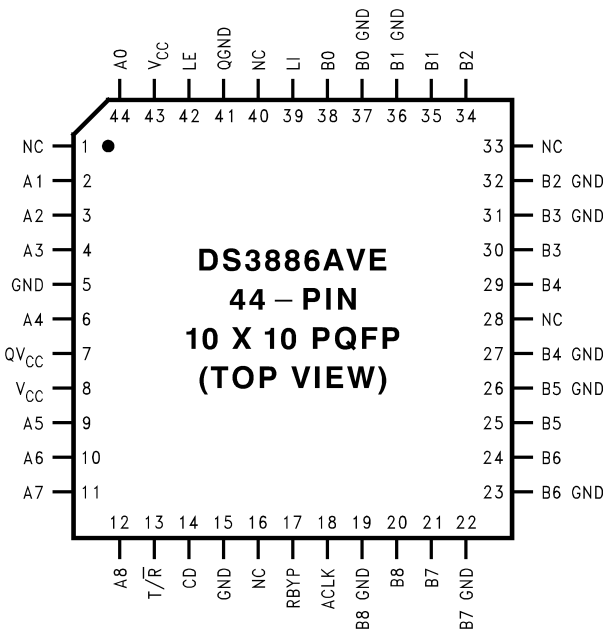


Figure 1. See Package Number PGB0044A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15 mA
Bus Termination Voltage	2.4V
Power Dissipation at 25°C	
PQFP (PGB0044A)	1.3W
Derate PQFP Package (PGB0044A)	11.1 mW/°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

(1) All input and/or output pins shall not exceed V_{CC} plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50 mA. Exception, LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}. Furthermore, the difference between V_{CC} and QV_{CC} should never be greater than 0.5V at any time including power-up.

(2) "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Bus Termination Voltage (V_T)	2.06	2.14	V
Operating Free Air Temperature	0	70	°C

DC Electrical Characteristics[1][2][3]

T_A = 0° to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT (CD, T/$\overline{R}$, An, ACLK, LE and RBYP)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} = 5.5V			250	µA
I_{IH}	Input High Current	V_{IN} = 2.4V, An = CD = 0.5V, T/$\overline{R}$ = 2.4V			40	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V, An = CD = 0.5V, T/$\overline{R}$ = 2.4V			−10	µA
I_{IL}	Input Low Current	An Port, An = 0.5V, CD = 0.5V			−100	µA
		T/R = 2.4V, RBYp = 2.4V				
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −12 mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT (Bn)						
V_{OLB}	Output Low Bus Voltage [2]	An = T/$\overline{R}$ = 2.4V, CD = 0.5V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OFF}	Output Off Low Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 0.75V, CD = 0.5V			−200	µA
	Output Off High Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 2.1V, CD = 0.5V			200	µA
	Output Off Low Current-Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 0.75V			−50	µA
	Output Off High Current-Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 2.1V			50	µA
V_{TH}	Receiver Input Threshold	T/$\overline{R}$ = CD = 0.5V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, Bn = 1 mA	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, Bn = 10 mA	2.9	3.9	5.0	V

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: V_{CC} = 5V and T_A = 25°C, unless otherwise stated.

(2) Only one output should be shorted at a time, and duration of the short should not exceed one second.

(3) Input waveforms shall have a rise and fall time of 3 ns.

DC Electrical Characteristics[1][2][3] (continued)

T_A = 0° to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CLN}	Negative Clamp Voltage	I_{CLAMP} = −12 mA			−1.2	V
RECEIVER OUTPUT (An)						
V_{OH}	Voltage Output High	Bn = 1.1V, I_{OH} = −2mA, T/$\overline{R}$ = CD = 0.5V	2.4	3.2		V
V_{OL}	Voltage Output Low	T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 24 mA		0.35	0.5	V
		T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 8 mA		0.30	0.4	V
I_{OZ}	TRI-STATE Leakage Current	V_{IN} = 2.4V, CD = 2.4V, T/$\overline{R}$ = 0.5V, Bn = 0.75V			10	µA
		V_{IN} = 0.5V, CD = 2.4V, T/$\overline{R}$ = 0.5V, Bn = 0.75V			−10	µA
I_{OS}	Output Short Circuit Current	Bn = 1.1V, T/$\overline{R}$ = CD = 0.5V [1]	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CCT}	I_{CCT}—Power Supply Current	T/$\overline{R}$ = All An = 3.4V, CD = 0.5V				
	for a TTL High Input	ACLK = LE = RBYP = 3.4V		55	62	mA
	(V_{IN} = V_{CC} − 2.1V)					
	Supply Current: Sum of V_{CC},	T/$\overline{R}$ = 0.5V, All Bn = 2.1V, LE = CD = 0.5V		45	53	mA
	QV_{CC} and LI	ACLK = RBYP = 3.4V				
I_{LI}	Live Insertion Current	T/$\overline{R}$ = An = CD = ACLK = 0.5V		1.5	2.2	mA
		T/$\overline{R}$ = All An = RBYB = 2.4V, CD = ACLK = 0.5V		3	4.5	mA

AC Electrical Characteristics[1]

T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = RBYP = 3V	1	3	5	ns
t_{PLH}	Fall-through mode		(Figure 2 and Figure 3)	1.5	3	5	ns
t_{PHL}	ACLK to Bn	Propagation Delay	CD = RBYP = 0V, T/$\overline{R}$ = 3V	1.7	4	6.5	ns
t_{PLH}	Latch mode		(Figure 2 and Figure 5)	2	4	6.5	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = 3V, An = 3V	3	5	9	ns
t_{PLH}		Disable Time	(Figure 2 and Figure 4)	2.5	5	6.7	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	CD = 0V (Figure 11 and Figure 12), RBYP = 3V	9	13	18	ns
t_{PLH}		Disable Time	CD = 0V (Figure 11 and Figure 12), RBYP = 3V	2	5	8	ns
t_r	Transition Time-Rise/Fall		CD = RBYP = 0V, T/$\overline{R}$ = 3V (Figure 2 and Figure 4) [2]	1	2	3.5	ns
t_f	20% to 80%			1	2	4	
SR	Slew Rate is calculated from 1.3V to 1.8V		CD = RBYP = 0V, T/$\overline{R}$ = 3V (Figure 2 and Figure 3) [2]		0.85	0.5	V/ns
t_{skew}	ACLK to Bn	Same Package	[3]		0.8	3	ns
	An to Bn	Same Package	[3]		0.8	3	ns
DRIVER TIMING REQUIREMENTS (Figure 5)							
t_S	An to ACLK	Set-up Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
t_H	ACLK to An	Hold Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	1			ns

(1) Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.
(2) Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5 V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1 V_{DC}.
(3) t_{skew} is an absolute value defined as differences seen in propagation delay between drivers in the same package with identical load conditions.

AC Electrical Characteristics[1] (continued)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{pw}	ACLK Pulse Width		CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
RECEIVER							
t_{PHL}	Bn to An	Propagation Delay	CD = T/$\overline{R}$ = 0V, LE = 3V	3	4.5	6	ns
t_{PLH}	Bypass Mode		(Figure 6 and Figure 7)	3	4.5	7.0	ns
t_{PHL}	LE to An	Propagation Delay	CD = T/$\overline{R}$ = 0V	3.5	5.5	10	ns
t_{PLH}	Latch Mode		(Figure 6 and Figure 8)	4.5	5.5	8.8	ns
t_{PLZ}	CD to An	Disable Time	LE = 3.0V	3	5	10	ns
t_{PZL}		Enable Time	Bn = 2.1V, T/$\overline{R}$ = 0V (Figure 9 and Figure 10)	2.5	6	8	ns
t_{PHZ}		Disable Time	LE = 3.0V	4	6	8.5	ns
t_{PZH}		Enable Time	Bn = 1.1V, T/$\overline{R}$ = 0V (Figure 9 and Figure 10)	2.5	5	8.5	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	LE = 3.0V, Bn = 2.1V	3	7.5	12	ns
t_{PZL}		Enable Time	CD = 0V (Figure 11 and Figure 12)	5	9.5	15	ns
t_{PHZ}		Disable Time	LE = 3.0V	3	6	9	ns
t_{PZH}		Enable Time	Bn = 1.1V, CD = 0V (Figure 9 and Figure 10)	3	6	9	ns
t_{skew}	LE to An	Same Package	[3]		0.5	3	ns
	Bn to An	Same Package	[3]		0.5	2.5	ns
RECEIVER TIMING REQUIREMENTS (Figure 8)							
t_S	Bn to LE	Set-up Time	CD = T/$\overline{R}$ = 0V	3			ns
t_H	LE to Bn	Hold Time	CD = T/$\overline{R}$ = 0V	1			ns
t_{pw}	LE Pulse Width		CD = T/$\overline{R}$ = 0V	5			ns
PARAMETERS NOT TESTED							
C_{output}	Capacitance at Bn		[4]		5		pF
t_{NR}	Noise Rejection		[5]		1		ns

(4) The parameter is tested using TDR techniques described in P1194.0 BTL Backplane Design Guide.
(5) This parameter is tested during device characterization. The measurements revealed that the part will typically reject 1 ns pulse width.

PIN DESCRIPTION

Pin Name	Number of Pins	Input/ Output	Description
A0–A8	9	I/O	TTL TRI-STATE receiver output and driver input
ACLK	1	I	Clock input for latch
B0–B8	9	I/O	BTL receiver input and driver output
B0GND–B8GND	9	NA	Driver output ground reduces ground bounce due to high current switching of driver outputs. [1]
CD	1	I	Chip Disable
GND	2	NA	Ground reference for switching circuits.[2]
LE	1	I	Latch Enable

(1) The multiplicity of grounds reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.
(2) Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5 V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1 V_{DC}.

PIN DESCRIPTION (continued)

Pin Name	Number of Pins	Input/ Output	Description
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (3)
NC	5	NA	No Connect
QGND	1	NA	Ground reference for receiver input bandgap reference and non-switching circuits. (1)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits. (3)
RBYP	1	I	Register bypass enable
T/$\overline{R}$	1	I	Transmit/$\overline{\text{Receive}}$ — Transmit (An to Bn) Receive (Bn to An)
V_{CC}	2	NA	V_{CC} supply for switching circuits. (3)

(3) The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Truth Table(1)

CD	T/$\overline{R}$	LE	RBYP	ACK	An	Bn
H	X	X	X	X	Z	H
L	H	X	H	X	L	H
L	H	X	H	X	H	L
L	H	X	L	X	X	Bn_0
L	H	X	L	L-H	H	L
L	H	X	L	L-H	L	H
L	L	H	X	X	H	L
L	L	H	X	X	L	H
L	L	L	X	X	An_0	X

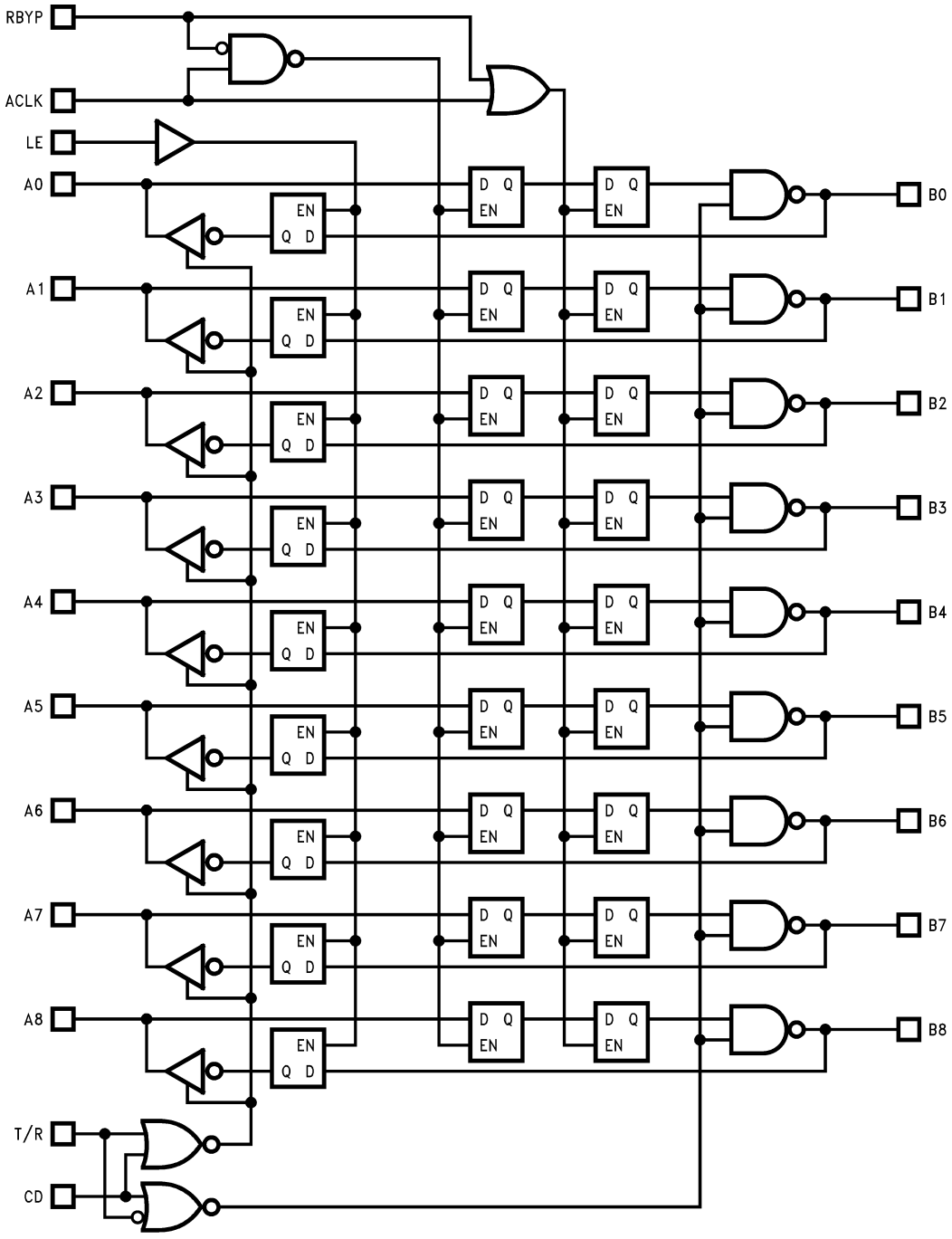
(1) X = High or low logic state
Z = High impedance state
L = Low state
H = High state
L-H = Low to high transition
An_0 = no change from previous state
Bn_0 = no change from previous state
BTL = high and low state are nominally 2.1V and 1.0V, respectively.
TTL = high and low state are nominally 2.4V and 0.5V, respectively.

Table 1. Package Thermal Characteristics(1)

Linear Feet per Minute Air Flow (LFPM)	θ_{JA} (°C/W) 44-Pin PQFP
0	82
225	68
500	60
900	53

(1) The above values are typical values and are different from the Absolute Maximum Rating values, which include guardbands.

Logic Diagram



Test Circuits and Timing Waveforms

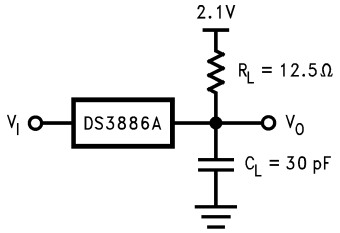


Figure 2. Driver Propagation Delay Set-up

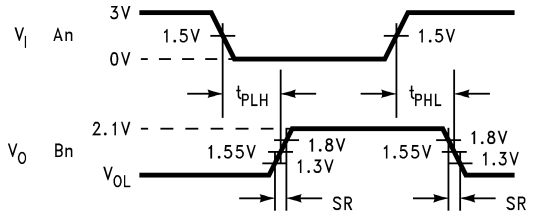


Figure 3. Driver: An to Bn, CD to An

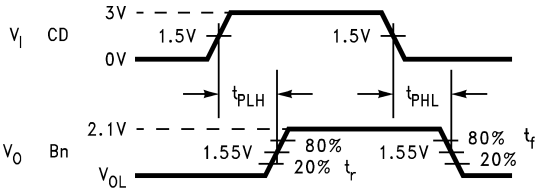


Figure 4. Driver: CD to Bn

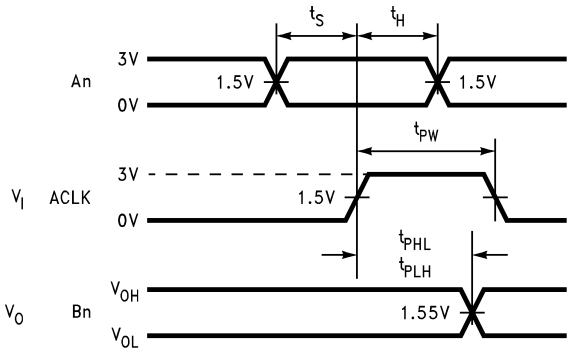


Figure 5. Driver: ACLK to Bn, t_S, t_H, t_{PW}

Table 2. Switch Position (1)

	t_{PLH}	t_{PHL}
S1	open	close

(1) Receiver Propagation Delay Set-up

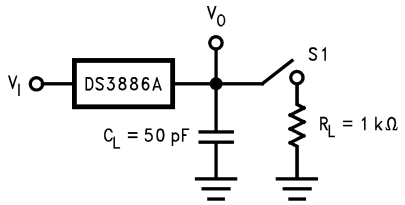


Figure 6. Receiver Propagation Delay Set-up

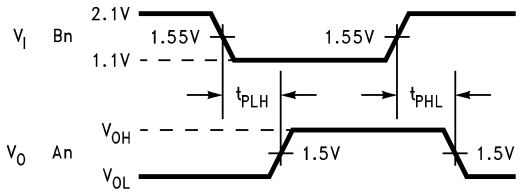


Figure 7. Receiver: Bn to An

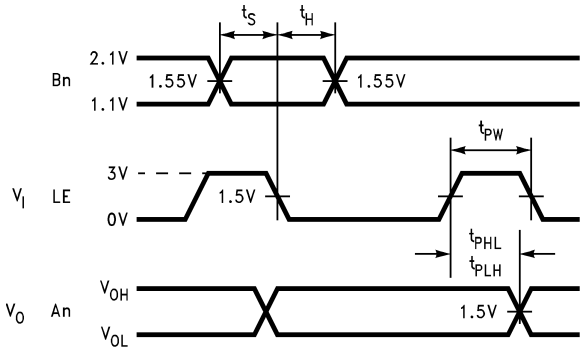


Figure 8. Receiver Enable/Disable Set-up

Table 3. Switch Position(1)

	t_{PZL}	t_{PZH}
	t_{PLZ}	t_{PHZ}
S1	close	open
S2	open	close

(1) Receiver: Enable/Disable Set-up

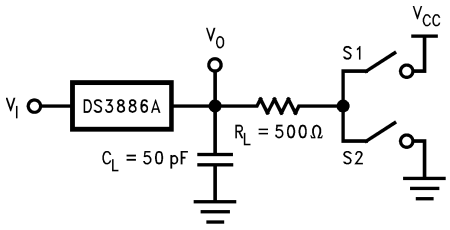


Figure 9. Receiver: Enable/Disable Set-up

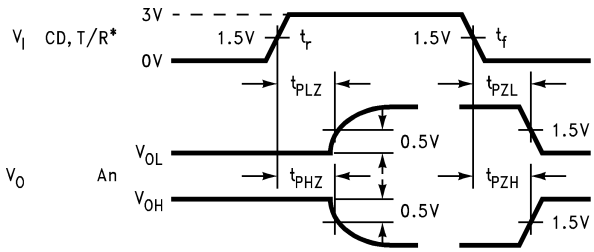


Figure 10. Receiver: CD to An, T/$\overline{R}$ to An (t_{PHZ} and t_{PZH} only)

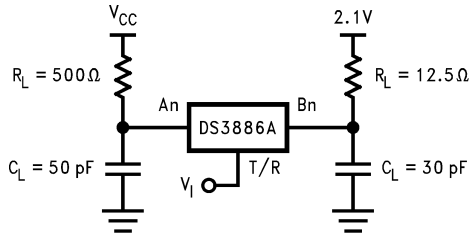


Figure 11. T/$\overline{R}$ to An, T/$\overline{R}$ to Bn

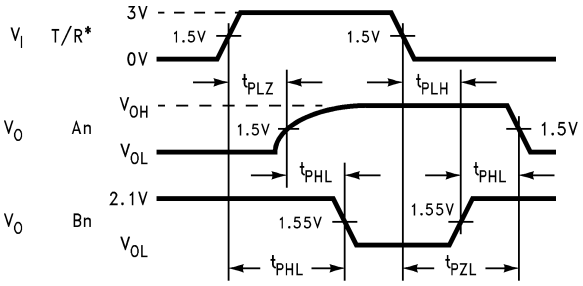


Figure 12. T/$\overline{R}$ to Bn (t_{PHL} and t_{PLH} only), T/$\overline{R}$ to An (t_{PZL} and t_{PLZ} only)

REVISION HISTORY

Changes from Revision C (February 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	10

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