National Semiconductor

DS35F86/DS34F86
RS-422/RS-423 Quad Line Receiver with TRI-STATE® Outputs

General Description

The DS34F86/DS35F86 RS-422/3 Quad Receiver features four independent receivers, which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. A PNP device buffers each output control lead to assure minimum loading for either logic one or logic zero inputs. In addition each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34F86/DS35F86 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F86/DS35F86 features lower power, extended temperature range, and improved specifications.

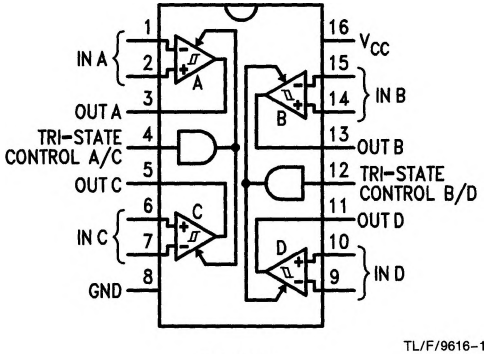
The DS34F86/DS35F86 offers optimum performance when used with the DS34F87/DS35F87 Quad Line Driver.

Features

- Military temperature range
- Low power version
- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs
- Fast propagation times 15 ns typical
- TTL compatible
- Single 5.0V supply voltage
- Output rise and fall times less than 20 ns
- Lead compatible and interchangeable with MC3486 and DS3486

Connection Diagram

16-Lead DIP



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Top View

Order Number DS34F86J or DS35F86J
See NS Package Number J16A

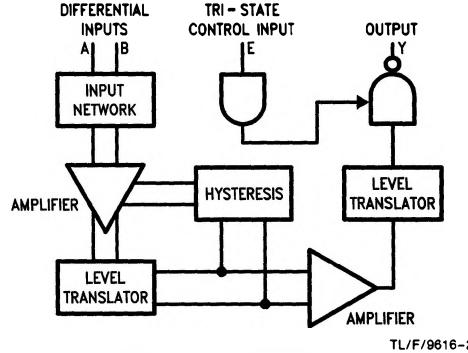

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FIGURE 1. Block Diagram

Function Table (Each Receiver)

Differential Inputs AB	Enable E	Output Y
$V_{ID} \leq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
Z = High Impedance (off)