

# DS26F32MQML Quad Differential Line Receivers

Check for Samples: DS26F32MQML

### **FEATURES**

- Input Voltage Range of ±7.0V (Differential or Common Mode) ±0.2V Sensitivity over the Input Voltage Range
- · High Input Impedance
- Operation from Single +5.0V Supply
- Input Pull-Down Resistor Prevents Output Oscillation on Unused Channels
- TRI-STATE Outputs, with Choice of Complementary Enables, for Receiving Directly onto a Data Bus

#### DESCRIPTION

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

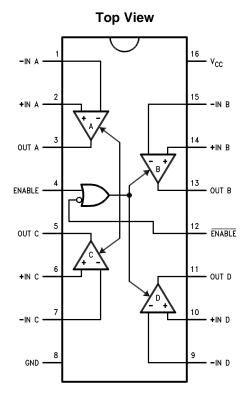
The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.



# **Connection Diagrams**



**Top View** В <u>∠</u> Z I  $\stackrel{\textstyle \scriptstyle Z}{\scriptstyle \scriptstyle I}$ 20 +IN B OUT B **ENABLE** NC NC ENABLE OUT C OUT D +IN C 9 GND ပ Ω Ω 2 Z -Z I <u>z</u>

Figure 2. 20-Lead LCCC Package See Package Number NAJ0020A

Figure 1. 16-Lead CDIP Package See Package Number NAC0016A, NFE0016A, or NAD0016A

Table 1. Function Table (Each Receiver)<sup>(1)</sup>

Differential Inputs	Ena	bles	Outputs		
$V_{ID} = (V_I +) - (V_I -)$	E	Ē	OUT		
V <sub>ID</sub> ≥ 0.2V	Н	X	Н		
	Х	L	Н		
V <sub>ID</sub> ≤ −0.2V	Н	X	L		
	Х	L	L		
X	L	Н	Z		

(1) H = High Level L = Low Level





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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# Absolute Maximum Ratings (1)

Storage Temperature Range	-65°C ≤ T <sub>A</sub> ≤ +150°C					
Operating Temperature Range	-55°C ≤ T <sub>A</sub> ≤ +125°C					
Lead Temperature (soldering, 60 sec)	300°C					
Supply Voltage	7.0V					
Common Mode Voltage Range	±25V					
Differential Input Voltage	±25V					
Enable Voltage	7.0V					
Output Sink Current	50 mA					
Maximum Power Dissipation (P <sub>D max</sub> at 25°C) <sup>(2)</sup> , <sup>(3)</sup> 500 mW						
Thermal Resistance						
$\theta_{JA}$						
NFE0016A package	100°C/W					
NAD0016A package	142°C/W					
NAJ0020A package	87°C/W					
$\theta_{JC}$						
Junction-to- case	See MIL-STD-1835					

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) Derate J package 10.0mW/°C above +25°C, derate W package 7.1mW/°C above +25°C, derate E package 11.5mW/°C above +25°C.
- (3) Power dissipation must be externally controlled at elevated temperatures.

# **Recommended Operating Range**

Operating Temperature	-55°C ≤ T <sub>A</sub> ≤ +125°C
Supply Voltage	4.5V to 5.5V

#### **Table 2. Radiation Features**

DS26F32MJRQMLV	100 krads (Si)
DS26F32MWRQMLV	100 krads (Si)
DS26F32MWGRQMLV	100 krads (Si)

# Table 3. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C		
1	Static tests at	25		
2	Static tests at	125		
3	Static tests at	-55		
4	Dynamic tests at	25		
5	Dynamic tests at	125		
6	Dynamic tests at	-55		
7	Functional tests at	25		
8A	Functional tests at	125		
8B	Functional tests at	-55		
9	Switching tests at	25		
10	Switching tests at	125		
11	Switching tests at	-55		
12	Settling time at	25		
13	Settling time at	125		
14	Settling time at	-55		

Product Folder Links: DS26F32MQML

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# **DS26F32 Electrical Characteristics DC Parameters**

The following conditions apply, unless otherwise specified.

DC:  $V_{CC} = 5V^{(1)}$ 

Parameter		Test Conditions Not		Min	Max	Units	Sub- groups	
I <sub>In</sub>	Input Current	Pin under test $V_{CC} = 4.5V$ , $V_I = 15V$ Other inputs -15V $\leq V_I \leq +15V$			2.3	mA	1, 2, 3	
		Pin under test $V_{CC} = 5.5V$ , $V_I = -15V$ Other inputs $-15V \le V_I \le +15V$			-2.8	mA	1, 2, 3	
I <sub>IL</sub>	Logical "0" Enable Current	$V_{CC} = 5.5V, V_{En} = 0.4V$			-360	μA	1, 2, 3	
I <sub>IH</sub>	Logical "1" Enable Current	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 2.7V			10	μA	1, 2, 3	
I <sub>I</sub>	Logical "1" Enable Current	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 5.5V			50	μA	1, 2, 3	
V <sub>IK</sub>	Input Clamp Voltage (Enable)	V <sub>CC</sub> = 4.5V, I <sub>I</sub> = -18mA			-1.5	V	1, 2, 3	
V <sub>OH</sub>	Logical "1" Output Voltage	$V_{CC} = 4.5V, \underline{I}_{OH} = -440\mu A,  \Delta V_I = 1V, VEn = .8 = V_{En}$		2.5		V	1, 2, 3	
V <sub>OL</sub>	Logical "0" Output Voltage	$V_{CC} = 4.5V, V\overline{En} = 0.8V = V_{En},$ $I_{OL} = 4mA, \Delta V_{I} = -1V$			0.4	V	1, 2, 3	
		$V_{CC} = 4.5V$ , $V\overline{En} = 8V = V_{En}$ , $I_{OL} = 8mA$ , $\Delta V_I = -1V$			.45	V	1, 2, 3	
I <sub>CC</sub>	Supply Current	$V_{CC} = 5.5 \underline{V}$ , All $V_I = Gnd$ , $V_{En} = 0V$ , $\overline{V}_{En} = 2V$			50	mA	1, 2, 3	
I <sub>OZ</sub>	Off-State Output Current	$V_{CC} = 5.5V, \underline{V}_{O} = 0.4V, V_{En} = 0.8V, \overline{V}_{En} = 2V$			-20	μΑ	1, 2, 3	
		$V_{CC} = 5.5V, V_{O} = 2.4V, V_{En} = 0.8V, V_{En} = 2V$			20	μΑ	1, 2, 3	
R <sub>I</sub>	Input Resistance	-15 ≤ V <sub>CM</sub> ≤ 15V		14		ΚΩ	1, 2, 3	
V <sub>Th</sub> Differential Input Voltage		$V_{CC} = 4.5V$ , $V_{OUT} = V_{OL}$ or $V_{OH}$ $-7V \le V_{CM} \le 7V$ , $V_{En} = \overline{V_{En}} = 2.5V$	(2)	-0.2	0.2	V	1, 2, 3	
		$V_{CC} = 5.5V, V_{OUT} = V_{OL} \text{ or } V_{OH} = -7V \le V_{CM} \le 7V, V_{En} = V_{En} = 2.5V$	(2)	-0.2	0.2	V	1, 2, 3	
V <sub>IL</sub>	Logical "0" Input Voltage (Enable)	V <sub>CC</sub> = 5.5V	(2)		0.8	V	1, 2, 3	
V <sub>IH</sub>	Logical "1" Input Voltage (Enable)	V <sub>CC</sub> = 4.5V	(2)	2.0		V	1, 2, 3	
I <sub>SC Min</sub>	Output Short Circuit Current	$V_{CC} = 4.5V$ , $V_O = 0V$ , $\Delta V_I = 1V$		-15		mA	1, 2, 3	
I <sub>SC Max</sub>	Output Short Circuit Current	$V_{CC} = 5.5V$ , $V_O = 0V$ , $\Delta V_I = 1V$			-85	mA	1, 2, 3	

<sup>(1)</sup> Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A

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<sup>(2)</sup> Parameter tested go-no-go only.



### **DS26F32 Electrical Characteristics AC Parameters**

The following conditions apply, unless otherwise specified.

AC:  $V_{CC} = 5V$  (1)

	Parameter	Test Conditions	Notes	Min	Max	Units	Sub- groups
t <sub>PLH</sub>		C <sub>L</sub> = 50pF	(2)		23	nS	9
			(2)		31	nS	10, 11
		C <sub>L</sub> = 15pF	(3)		22	nS	9
			(3)		30	nS	10, 11
PHL	C <sub>L</sub> = 50pF	(2)		23	nS	9	
			(2)		31	nS	10, 11
		C <sub>L</sub> = 15pF	(3)		22	nS	9
			(3)		30	nS	10, 11
t <sub>PZH</sub> Enable Time	Enable Time	C <sub>L</sub> = 50pF	(2)		18	nS	9
			(2)		29	nS	10, 11
		$C_L = 15pF$	(3)		16	nS	9
			(3)		27	nS	10, 11
t <sub>PZL</sub>	Enable Time	C <sub>L</sub> = 50pF	(2)		20	nS	9
			(2)		29	nS	10, 11
		C <sub>L</sub> = 15pF	(3)		18	nS	9
			(3)		27	nS	10, 11
t <sub>PHZ</sub>	Disable Time	C <sub>L</sub> = 50pF	(2)		55	nS	9
			(2)		62	nS	10, 11
		$C_L = 5pF$	(3)		20	nS	9
			(3)		27	nS	10, 11
t <sub>PLZ</sub>	Disable Time	C <sub>L</sub> = 50pF	(2)		30	nS	9
			(2)		42	nS	10, 11
		$C_L = 5pF$	(3)		18	nS	9
			(3)		30	nS	10, 11

<sup>(1)</sup> Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A

#### **DS26F32 Electrical Characteristics DC Drift Parameters**

This section applies to -QMLV devices only. Devices shall be read & recorded at  $T_A = 25^{\circ}$ C before and after each burn-in and shall not change by more than the limits indicated. The delta rejects shall be included in the PDA calculation.

	Parameter	Test Conditions	Notes	Min	Max	Units	Sub- groups
V <sub>OH</sub>	Logical "1" Output Voltage	$V_{CC} = 4.5V, \underline{I_{OH}} = -440\mu A, \\ \Delta V_{I} = 1V, VEn = 0.8V = V_{En}$		-250	250	mV	1
V <sub>OL</sub> Logical "0" Output Voltage		$V_{CC} = 4.5V, I_{OL} = 4mA, \\ \Delta V_{I} = -1V, VEn = 0.8V = V_{En}$		-45	45	mV	1
		$V_{CC} = 4.5V, I_{OL} = 8mA, \\ \Delta V_{I} = -1V, VEn = 0.8V = V_{En}$		-45	45	mV	1
I	Input Current	Pin under test $V_{CC} = 4.5V$ , $V_{I} = 15V$ Other inputs -15V $\leq V_{I} \leq$ +15V		-0.28	0.28	mA	1
		Pin under test $V_{CC} = 5.5V$ , $V_I = -15V$ Other inputs $-15V \le V_I \le +15V$		-0.28	0.28	mA	1

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<sup>(2)</sup> Tested at 50pF, system capacitance exceeds 5pF to 15pF.

<sup>(3)</sup> Tested at 50pF guarantees limit at 15pF & 5pF.



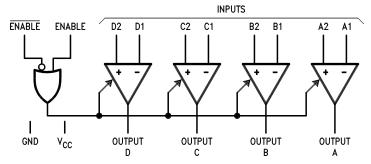
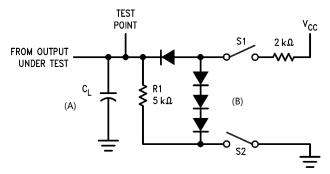


Figure 3. Logic Symbol



C L includes probe and jig capacitance.

- A. Parameter tested go-no-go only.
- B. Tested at 50pF guarantees limit at 15pF and 5pF.

Figure 4. Load Test Circuit for Three-State Outputs

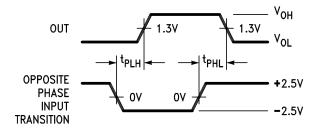


Diagram shown for ENABLE Low.

S1 and S2 of Load Circuit are closed except where shown.

Pulse Generator of all Pulses: Rate  $\leq$  1.0 MHz,  $Z_O = 50\Omega$ ,  $t_f \leq$  6.0 ns,  $t_f \leq$  6.0 ns.

Figure 5. Propagation Delay

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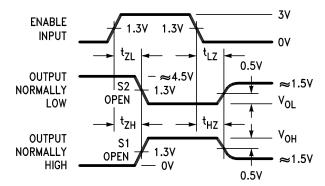


Diagram shown for  $\overline{\text{ENABLE}}$  Low.

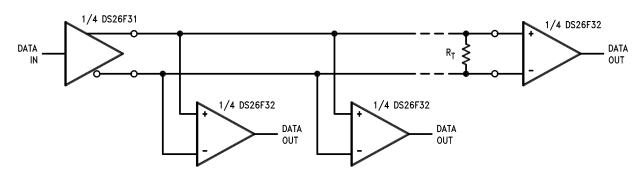
S1 and S2 of Load Circuit are closed except where shown.

Pulse Generator of all Pulses: Rate ≤ 1.0 MHz,  $Z_O$  = 50 $\Omega$ ,  $t_r$  ≤ 6.0 ns,  $t_f$  ≤ 6.0 ns.

All diodes are IN916 or IN3064.

Figure 6. Enable and Disable Times

### TYPICAL APPLICATION



**Table 4. Revision History** 

Released	Revision	Section	Originator	Changes
03/01/06	А	New Release, Corporate format		1 MDS data sheet converted into one Corp. data sheet format. MNDS26F32M-X-RH Rev 0C0 will be archived.

Product Folder Links: DS26F32MQML





24-Jan-2013

# **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
5962-7802005M2A	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM		DS26F32ME/ 883 Q 5962-78020 05M2A ACO 05M2A >T	Samples
5962-7802005MFA	ACTIVE	CLGA	NAD	16	19	TBD	CU SNPB	Level-1-NA-UNLIM		DS26F32MW /883 Q 5962-78020 05MFA ACO 05MFA >T	Samples
5962R7802005VEA	ACTIVE	CDIP	NFE	16	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MJRQMLV 5962R7802005VEA Q	Samples
5962R7802005VFA	ACTIVE	CLGA	NAD	16	19	TBD	CU SNPB	Level-1-NA-UNLIM		DS26F32MWR QMLV Q 5962R78020 05VFA ACO 05VFA >T	Samples
DS26F32ME/883	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM		DS26F32ME/ 883 Q 5962-78020 05M2A ACO 05M2A >T	Samples
DS26F32MJRQMLV	ACTIVE	CDIP	NFE	16	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MJRQMLV 5962R7802005VEA Q	Samples
DS26F32MW/883	ACTIVE	CLGA	NAD	16	19	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MW /883 Q 5962-78020 05MFA ACO 05MFA >T	Samples
DS26F32MWRQMLV	ACTIVE	CLGA	NAD	16	19	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MWR QMLV Q 5962R78020 05VFA ACO 05VFA >T	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.





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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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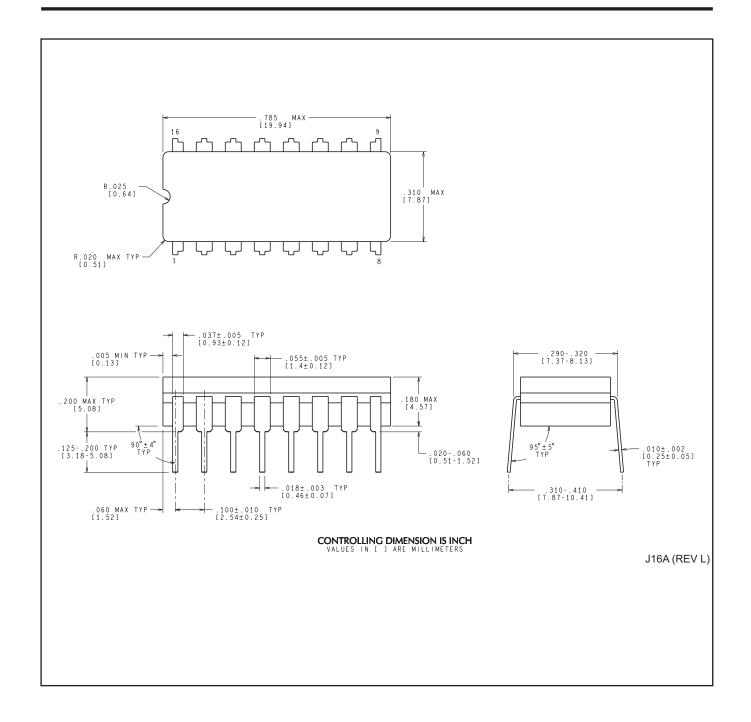
#### OTHER QUALIFIED VERSIONS OF DS26F32MQML, DS26F32MQML-SP:

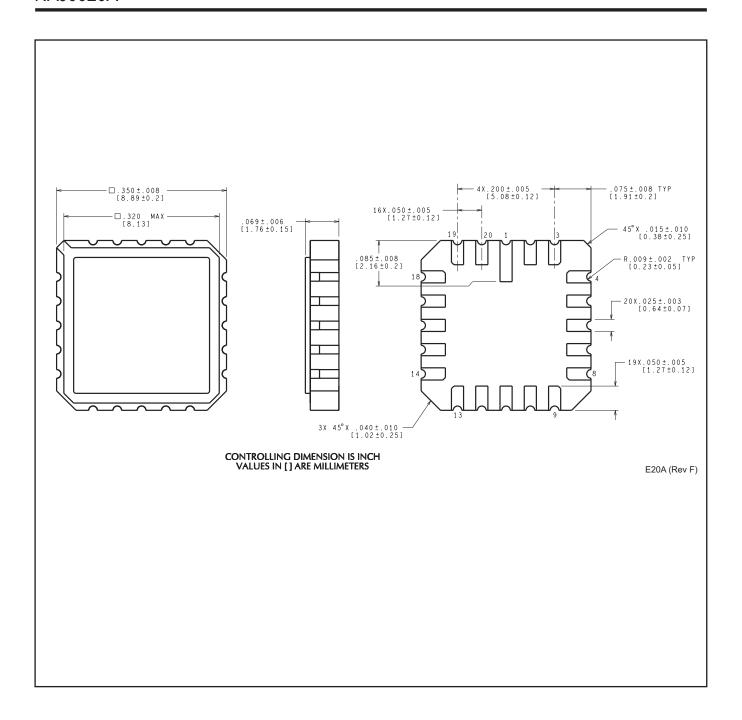
Military: DS26F32MQML

Space: DS26F32MQML-SP

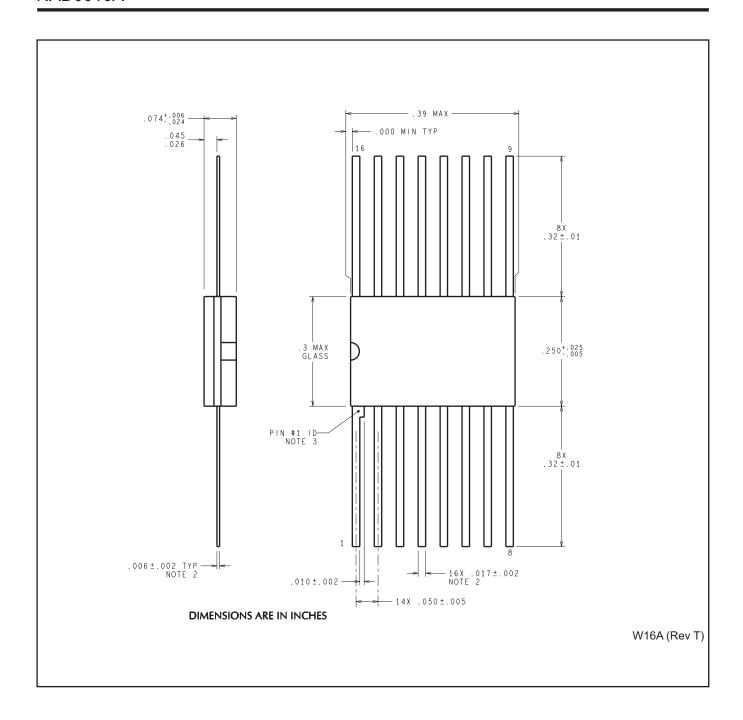
NOTE: Qualified Version Definitions:

- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application











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