DS25BR400 Quad 2.5 Gbps CML Transceiver with Transmit De-Emphasis and Receive Equalization

Check for Samples: DS25BR400

FEATURES

- **250 Mbps – 2.5 Gbps Low Jitter Operation**
- **Optional Fixed Input Equalization**
- **Selectable Output De-Emphasis**
- **Individual Loopback Controls**
- **On-Chip Termination**
- **+3.3V Supply**
- **Lead-Less WQFN-60 Pin Package**
  - **(9 mm x9 mm x0.8 mm, 0.5 mm Pitch)**
- **−40°C to +85°C Industrial Temperature Range**
- **6 kV ESD Rating, HBM**

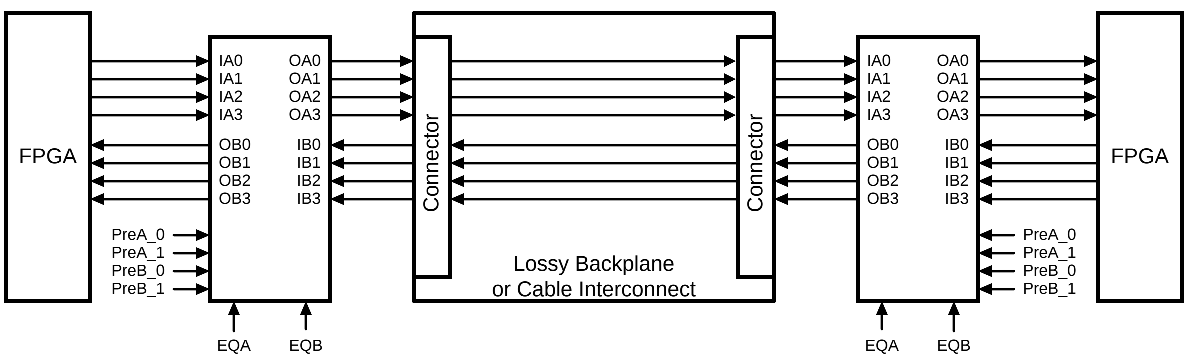
APPLICATIONS

- **Backplane or Cable Driver**
- **Signal Buffering and Repeating**

DESCRIPTION

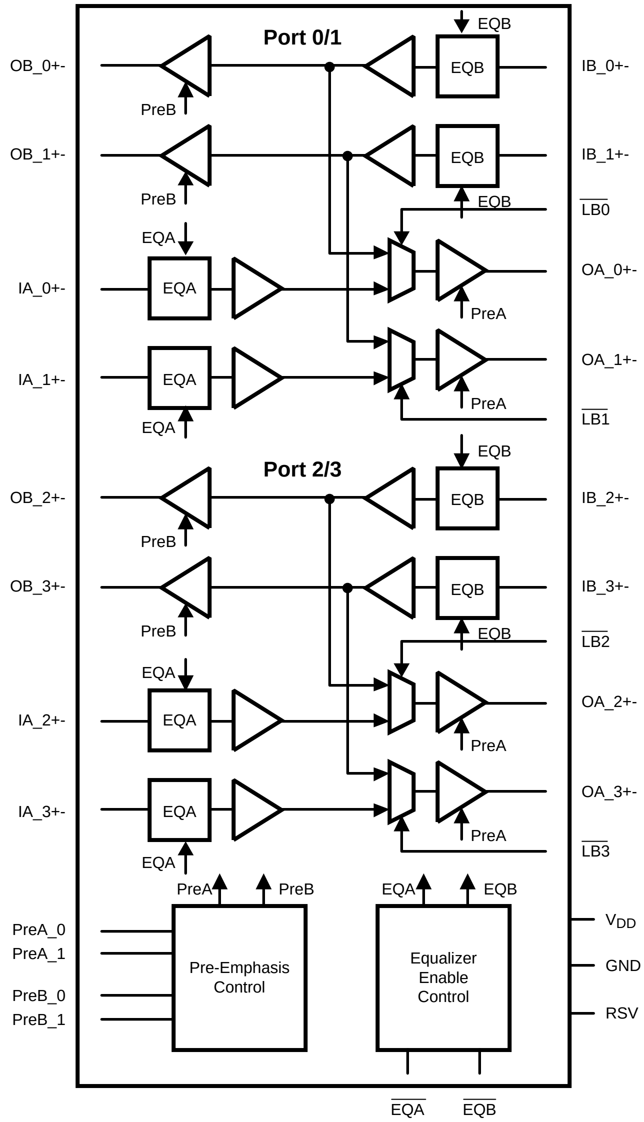
The DS25BR400 is a quad 250 Mbps – 2.5 Gbps CML transceiver, or 8-channel buffer, for use in backplane and cable applications. With operation down to 250 Mbps, the DS25BR400 can be used in applications requiring both low and high frequency data rates. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. The equalizers are enabled through two control pins. These control pins provide flexibility in applications where ISI distortion may vary from one direction to another. All output drivers have four selectable steps of de-emphasis to compensate for transmission loss. The de-emphasis blocks are also grouped in fours. In addition, the DS25BR400 also has loopback control capability on four channels. All the CML drivers have 50Ω termination to V_{CC}. All receivers are internally terminated with differential 100Ω.

Simplified Application Diagram



NOTE
All CML inputs and outputs must be AC coupled for optimal performance.

Functional Block Diagram



Connection Diagram

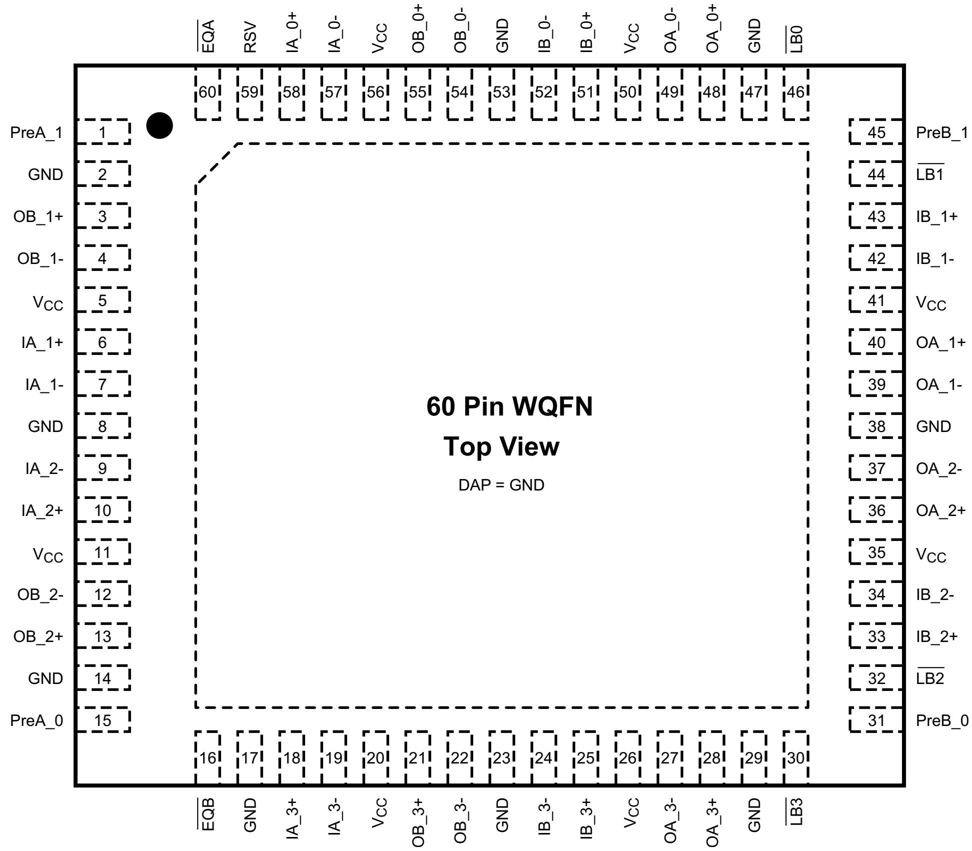


Figure 1. Leadless WQFN-60 Pin Package
(9 mm x 9 mm x 0.8 mm, 0.5 mm pitch)
See Package Number NKA0060A

Table 1. PIN DESCRIPTIONS

Pin Name	Pin Number	I/O (1)	Description
DIFFERENTIAL I/O			
IB_0+ IB_0−	51 52	I	Inverting and non-inverting differential inputs of port_0. IB_0+ and IB_0− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OA_0+ OA_0−	48 49	O	Inverting and non-inverting differential outputs of port_0. OA_0+ and OA_0− are connected to V_{CC} through a 50Ω resistor.
IB_1+ IB_1−	43 42	I	Inverting and non-inverting differential inputs of port_1. IB_1+ and IB_1− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OA_1+ OA_1−	40 39	O	Inverting and non-inverting differential outputs of port_1. OA_1+ and OA_1− are connected to V_{CC} through a 50Ω resistor.
IB_2+ IB_2−	33 34	I	Inverting and non-inverting differential inputs of port_2. IB_2+ and IB_2− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OA_2+ OA_2−	36 37	O	Inverting and non-inverting differential outputs of port_2. OA_2+ and OA_2− are connected to V_{CC} through a 50Ω resistor.
IB_3+ IB_3−	25 24	I	Inverting and non-inverting differential inputs of port_3. IB_3+ and IB_3− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OA_3+ OA_3−	28 27	O	Inverting and non-inverting differential outputs of port_3. OA_3+ and OA_3− are connected to V_{CC} through a 50Ω resistor.
IA_0+ IA_0−	58 57	I	Inverting and non-inverting differential inputs of port_0. IA_0+ and IA_0− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.

(1) I = Input, O = Output, P = Power

Table 1. PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O (1)	Description
OB_0+ OB_0−	55 54	O	Inverting and non-inverting differential outputs of port_0. OB_0+ and OB_0− are connected to V_{CC} through a 50Ω resistor.
IA_1+ IA_1−	6 7	I	Inverting and non-inverting differential inputs of port_1. IA_1+ and IA_1− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OB_1+ OB_1−	3 4	O	Inverting and non-inverting differential outputs of port_1. OB_1+ and OB_1− are connected to V_{CC} through a 50Ω resistor.
IA_2+ IA_2−	10 9	I	Inverting and non-inverting differential inputs of port_2. IA_2+ and IA_2− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OB_2+ OB_2−	13 12	O	Inverting and non-inverting differential outputs of port_2. OB_2+ and OB_2− are connected to V_{CC} through a 50Ω resistor.
IA_3+ IA_3−	18 19	I	Inverting and non-inverting differential inputs of port_3. IA_3+ and IA_3− are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8.
OB_3+ OB_3−	21 22	O	Inverting and non-inverting differential outputs of port_3. OB_3+ and OB_3− are connected to V_{CC} through a 50Ω resistor.
CONTROL (3.3V LVCMOS)			
$\overline{EQA}$	60	I	This pin is active LOW. A logic LOW at $\overline{EQA}$ enables equalization for input channels IA_0±, IA_1±, IA_2±, and IA_3±. By default, this pin is internally pulled high and equalization is disabled.
$\overline{EQB}$	16	I	This pin is active LOW. A logic LOW at $\overline{EQB}$ enables equalization for input channels IB_0±, IB_1±, IB_2±, and IB_3±. By default, this pin is internally pulled high and equalization is disabled.
PreA_0 PreA_1	15 1	I	PreA_0 and PreA_1 select the output de-emphasis levels (OA_0±, OA_1±, OA_2±, and OA_3±). PreA_0 and PreA_1 are internally pulled high. Please see Table 3 for de-emphasis levels.
PreB_0 PreB_1	31 45	I	PreB_0 and PreB_1 select the output de-emphasis levels (OB_0±, OB_1±, OB_2±, and OB_3±). PreB_0 and PreB_1 are internally pulled high. Please see Table 3 for de-emphasis levels.
$\overline{LB0}$	46	I	This pin is active LOW. A logic LOW at $\overline{LB0}$ enables the internal loopback path from IB_0± to OA_0±. $\overline{LB0}$ is internally pulled high. Please see Table 2 for more information.
$\overline{LB1}$	44	I	This pin is active LOW. A logic LOW at $\overline{LB1}$ enables the internal loopback path from IB_1± to OA_1±. $\overline{LB1}$ is internally pulled high. Please see Table 2 for more information.
$\overline{LB2}$	32	I	This pin is active LOW. A logic LOW at $\overline{LB2}$ enables the internal loopback path from IB_2± to OA_2±. $\overline{LB2}$ is internally pulled high. Please see Table 2 for more information.
$\overline{LB3}$	30	I	This pin is active LOW. A logic LOW at $\overline{LB3}$ enables the internal loopback path from IB_3± to OA_3±. $\overline{LB3}$ is internally pulled high. Please see Table 2 for more information.
RSV	59	I	Reserve pin to support factory testing. This pin can be left open, tied to GND, or tied to GND through an external pull-down resistor.
POWER			
V_{CC}	5, 11, 20, 26, 35, 41, 50, 56	P	V_{CC} = 3.3V ± 5%. Each V_{CC} pin should be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.
GND	2, 8, 14, 17, 23, 29, 38, 47, 53	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	DAP is the metal contact at the bottom side, located at the center of the WQFN-60 pin package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.

Functional Description

The DS25BR400 is a quad 250 Mbps – 2.5 Gbps CML transceiver, or 8-channel buffer, for use in backplane and cable applications. The DS25BR400 is not designed to operate with data rates below 250 Mbps or with a DC bias applied to the CML inputs or outputs. Most high speed links are encoded for DC balance and have been defined to include AC coupling capacitors allowing the DS25BR400 to be directly inserted into the datapath without any limitation. The ideal AC coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC coupling capacitor value ranges between 100 and 1000nF, some specifications with scrambled data may require a larger capacitor for optimal performance. To reduce unwanted parasitics around and within the AC coupling capacitor, a body size of 0402 is recommended. Figure 7 shows the AC coupling capacitor placement in an AC test circuit.

To compensate for the high frequency losses incurred during signal transmission in cables and backplanes the DS25BR400 employs input and output signal conditioning. Each input stage has a fixed equalizer and all output drivers have four selectable steps of de-emphasis to reduce deterministic jitter on the serial link. All the CML output drivers have 50Ω termination to V_{CC}. All receiver inputs are internally terminated with differential 100Ω impedance.

Table 2. Logic Table for Loopback Controls

$\overline{\text{LB0}}$	**Loopback Function**
0	Enable loopback from IB_0± to OA_0±.
1 (default)	Normal mode. Loopback disabled.
$\overline{\text{LB1}}$	**Loopback Function**
0	Enable loopback from IB_1± to OA_1±.
1 (default)	Normal mode. Loopback disabled.
$\overline{\text{LB2}}$	**Loopback Function**
0	Enable loopback from IB_2± to OA_2±.
1 (default)	Normal mode. Loopback disabled.
$\overline{\text{LB3}}$	**Loopback Function**
0	Enable loopback from IB_3± to OA_3±.
1 (default)	Normal mode. Loopback disabled.

Table 3. De-Emphasis Controls

PreA_[1:0]	Default VOD Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	De-Emphasis in dB (VODPE/VODB)
0 0	1200	1200	0
0 1	1200	850	−3
1 0	1200	600	−6
1 1 (Default)	1200	426	−9
PreB_[1:0]	**Default VOD Level in mV_{PP} (VODB)**	**De-Emphasis Level in mV_{PP} (VODPE)**	**De-Emphasis in dB (VODPE/VODB)**
0 0	1200	1200	0
0 1	1200	850	−3
1 0	1200	600	−6
1 1 (Default)	1200	426	−9

Output De-Emphasis

De-emphasis is the conditioning function for use in compensating against backplane transmission loss. The DS25BR400 provides four steps of de-emphasis ranging from 0, −3, −6 and −9 dB, user-selectable dependent on the loss profile of the backplane. Figure 2 shows a driver de-emphasis waveform. The de-emphasis duration is nominal 200 ps, corresponding to 50% bit-width at 2.5 Gbps. The de-emphasis levels of switch-side and line-side can be individually programmed.

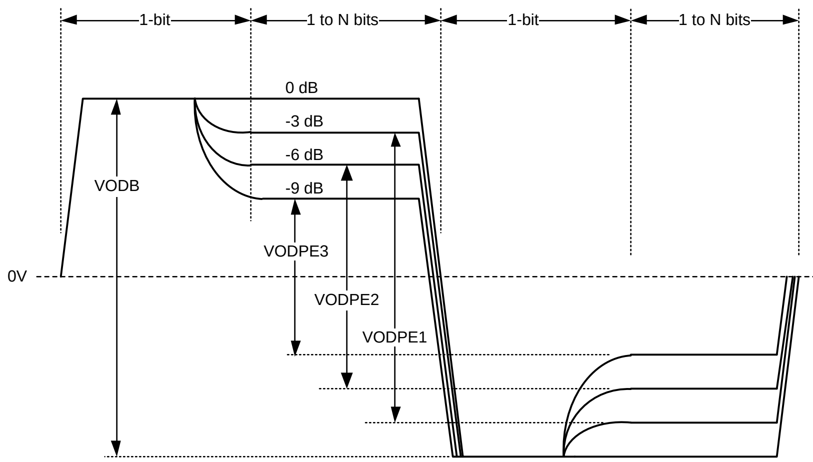


Figure 2. Driver De-Emphasis Differential Waveform (showing all 4 de-emphasis steps)

Input Equalization

Each differential input of the DS25BR400 has a fixed equalizer front-end stage. Input group A and B can be individually enabled and disabled. It is designed to provide fixed equalization for short board traces with transmission losses of approximately 5 dB between 375 MHz to 1.875 GHz. Programmable de-emphasis together with input equalization ensures an acceptable eye opening for a 40-inch FR-4 backplane.

The differential input equalizer for inputs on Channel A and inputs on Channel B can be bypassed by using $\overline{EQA}$ and $\overline{EQB}$, respectively. By default, the equalizers are internally pulled high and disabled. Therefore, $\overline{EQA}$ and $\overline{EQB}$ must be asserted LOW to enable equalization.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})	−0.3V to 4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} +0.3V)
CML Input/Output Voltage	−0.3V to (V_{CC} +0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature Soldering, 4 sec	+260°C
Thermal Resistance, θ_{JA}	22.3°C/W
Thermal Resistance, θ_{JC}	3.2°C/W
Thermal Resistance, Φ_{JB}	10.3°C/W
ESD Ratings (3)	
HBM	6kV
CDM	1kV
MM	350V

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. For guaranteed specifications and the test conditions, see Electrical Characteristics. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) ESD tests conform to the following standards:
Human Body Model (HBM) applicable standard: MIL-STD-883, Method 3015.7
Machine Model (MM) applicable standard: JESD22-A115-A (ESD MM std. of JEDEC)
Field -Induced Charge Device Model (CDM) applicable standard: JESD22-C101-C (ESD FICDM std. of JEDEC)

Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage (V_{CC}-GND)	3.135	3.3	3.465	V
Supply Noise Amplitude 10 Hz to 2 GHz			100	mV_{PP}
Ambient Temperature	−40		+85	°C
Case Temperature			100	°C

Electrical Characteristics(1)(2)

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ (3)	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC} +0.3	V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	−10		10	μA
I_{IL}	Low Level Input Current	V_{IN} = GND	75	94	124	μA
R_{PU}	Pull-High Resistance			35		kΩ
RECEIVER SPECIFICATIONS						
V_{ID}	Differential Input Voltage Range	AC Coupled Differential Signal. Below 1.25 Gb/s At 1.25 Gbps–3.125 Gbps Above 3.125 Gbps This parameter is not production tested.	100 100 100		1750 1560 1200	mV_{P-P} mV_{P-P} mV_{P-P}
V_{ICM}	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground.		1.3		V
R_{ITD}	Input Differential Termination	On-chip differential termination between IN+ or IN−. Figure 8	84	100	116	Ω
DRIVER SPECIFICATIONS						
VODB	Output Differential Voltage Swing without De-Emphasis	R_L = 100Ω ±1% PreA_1 = 0; PreA_0 = 0 PreB_1 = 0; PreB_0 = 0 Driver de-emphasis disabled. Running K28.7 pattern at 2.5 Gbps. (Figure 7)	1000	1200	1400	mV_{P-P}
V_{PE}	Output De-Emphasis Voltage Ratio 20*log(VODPE/VODB)	R_L = 100Ω ±1% Running K28.7 pattern at 2.5 Gbps PreX_[1:0] = 00 PreX_[1:0] = 01 PreX_[1:0] = 10 PreX_[1:0] = 11 X = A/B channel de-emphasis drivers (Figure 2 / Figure 7)		0 −3 −6 −9		dB dB dB dB
t_{PE}	De-Emphasis Width	Tested at −9 dB de-emphasis level, PreX[1:0] = 11 X = A/B channel de-emphasis drivers See Figure 6 on measurement condition.	125	200	250	ps
R_{OTSE}	Output Termination	On-chip termination from OUT+ or OUT− to V_{CC}	42	50	58	Ω
R_{OTD}	Output Differential Termination	On-chip differential termination between OUT+ and OUT−		100		Ω

(1) K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000}K28.5 pattern is a 20-bit repeating pattern of +K28.5 and −K28.5 code groups {110000 0101 001111 1010}
(2) IN+ and IN− are generic names that refer to one of the many pairs of complementary inputs of the DS25BR400. OUT+ and OUT− are generic names that refer to one of the many pairs of the complementary outputs of the DS25BR400. Differential input voltage V_{ID} is defined as |IN+ – IN−|. Differential output voltage V_{OD} is defined as |OUT+ – OUT−|.
(3) Typical specifications are at T_A = 25 °C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Electrical Characteristics(1)(2) (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ (3)	Max	Units
ΔR_{OTSE}	Mis-Match in Output Termination Resistors	Mis-match in output termination resistors			5	%
V_{OCM}	Output Common Mode Voltage			2.7		V
POWER DISSIPATION						
P_D	Power Dissipation	V_{DD} = 3.465V All outputs terminated by 100Ω ±1%. PreB_[1:0] = 0, PreA_[1:0] = 0 Running PRBS 2^7-1 pattern at 2.5 Gbps			1.3	W
AC CHARACTERISTICS (4)						
t_R	Differential Low to High Transition Time	Measured with a clock-like pattern at 2.5 Gbps, between 20% and 80% of the differential output voltage. De-emphasis disabled. Transition time is measured with the fixture shown in Figure 7 adjusted to reflect the transition time at the output pins.		80		ps
t_F	Differential High to Low Transition Time			80		ps
t_{PLH}	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output.			1	ns
t_{PHL}	Differential High to Low Propagation Delay				1	ns
t_{SKP}	Pulse Skew	$\|t_{PHL}–t_{PLH}\|$			20	ps
t_{SKO}	Output Skew (5)	Difference in propagation delay between channels on the same part (Channel-to-Channel Skew)			100	ps
t_{SKPP}	Part-to-Part Skew (5)	Difference in propagation delay between devices across all channels operating under identical conditions			165	ps
t_{LB}	Loopback Delay Time	Delay from enabling loopback mode to signals appearing at the differential outputs Figure 5			4	ns
RJ	Device Random Jitter (6)	At 0.25 Gbps At 1.5 Gbps At 2.5 Gbps Alternating-10 pattern. De-emphasis disabled. (Figure 7)			2 2 2	ps rms ps rms ps rms
DJ	Device Deterministic Jitter (7)	At 0.25 Mbps, PRBS7 pattern At 1.5 Gbps, K28.5 pattern At 2.5 Gbps, K28.5 pattern At 2.5 Gbps, PRBS7 pattern De-emphasis disabled. (Figure 7)			25 25 25 25	ps pp ps pp ps pp ps pp
DR	Data Rate (8)	Alternating-10 pattern	0.25		2.5	Gbps

(4) All CML Inputs and Outputs must be AC coupled for optimal jitter performance.
(5) t_{SKO} is the magnitude difference in propagation delays between all data paths on one device. This is channel-to-channel skew. t_{SKPP} is the worst case difference in propagation delay across multiple devices on all channels and operating under identical conditions. For example, for two devices operating under the same conditions, t_{SKPP} is the magnitude difference between the shortest propagation delay measurement on one device to the longest propagation delay measurement on another device.
(6) Device output random jitter is a measurement of random jitter contributed by the device. It is derived by the equation SQRT[$(RJ_{OUT})^2$ – $(RJ_{IN})^2$], where RJ_{OUT} is the total random jitter measured at the output of the device in ps(rms), RJ_{IN} is the random jitter of the pattern generator driving the device. Below 400 Mbps, system jitter and device jitter could not be separated. The 250 Mbps specification includes system random jitter. Please see Figure 7 for the AC test circuit.
(7) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ_{OUT} - DJ_{IN}), where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in ps(p-p). DJ_{IN} is the peak-to-peak deterministic jitter at the input of the test board. Please see Figure 7 for the AC test circuit.
(8) This parameter is guaranteed by design and/or characterization and is not tested in production.

TIMING DIAGRAMS

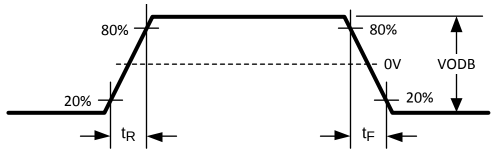


Figure 3. Driver Output Transition Time

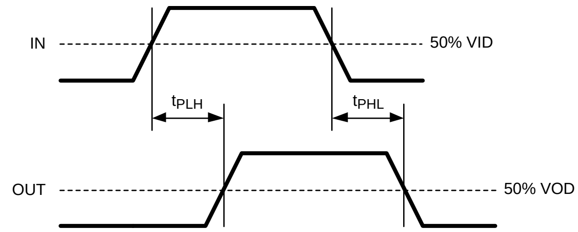


Figure 4. Propagation Delay

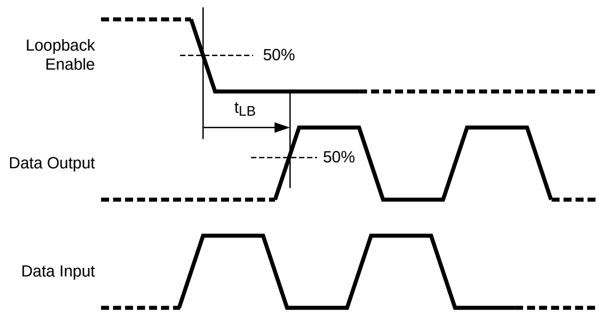


Figure 5. Loopback Delay Timing

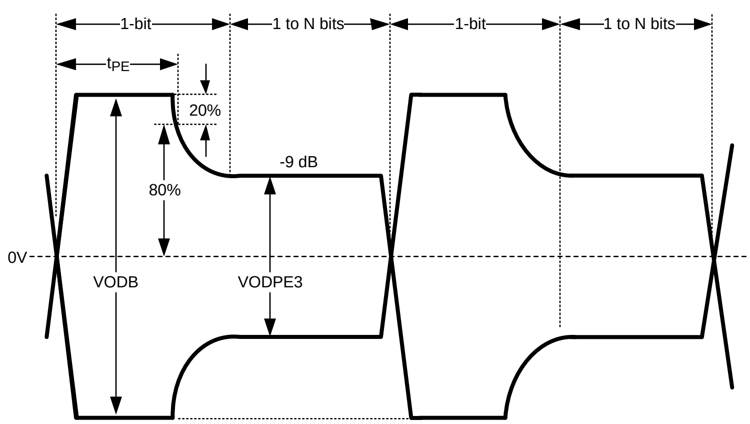


Figure 6. Output De-Emphasis Duration

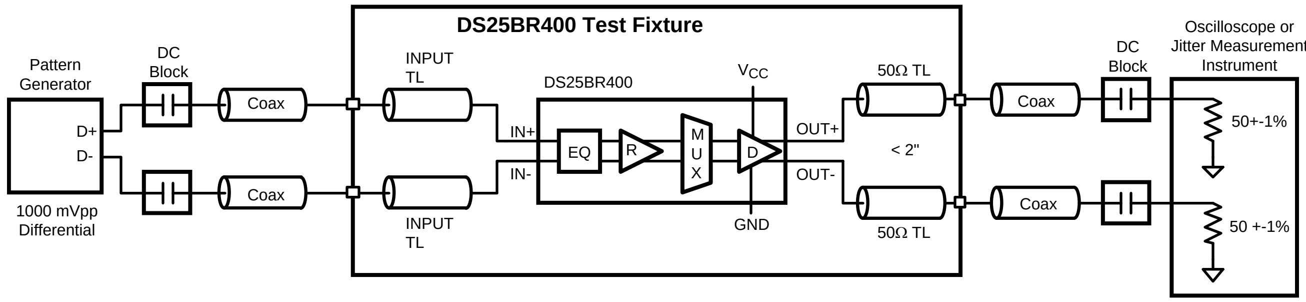


Figure 7. AC Test Circuit

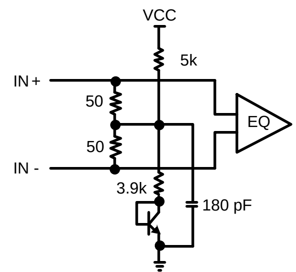


Figure 8. Receiver Input Termination

REVISION HISTORY

Changes from Revision H (February 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS25BR400TSQ	ACTIVE	WQFN	NKA	60	250	TBD	Call TI	Call TI	-40 to 85		Samples
DS25BR400TSQ/NOPB	ACTIVE	WQFN	NKA	60	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	DS25BR400 TSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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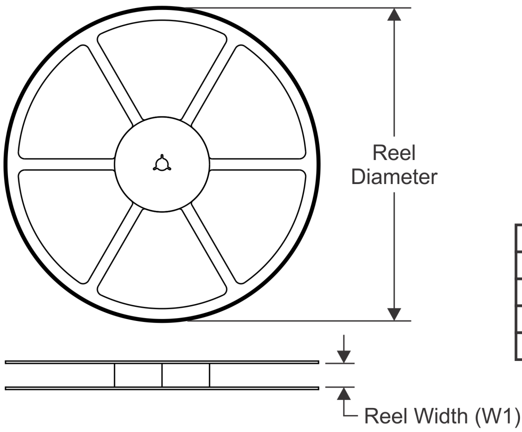
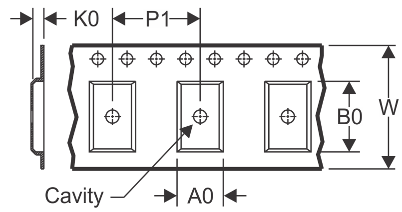
TAPE AND REEL INFORMATION

REEL DIMENSIONS

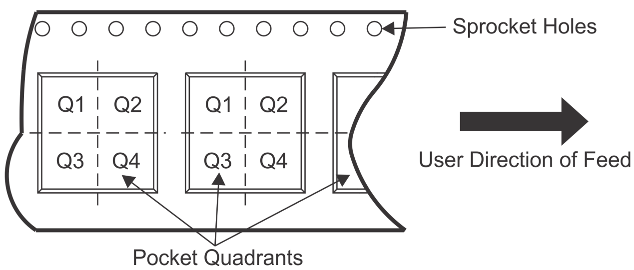


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

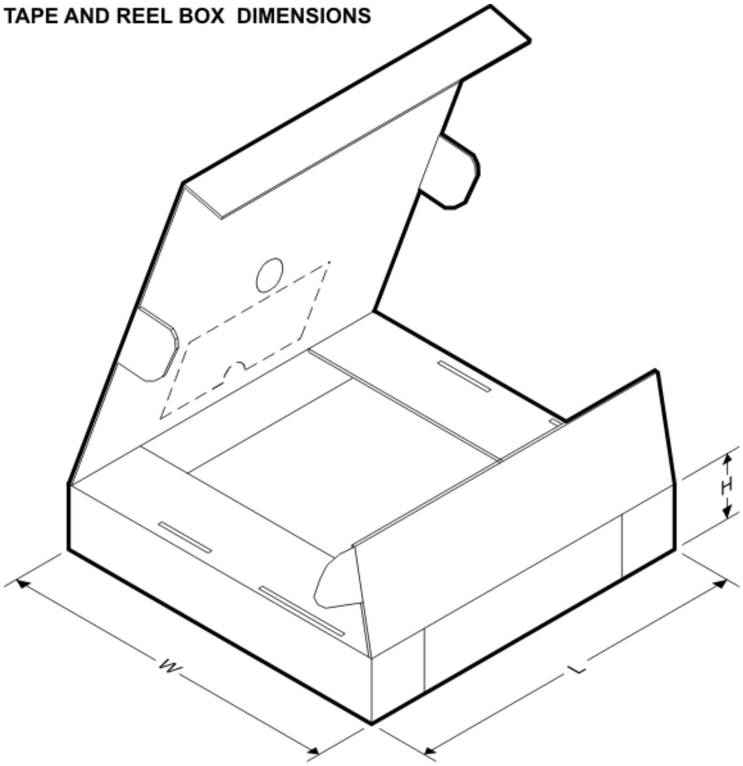
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR400TSQ/NOPB	WQFN	NKA	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

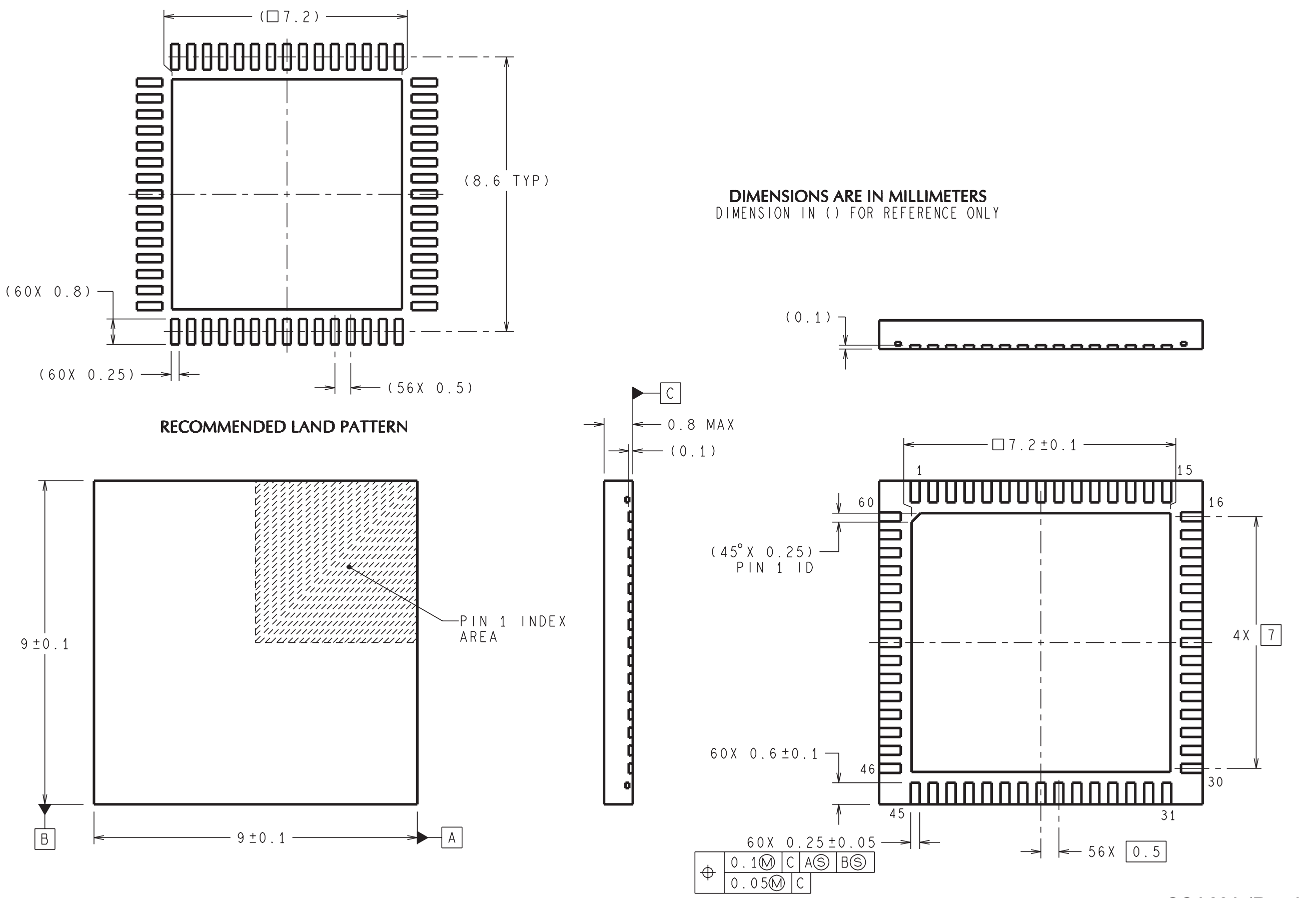
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR400TSQ/NOPB	WQFN	NKA	60	250	213.0	191.0	55.0

NKA0060A



SQA60A (Rev A)

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