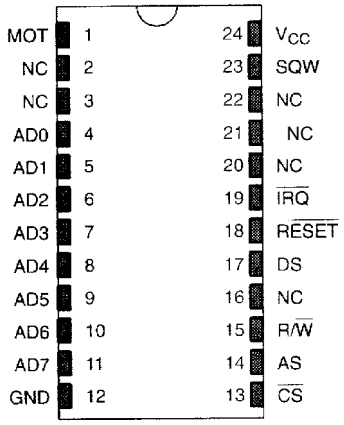
DS12887
Real-Time Clock

www.maxim-ic.com

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin-compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap-year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12-hour or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general-purpose RAM
- Programmable square-wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122ms to 500ms
  - End-of-clock update cycle
- Underwriters Laboratory (UL) recognized

PIN ASSIGNMENT (Top View)



DS12887 24 PDIP Module (700mil)

Package Dimension Information

http://www.maxim-ic.com/TechSupport/DallasPackInfo.htm

PIN DESCRIPTION

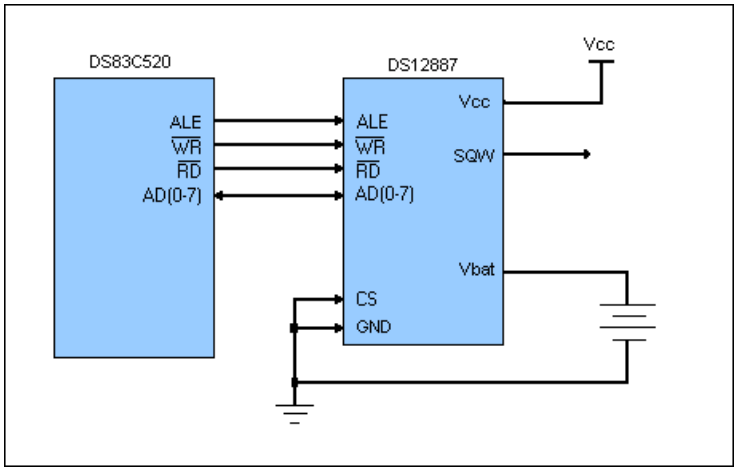
AD0–AD7	– Multiplexed Address/Data Bus
N.C.	– No Connection
MOT	– Bus Type Selection
$\overline{CS}$	– Chip Select
AS	– Address Strobe
R/$\overline{W}$	– Read/Write Input
DS	– Data Strobe
$\overline{RESET}$	– Reset Input
$\overline{IRQ}$	– Interrupt Request Output
SQW	– Square-Wave Output
V_{CC}	– +5V Supply
GND	– Ground

ORDERING INFORMATION

PART	PIN-PACKAGE	TOP MARK	TEMP RANGE
DS12887	24 PDIP Module	DS12887	0°C to +70°C

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.*

TYPICAL OPERATING CIRCUIT



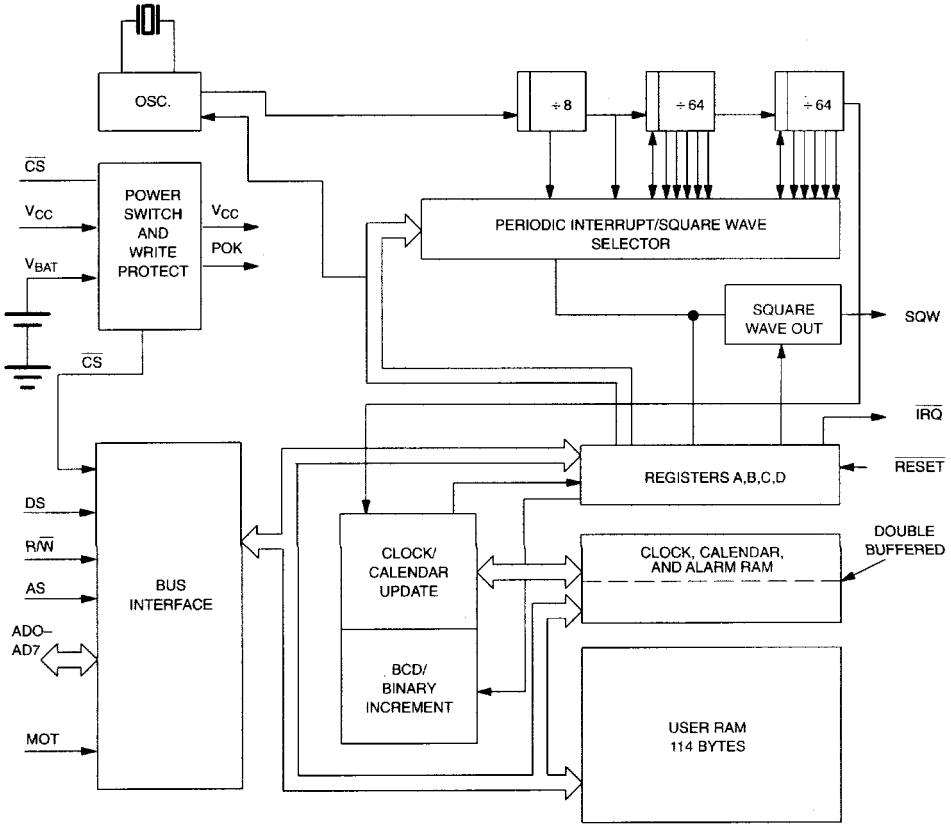
DESCRIPTION

The DS12887 real-time clock (RTC) plus RAM is designed to be a direct replacement for the DS1287. The DS12887 is identical in form, fit, and function to the DS1287, and has an additional 64 bytes of general-purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS12887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a 100-year calendar, programmable interrupt, square-wave generator, and 114 bytes of NV SRAM. The RTC is unique in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS12887. The following paragraphs describe the function of each pin.

Figure 1. BLOCK DIAGRAM



POWER-UP/DOWN CONSIDERATIONS

The RTC function continues to operate, and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS12887 and reaches a level of greater than 4.25V, the device becomes accessible after 200ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25V, the chip-select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS12887 is, therefore, write-protected. When the DS12887 is in a write-protected state, all inputs are ignored and all outputs are in a high-impedance state. When V_{CC} falls below a level of approximately 3V, the external V_{CC} supply is switched off, and an internal lithium energy source supplies power to the RTC and the RAM memory.

SIGNAL DESCRIPTIONS

GND, V_{CC} – DC power is provided to the device on these pins. V_{CC} is the +5V input. When 5V are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25V typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3V typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at +25°C, regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) – The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pulldown resistance of approximately 20kΩ.

SQW (Square-Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25V, typically.

Table 1. PERIODIC INTERRUPT RATE AND SQUARE-WAVE OUTPUT FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070µs	8.192kHz
0	1	0	0	244.141µs	4.096kHz
0	1	0	1	488.281µs	2.048kHz
0	1	1	0	976.5625µs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

AD0–AD7 (Multiplexed Bidirectional Address/Data Bus) – Multiplexed buses save pins because address information and data information time-share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS12887 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ ALE, at which time the DS12887 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS12887 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read

cycle is terminated and the bus returns to a high-impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input) – A positive-going address-strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS12887. The next rising edge that occurs on the AS bus clears the address regardless of whether $\overline{CS}$ is asserted. Access commands should be sent in pairs.

DS (Data Strobe or Read Input) – The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode, DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS12887 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS12887 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read ($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS12887 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the output-enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input) – The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level that indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active-low signal called WR. In this mode, the R/$\overline{W}$ pin has the same meaning as the write-enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip-Select Input) – The chip select signal must be asserted low for a bus cycle in the DS12887 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles that take place without asserting $\overline{CS}$ latch addresses but no access occur. When V_{CC} is below 4.25V, the DS12887 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the RTC data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) – The $\overline{IRQ}$ pin is an active-low output of the DS12887 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pullup resistor.

$\overline{RESET}$ (Reset Input) – The $\overline{RESET}$ pin has no affect on the clock, calendar, or RAM. On power-up, the $\overline{RESET}$ pin can be held low for a time to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time

$\overline{\text{RESET}}$ is low should exceed 200ms to ensure that the internal timer that controls the DS12887 on power-up has timed out. When $\overline{\text{RESET}}$ is low and V_{CC} is above 4.25V, the following occurs:

A) Periodic Interrupt Enable (PEI) bit is cleared to 0.
B) Alarm Interrupt Enable (AIE) bit is cleared to 0.
C) Update Ended Interrupt Flag (UF) bit is cleared to 0.
D) Interrupt Request Status Flag (IRQF) bit is cleared to 0.
E) Periodic Interrupt Flag (PF) bit is cleared to 0.
F) The device is not accessible until $\overline{\text{RESET}}$ is returned high.
G) Alarm Interrupt Flag (AF) bit is cleared to 0.
H) H. $\overline{\text{IRQ}}$ pin is in the high impedance state.
I) Square-Wave Output Enable ($\overline{\text{SQWE}}$) bit is cleared to 0.
J) Update Ended Interrupt Enable (UIE) is cleared to 0.

In a typical application $\overline{\text{RESET}}$ can be connected to V_{CC}. This connection allows the DS12887 to go in and out of power fail without affecting any of the control registers.

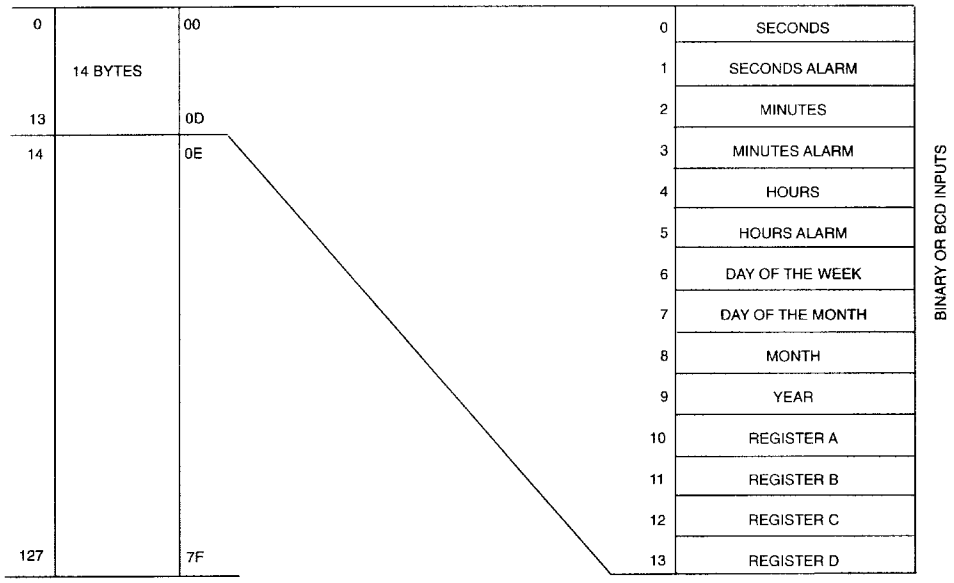
ADDRESS MAP

The address map of the DS12887 is shown in Figure 2. The address map consists of 114 bytes of user RAM; 10 bytes of RAM that contain the RTC time, calendar, and alarm data; and 4 bytes that are used for control and status. All 128 bytes can be directly written or read except for the following:

1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) The high-order bit of the seconds byte is read-only.

The contents of four registers (A, B, C, and D) are described in the *Registers* section.

Figure 2. ADDRESS MAP



TIME, CALENDAR, AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the 10 time, calendar, and alarm bytes can be either binary or binary coded decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 10 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 10 time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the RTC to update the time and calendar bytes. Once initialized, the RTC makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24–12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high-order bit of the hours byte represents PM when it is a logic 1. The time, calendar, and alarm bytes are always accessible because they are double buffered. The 10 bytes are advanced once per second by 1 second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., might not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a “don’t care” state in one or more of the three alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm is generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second.

Table 2. TIME, CALENDAR, AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	DATA MODE RANGE	
			BINARY	BCD
0	Seconds	0–59	00–3B	00–59
1	Seconds Alarm	0–59	00–3B	00–59
2	Minutes	0–59	00–3B	00–59
3	Minutes Alarm	0–59	00–3B	00–59
4	Hours, 12-hour Mode	1–12	01–0C AM, 81–8C PM	01–12AM, 81–92PM
	Hours, 24-hour Mode	0–23	00–17	00–23
5	Hours Alarm, 12-hour	1–12	01–0C AM, 81–8C PM	01–12AM, 81–92PM
	Hours Alarm, 24-hourr	0–23	00–17	00–23
6	Day of the Week Sunday = 1	1–7	01–07	01–07
7	Date of the Month	1–31	01–1F	01–31
8	Month	1–12	01–0C	01–12
9	Year	0–99	00–63	00–99

NV RAM

The 114 general-purpose NV RAM bytes are not dedicated to any special function within the DS12887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500ms to 122µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independently of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit that software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that set bits remain stable throughout the read cycle. All bits that are set (high) are cleared when read and new interrupts that are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each used flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic 1 in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12887. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS12887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A turns the oscillator on and enables the countdown chain. A pattern of 11X turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE-WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square-wave output signal on the SQW pin. The RS0–RS3 bits in Register A establish the square-wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1–of–15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square-wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt causes the $\overline{\text{IRQ}}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits, which select the square-wave frequency (Table 1). Changing the Register A bits affect both the square-wave frequency and the periodic-interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square-wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The DS12887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

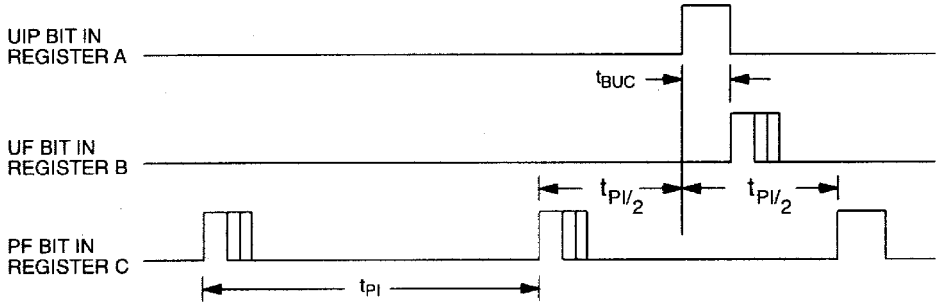
There are three methods that can handle access of the RTC that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is

changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within one ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

Figure 3. UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS12887 has four control registers that are accessible at all times, even during the update cycle.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP – The update-in-progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244□s. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2– These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that turn the oscillator on and allow the RTC to keep time. A pattern of 11X enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0 – These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square-wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1) Enable the interrupt with the PIE bit;
2) Enable the SQW output pin with the SQWE bit;
3) Enable both at the same time and the same rate; or
4) Enable neither.

Table 1 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET – When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS12887.

PIE – The periodic-interrupt enable (PIE) bit is a read/write bit that allows the periodic-interrupt flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12887 functions, but is cleared to 0 on $\overline{\text{RESET}}$.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit that, when set to a 1, permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to 0. The internal functions of the DS12887 do not affect the AIE bit.

UIE – The update-ended interrupt enable (UIE) bit is a read/ write that enables the update-end flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a 1, a square-wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to z0, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data while a 0 in DM specifies BCD data.

24/12 – The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE – The Daylight Savings Enable (DSE) bit is a read/write bit that enables two special updates when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF– The interrupt request flag (IRQF) bit is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF x PIE + AF x AIE + UF x UIE.

Any time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF– The periodic-interrupt flag (PF) is a read-only bit that is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{\text{IRQ}}$ signal is active and sets the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF– A 1 in the alarm-interrupt flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a 1, the $\overline{\text{IRQ}}$ pin goes low and a 1 appears in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C clears AF.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is set to 1, the one in UF causes the IRQF bit to be a 1, which asserts the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0, BIT 1, BIT 2, BIT 3 – These are unused bits of the status Register C. These bits always read 0 and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The valid RAM and time (VRT) bit is set to the 1 state prior to shipment. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6, BIT 5, BIT 4, BIT 3, BIT 2, BIT 1, BIT 0– The remaining bits of Register D are not usable. They cannot be written and, when read, they always read 0.

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C
Soldering Temperature	See IPC/JEDEC J-STD-020A (Note 7)

**This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V, 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output at 2.4V	I_{OH}	-1.0			mA	1, 5
Output at 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip-Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read-Data Hold Time	t_{DHR}	10		80	ns	
Write-Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

NOTES:

1) All voltages are referenced to ground.
2) All outputs are open.
3) The MOT pin has an internal pulldown of 20kΩ.
4) Applies to the AD0–AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in the high-impedance state.
5) The $\overline{IRQ}$ pin is open drain.
6) Measured with a load as shown in Figure 4.
7) RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

Figure 4. OUTPUT LOAD

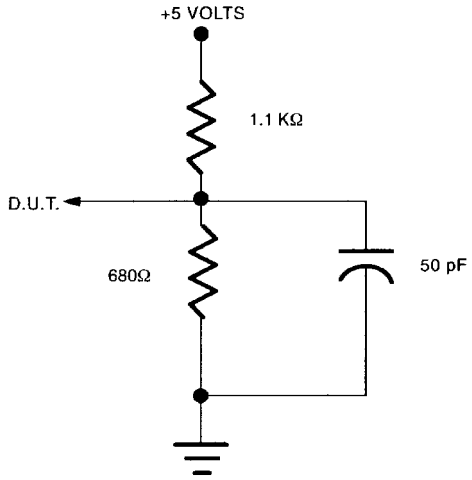


Figure 5. BUS TIMING FOR MOTOROLA INTERFACE

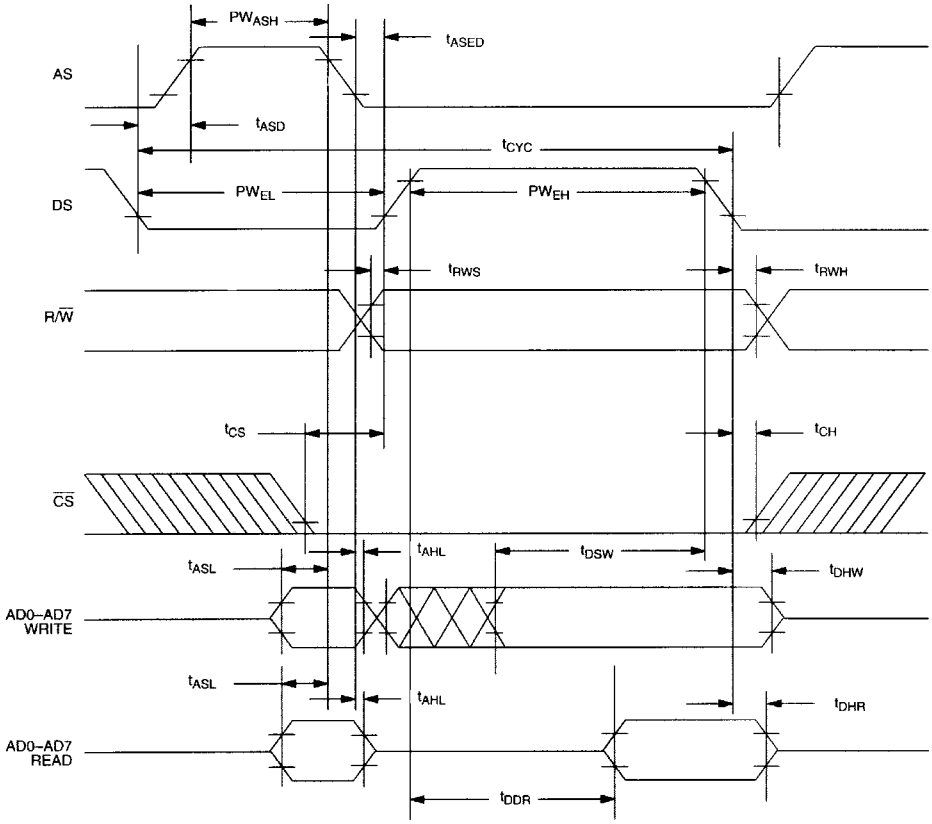


Figure 6. BUS TIMING FOR INTEL INTERFACE WRITE CYCLE

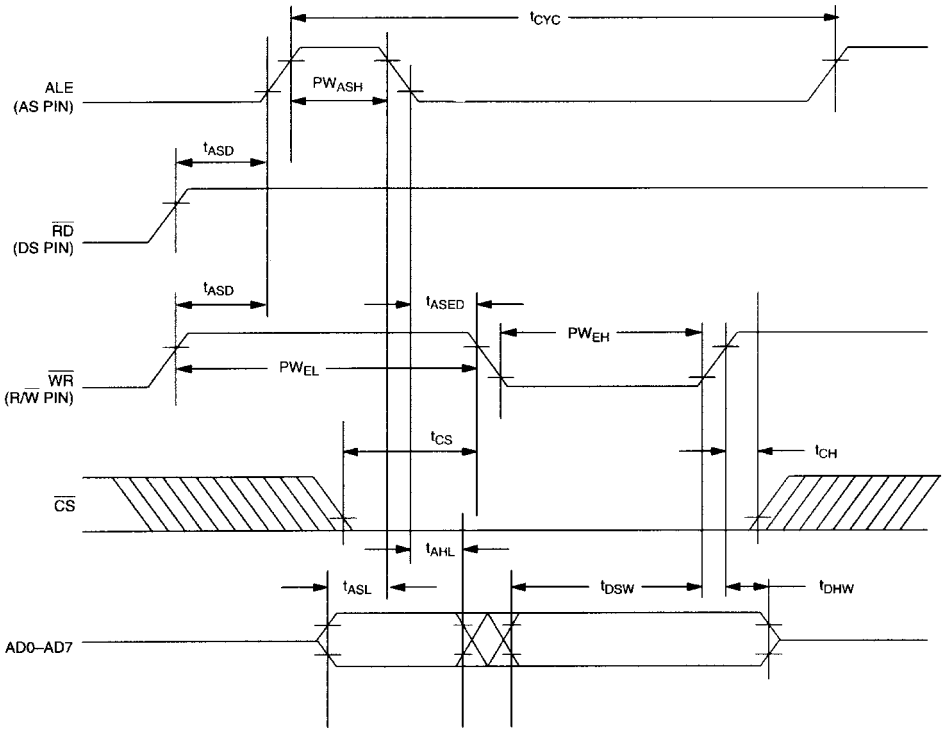


Figure 7. BUS TIMING FOR INTEL INTERFACE READ CYCLE

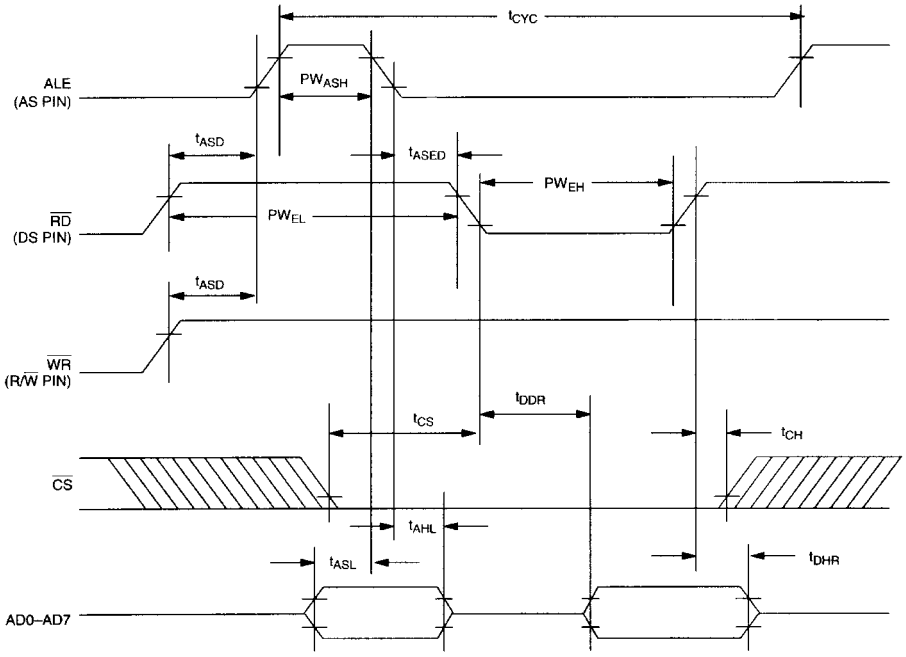


Figure 8. IRQ RELEASE DELAY TIMING

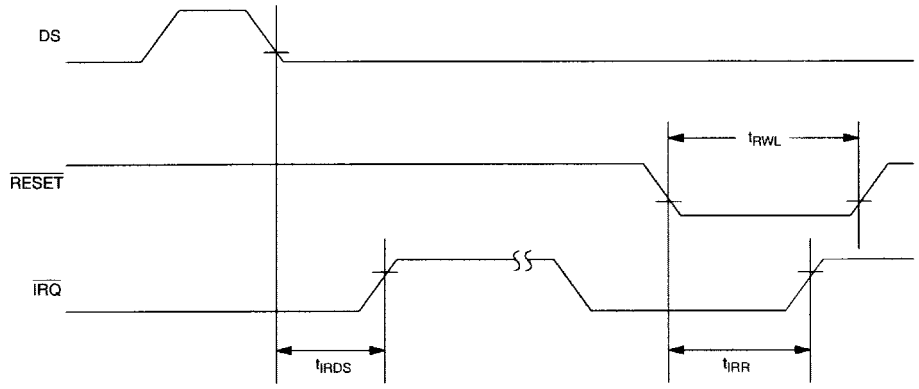
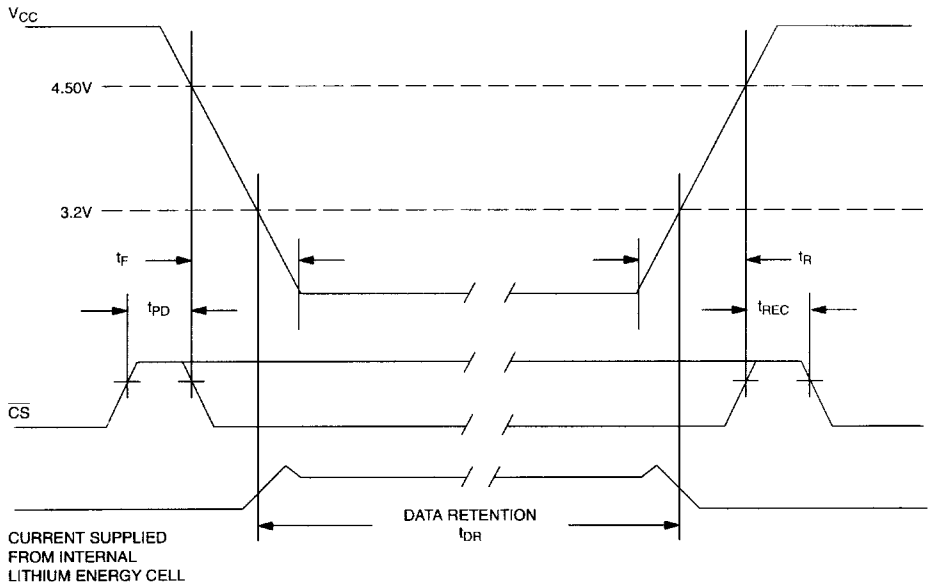


Figure 9. POWER-UP/DOWN TIMING



POWER-UP/DOWN TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

Note: The RTC keeps time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.