

DS10CP152Q Automotive 1.5 Gbps 2X2 LVDS Crosspoint Switch

 Check for Samples: [DS10CP152Q](#)

FEATURES

- AECQ-100 Grade 3
- DC - 1.5 Gbps Low Jitter, Low Skew, Low Power Operation
- Pin Configurable, Fully Differential, Non-Blocking Architecture
- Wide Input Common Mode Voltage Range Allows DC-Coupled Interface to LVDS, CML and LVPECL Drivers
- On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count and Minimizes Board Space
- 8 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small SOIC-16 Space Saving Package

DESCRIPTION

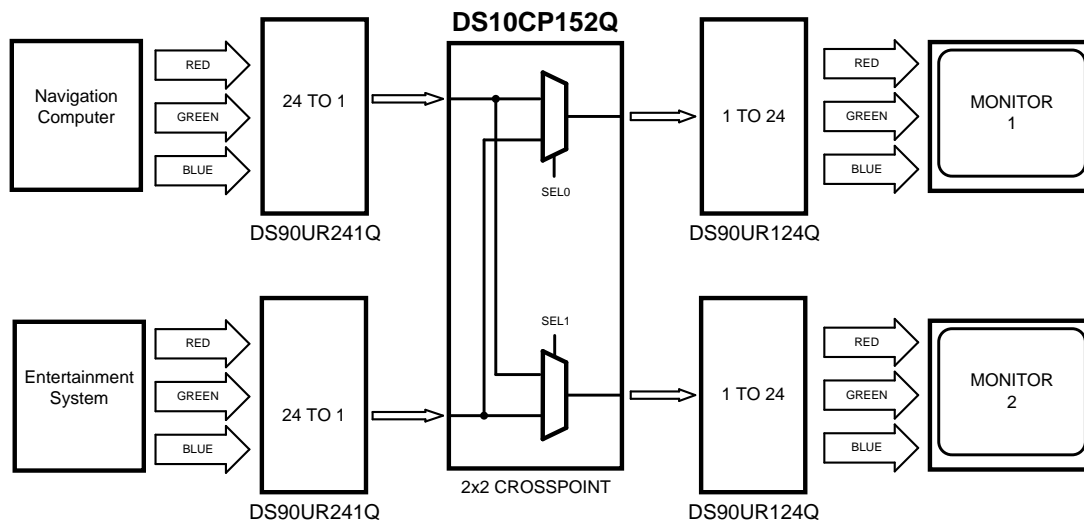
The DS10CP152Q is a 1.5 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

APPLICATIONS

- Automotive Display Applications
- Clock and Data Buffering and Muxing
- SD/HD SDI Routers

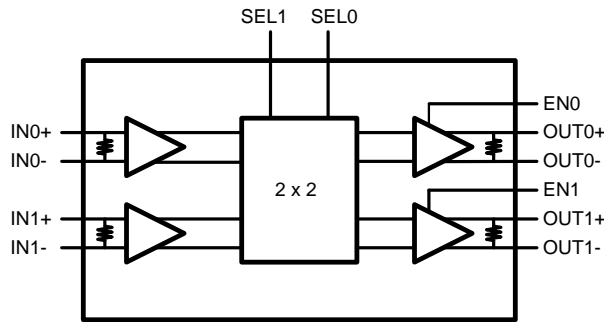
Typical Application



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Block Diagram



Connection Diagram

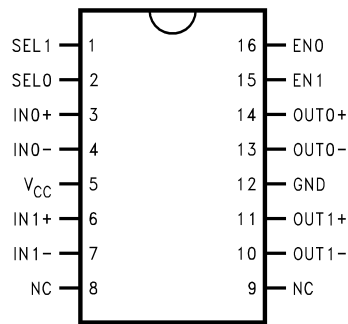


Figure 1. DS10CP152Q Pin Diagram

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0-, IN1+, IN1-	3, 4, 6, 7	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-	14, 13, 11, 10	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
SEL1, SEL0	1, 2	I, LVCMOS	Switch configuration pins.
EN0, EN1	16, 15	I, LVCMOS	Output enable pins.
NC	8, 9	NC	"NO CONNECT" pins.
VDD	5	Power	Power supply pin.
GND	12	Power	Ground pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage	-0.3V to +4V
LVCMOS Input Voltage	-0.3V to ($V_{CC} + 0.3V$)
LVDS Input Voltage	-0.3V to +4V
Differential Input Voltage VID	1V
LVDS Output Voltage	-0.3V to ($V_{CC} + 0.3V$)
LVDS Differential Output Voltage	0V to 1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+105°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
D0016A Package	1.10W
Derate D0016A Package	13.75 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+72.7°C/W
θ_{JC}	+41.2°C/W
ESD Susceptibility	
HBM ⁽³⁾	≥8 kV
MM ⁽⁴⁾	≥250V
CDM ⁽⁵⁾	≥1250V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	-40	+25	+85	°C

DC Electrical Characteristics

 Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 3.6V$ $V_{CC} = 3.6V$	40	175	250	μA

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .
- (3) Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25°C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Low Level Input Current	$V_{IN} = \text{GND}$ $V_{CC} = 3.6\text{V}$		± 1	± 10	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18\text{ mA}$, $V_{CC} = 0\text{V}$		-0.9	-1.5	V
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	$V_{CM} = +0.05\text{V}$ or $V_{CC}-0.05\text{V}$		0	+100	mV
V_{TL}	Differential Input Low Threshold		-100	0		mV
V_{CMR}	Common Mode Voltage Range	$V_{ID} = 100\text{ mV}$	0.05		$V_{CC} - 0.05$	V
I_{IN}	Input Current	$V_{IN} = 3.6\text{V}$ or 0V $V_{CC} = 3.6\text{V}$ or 0V		± 1	± 10	μA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current ⁽⁴⁾	OUT to GND		-23	-55	mA
		OUT to V_{CC}		8	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	EN0 = EN1 = H		58	70	mA
I_{CCZ}	Outputs Powered Down Supply Current	EN0 = EN1 = L		25	30	mA

(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS						
t_{PLHD}	Differential Propagation Delay Low to High	$R_L = 100\Omega$		440	650	ps
t_{PHLD}	Differential Propagation Delay High to Low			400	650	ps
t_{SKD1}	Pulse Skew $ t_{PLHD} - t_{PHLD} $ ⁽⁴⁾			40	120	ps
t_{SKD2}	Channel to Channel Skew ⁽⁵⁾			25	60	ps

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Typical values represent most likely parametric norms for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (3) Specification is guaranteed by characterization and is not tested in production.
- (4) t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (5) t_{SKD2} , Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
t _{SKD3}	Part to Part Skew ⁽⁶⁾			45	190	ps	
t _{LHT}	Rise Time	R _L = 100Ω		170	350	ps	
t _{HLT}	Fall Time			170	350	ps	
t _{ON}	Output Enable Time			5	20	μs	
t _{OFF}	Output Disable Time			3	12	ns	
t _{SEL}	Select Time			3	12	ns	
JITTER PERFORMANCE ⁽³⁾							
t _{RJ1}	Random Jitter (RMS Value)	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ)	135 MHz		0.5	1.2	ps
t _{RJ2}			311 MHz		0.5	1.2	ps
t _{RJ3}			503 MHz		0.5	1.2	ps
t _{RJ4}			750 MHz		0.5	1.2	ps
t _{DJ1}	Deterministic Jitter (Peak-to-Peak Value)	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ)	270 Mbps		9	38	ps
t _{DJ2}			622 Mbps		7	36	ps
t _{DJ3}			1.06 Gbps		7	34	ps
t _{DJ4}			1.5 Gbps		9	35	ps
t _{TJ1}	Total Jitter (Peak to Peak Value)	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ)	270 Mbps		0.01	0.03	UI _{P-P}
t _{TJ2}			622 Mbps		0.01	0.04	UI _{P-P}
t _{TJ3}			1.06 Gbps		0.01	0.05	UI _{P-P}
t _{TJ4}			1.5 Gbps		0.01	0.07	UI _{P-P}

(6) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

DC Test Circuits

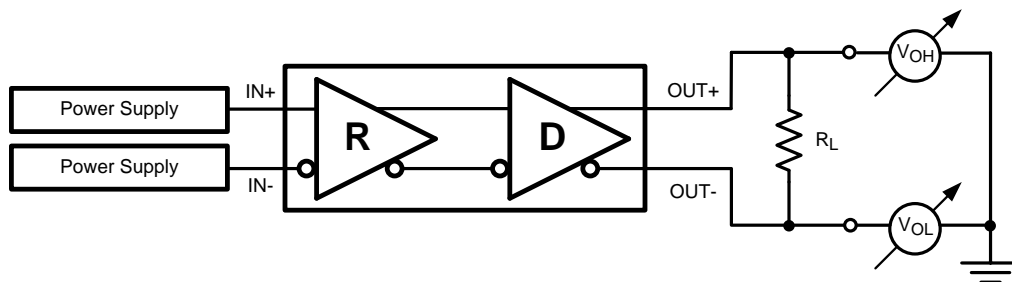


Figure 2.

AC Test Circuits and Timing Diagrams

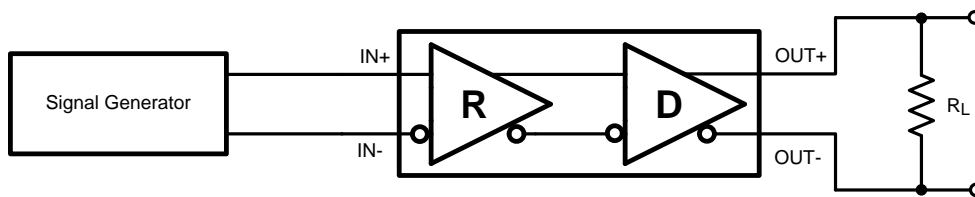


Figure 3.

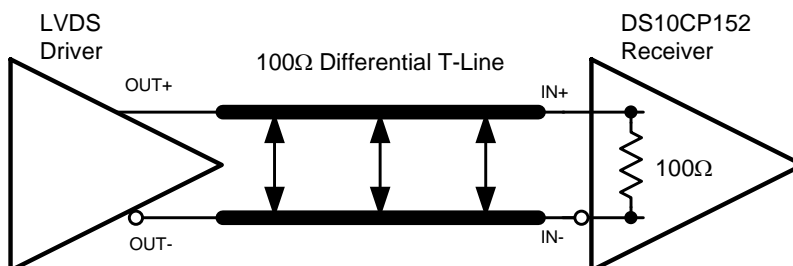


Figure 6. Typical LVDS Driver DC-Coupled Interface to an DS10CP152Q Input

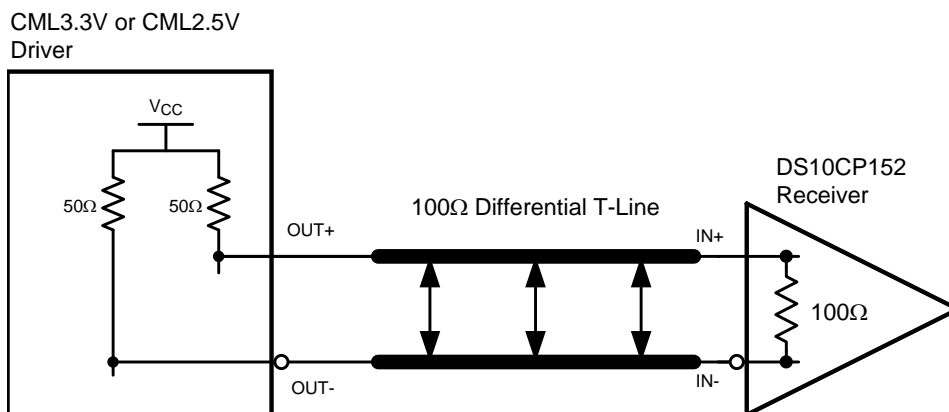


Figure 7. Typical CML Driver DC-Coupled Interface to an DS10CP152Q Input

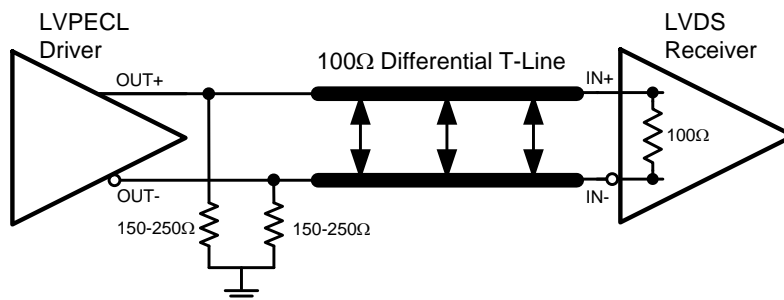


Figure 8. Typical LVPECL Driver DC-Coupled Interface to an DS10CP152Q Input

OUTPUT INTERFACING

The DS10CP152Q outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

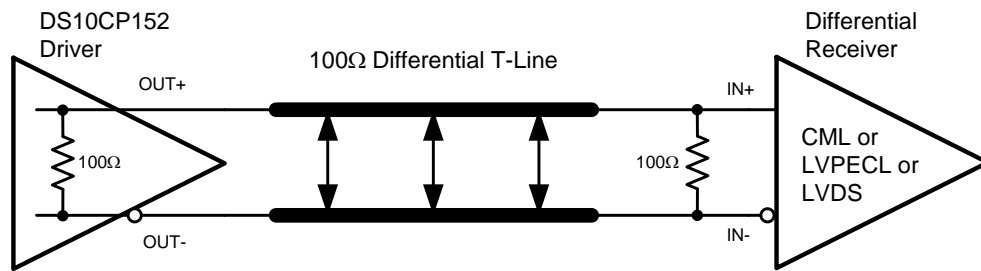
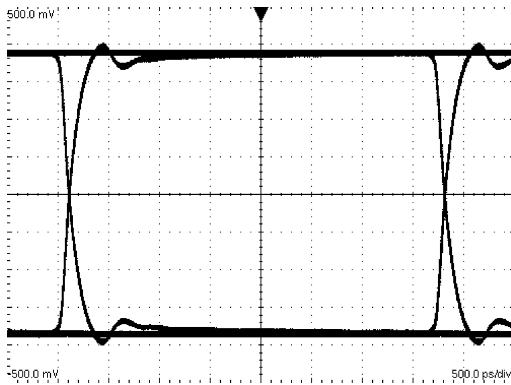
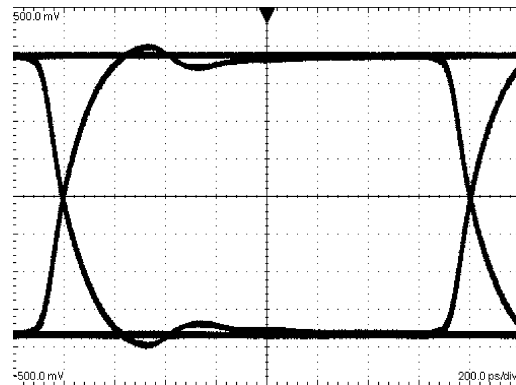


Figure 9. Typical DS10CP152Q Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

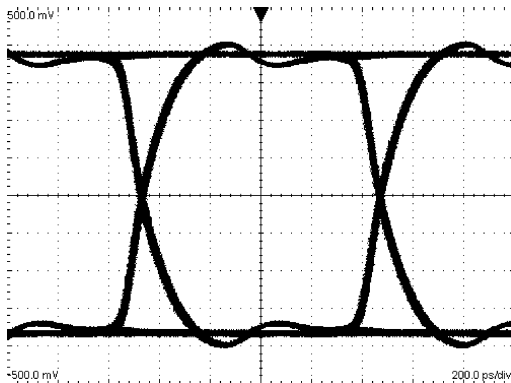
Typical Performance Characteristics



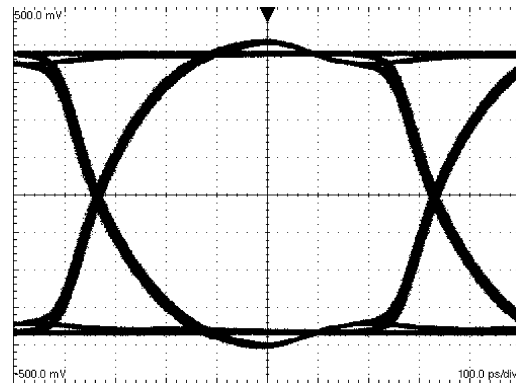
**Figure 10. A 270 Mbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:500 ps / DIV**



**Figure 11. A 622 Mbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:200 ps / DIV**





**Figure 12. A 1.06 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:200 ps / DIV**



**Figure 13. A 1.5 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:100 ps / DIV**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS10CP152QMA/NOPB	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS10CP152 QMA	
DS10CP152QMAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS10CP152 QMA	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS10CP152QMA/NOPB	SOIC	D	16	250	178.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS10CP152QMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS10CP152QMA/NOPB	SOIC	D	16	250	203.0	190.0	41.0
DS10CP152QMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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