Piezo Haptic Driver with Integrated Boost Converter and Digital Front End

Check for Samples: DRV2665

FEATURES

- **Integrated Digital Front End**
  - **I^2C Bus Control up to 400 kHz**
  - **Internal 100 Byte FIFO Interface**
  - **Immersion TS5000 Compliant**
  - **Optional Analog Inputs**
- **High Voltage Piezo-Haptic Driver**
  - **Drives up to 100 nF at 200 V_{PP} and 300 Hz**
  - **Drives up to 150 nF at 150 V_{PP} and 300 Hz**
  - **Drives up to 330 nF at 100 V_{PP} and 300 Hz**
  - **Drives up to 680 nF at 50 V_{PP} and 300 Hz**
  - **Differential Output**
- **Integrated 105 V Boost Converter**
  - **Adjustable Boost Voltage**
  - **Adjustable Boost Current Limit**
  - **Integrated Power FET and Diode**
  - **No Transformer Required**
- **Fast Start Up Time of 2 ms (typical)**
- **Wide Supply Voltage Range of 3 V to 5.5 V**
- **1.8 V Compatible, 5 V Tolerant Digital Pins**
- **Available in a 4 mm × 4 mm × 0.9 mm QFN package (RGP)**
- **Pin-Similar with DRV8662**

APPLICATIONS

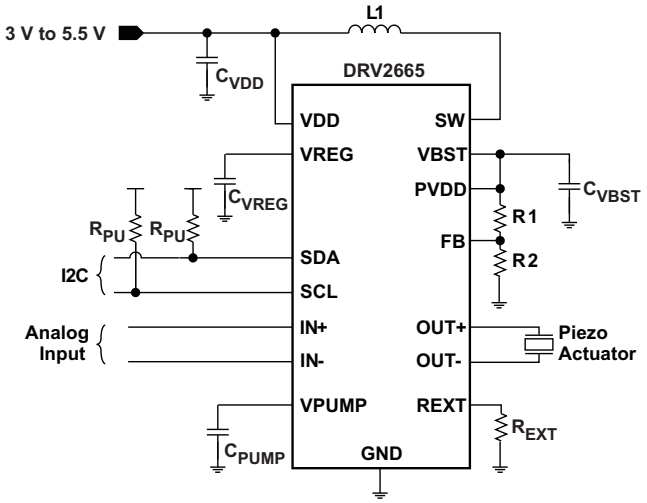
- **Mobile Phones**
- **Tablets**
- **Portable Computers**
- **Keyboards and Mice**
- **Electronic Gaming**
- **Touch Enabled Devices**

DESCRIPTION

The DRV2665 is a piezo haptic driver with integrated 105 V boost switch, integrated power diode, integrated fully-differential amplifier, and integrated digital front end. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be driven as haptic packets over the I^2C port or via the analog inputs.

The DRV2665 digital interface is available via an I^2C compatible bus. A digital interface relieves the costly processor burden of PWM generation or additional analog channel requirements in the host system. Any writes to the internal first-in, first-out buffer (FIFO) will automatically wake up the device and begin playing the waveform after the 2 ms internal startup procedure. When the data flow stops or the FIFO under-runs, the DRV2665 will automatically enter a pop-less shutdown procedure.

The boost voltage is set using two external resistors, and the boost current limit is programmable via the R_{EXT} resistor. A typical start-up time of 2 ms makes the DRV2665 an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when overdriven.



For more information, please contact your local TI sales representative.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV2665RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
DRV2665RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

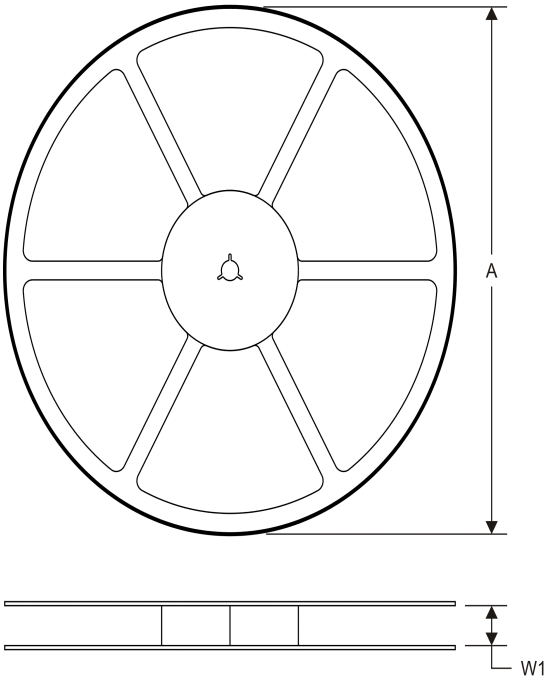
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

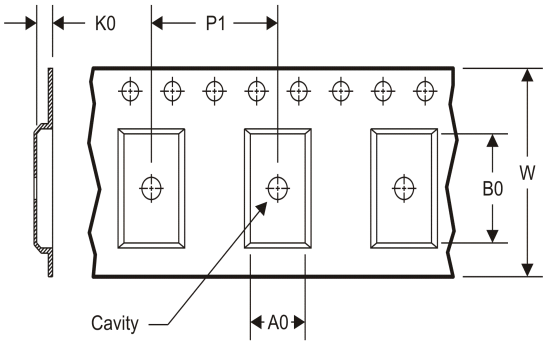
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



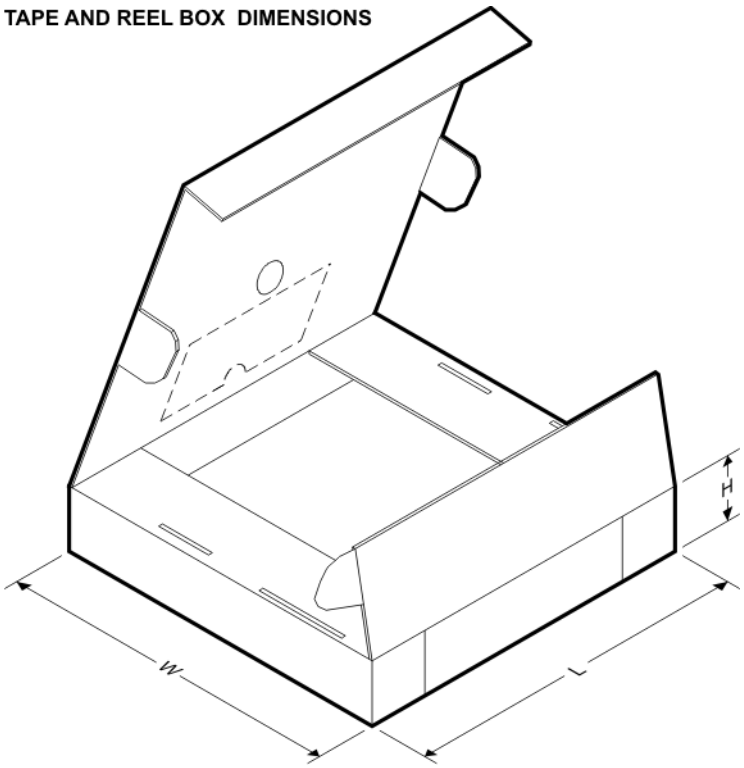
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2665RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV2665RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

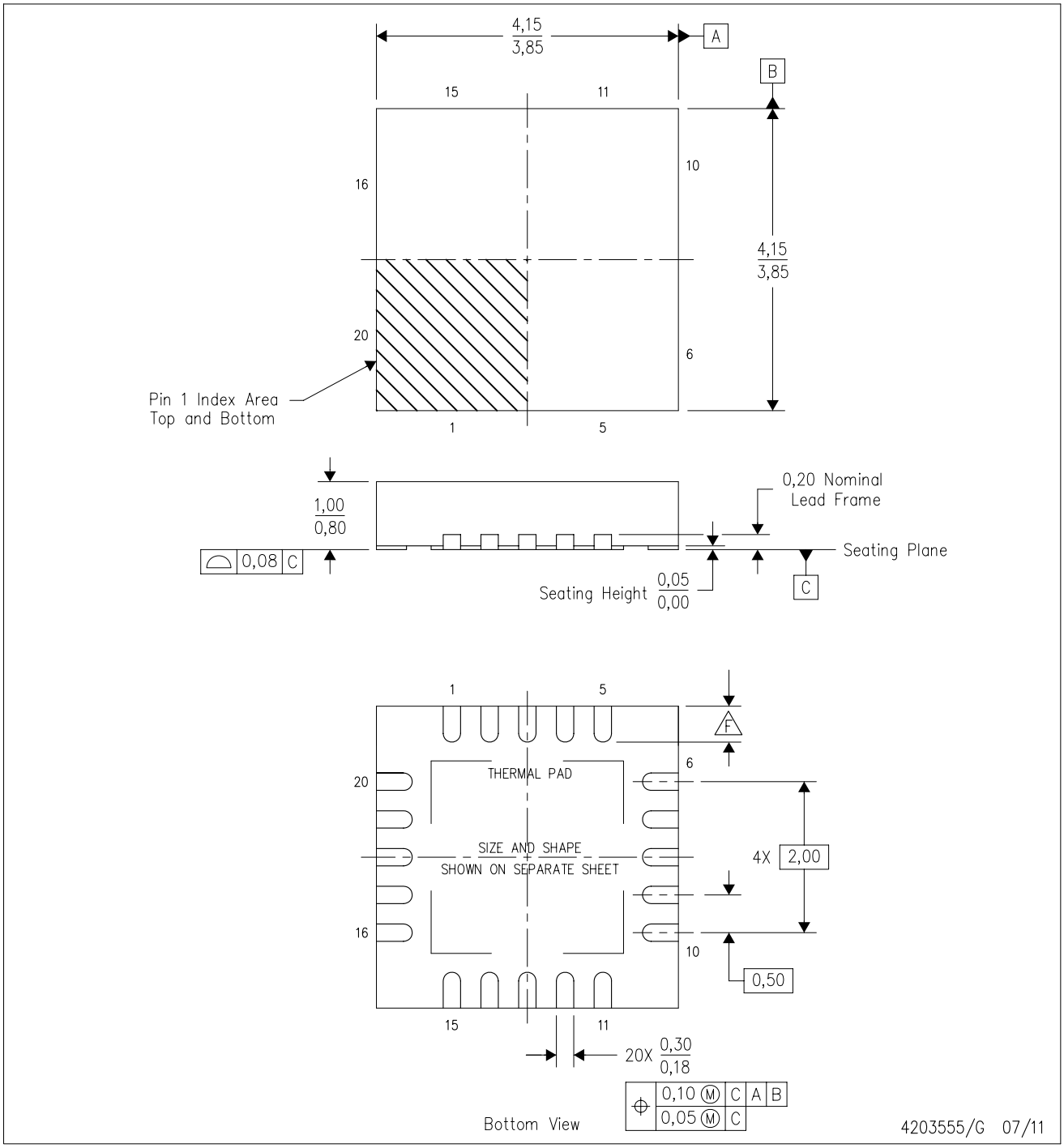
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2665RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
DRV2665RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

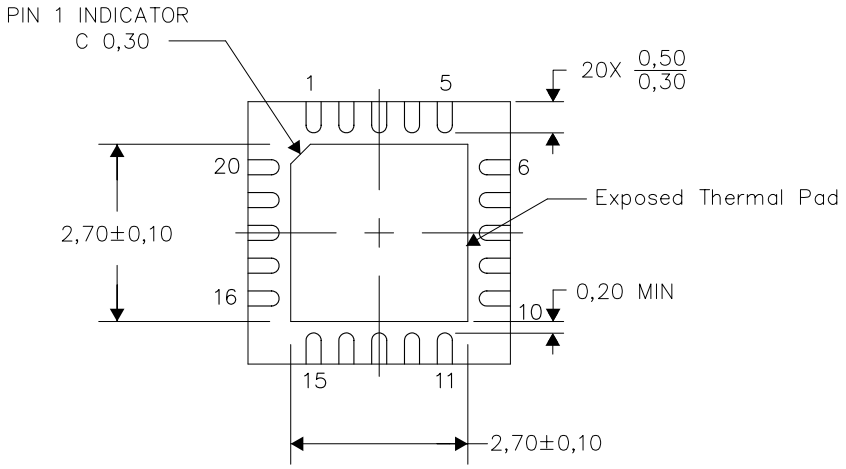
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



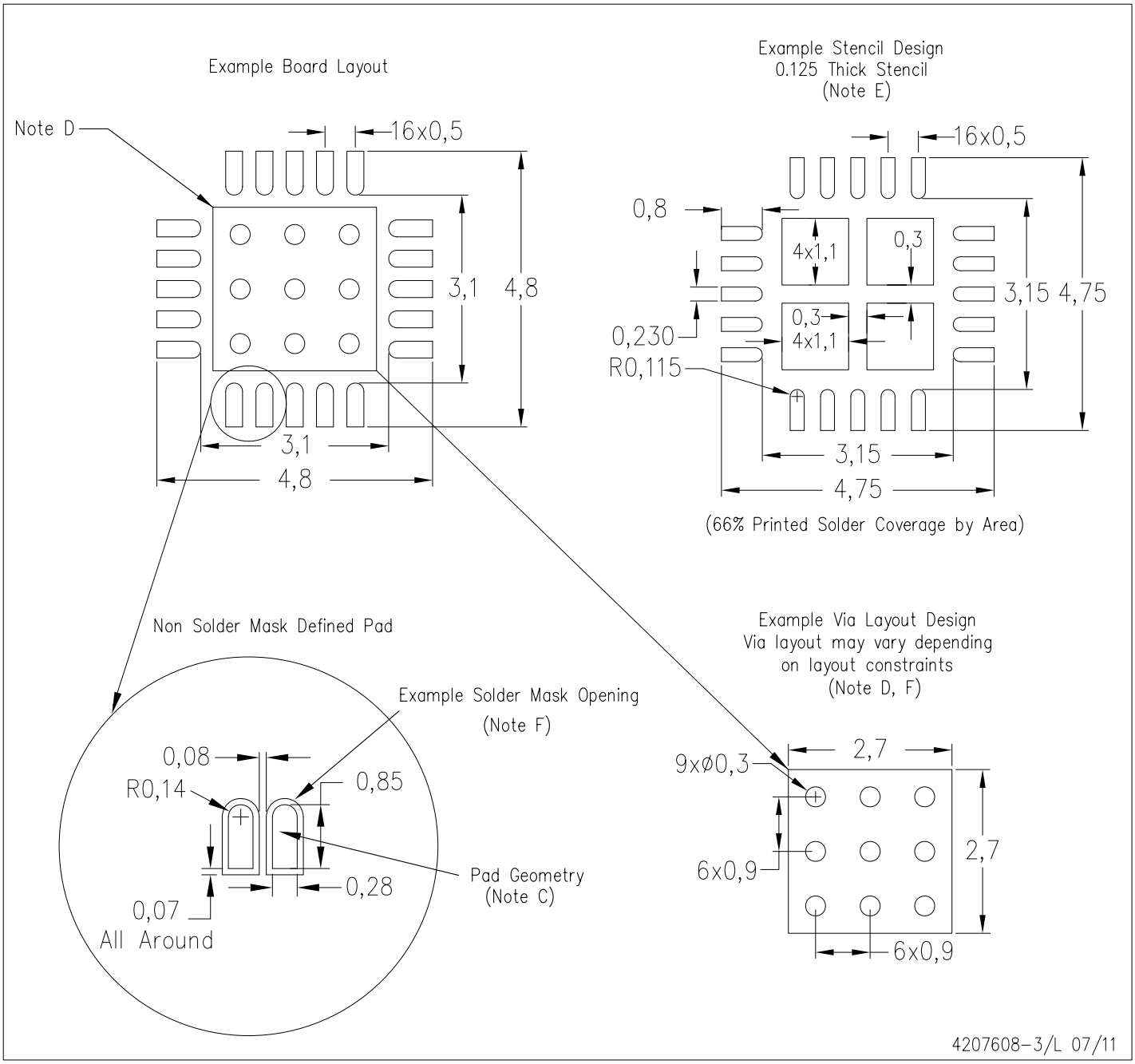
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/X 02/12

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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