POWER SAVING CURRENT CONTROLLED SOLENOID DRIVER

Check for Samples: DRV120

FEATURES

- **Integrated MOSFET With PWM to Control Solenoid Current**
  - **Integrated Sense Resistor for Regulating Solenoid Current**
- **Fast Ramp-Up of Solenoid Current to Guarantee Activation**
- **Solenoid Current is Reduced in Hold Mode for Lower Power and Thermal Dissipation**
- **Peak Current, Keep Time at Peak Current, Hold Current and PWM Clock Frequency Can Be Set Externally. They Can Also Be Operated at Nominal Values Without External Components.**
- **Internal Supply Voltage Regulation**
  - **Up to 28-V External Supply**
- **Protection**
  - **Thermal Shutdown**
  - **Under Voltage Lockout (UVLO)**
  - **Maximum Ramp Time**
  - **Optional STATUS Output**
- **Operating Temperature Range: -40ºC to 105ºC**
- **8-Pin and 14-Pin TSSOP Package Options**

APPLICATIONS

- **Electromechanical Driver: Solenoids, Valves, Relays**
- **White Goods, Solar, Transportation**

DESCRIPTION

The DRV120 is a PWM current driver for solenoids. It is designed to regulate the current with a well controlled waveform to guarantee activation and to reduce power dissipation at the same time. The solenoid current is ramped up fast to ensure opening of the valve or relay. After the initial ramping, solenoid current is kept at peak value to ensure the correct operation, after which it is reduced to a lower hold level in order to avoid thermal problems and reduce power dissipation.

The peak current duration is set with an external capacitor. The current ramp peak and hold levels, as well as PWM frequency can independently be set with external resistors. External setting resistors can also be omitted, if the default values for the corresponding parameters are suitable for the application.

DRV120 can operate from external 6-V to 28-V supply.

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
(TSSOP-8) - PW	Reel of 2000	DRV120PWR	120
(TSSOP-14) - PW	Reel of 2000	DRV120APWR	120A

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TYPICAL APPLICATION

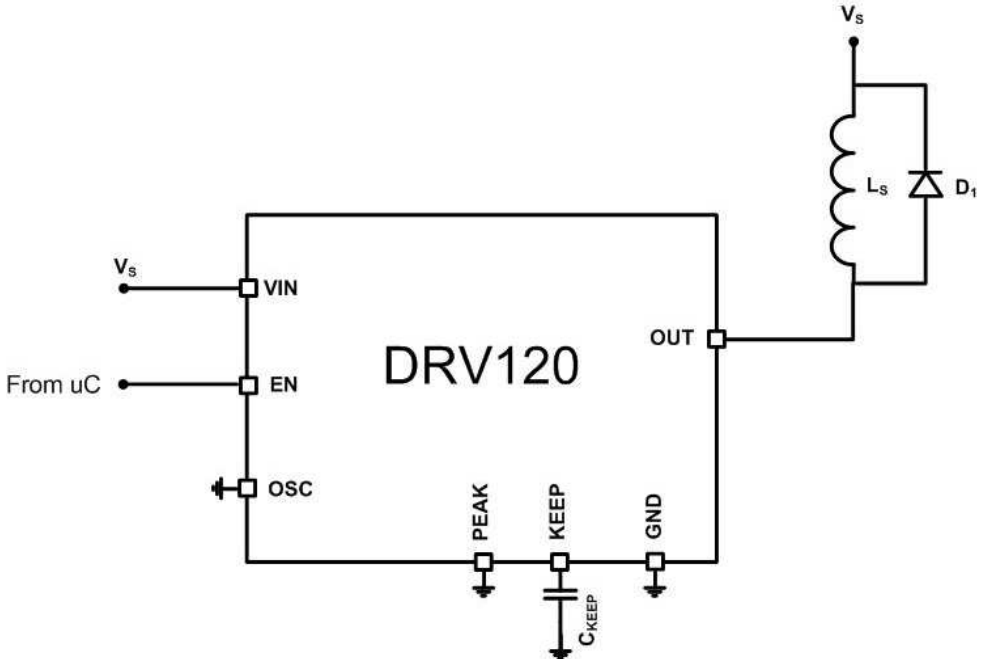


Figure 1. Default Configuration With 8-Pin TSSOP Option

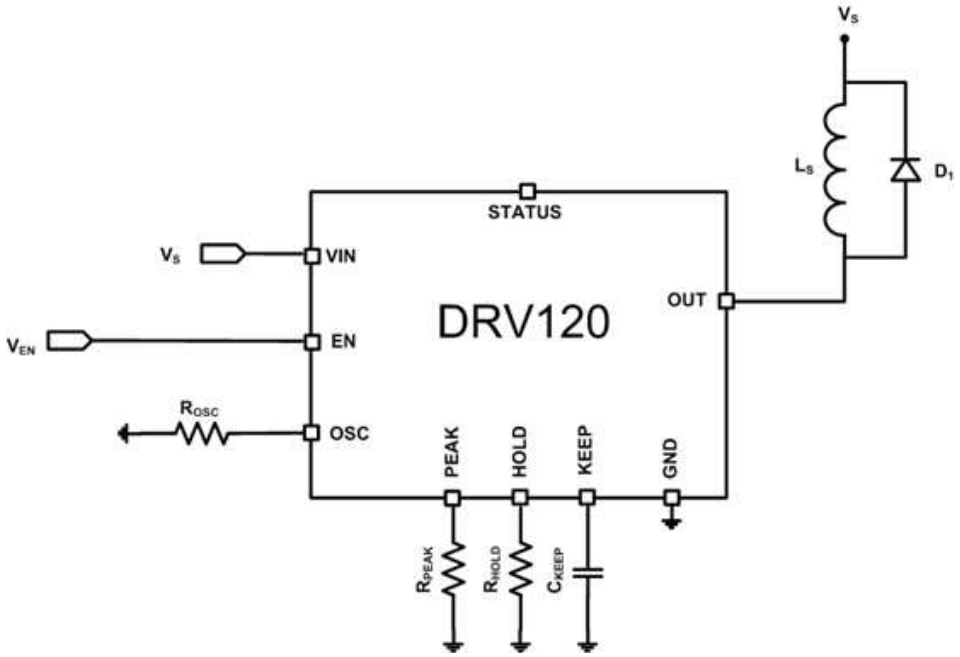


Figure 2. External Parameter Setting for 14-Pin TSSOP Option

DEVICE INFORMATION

Functional Block Diagram

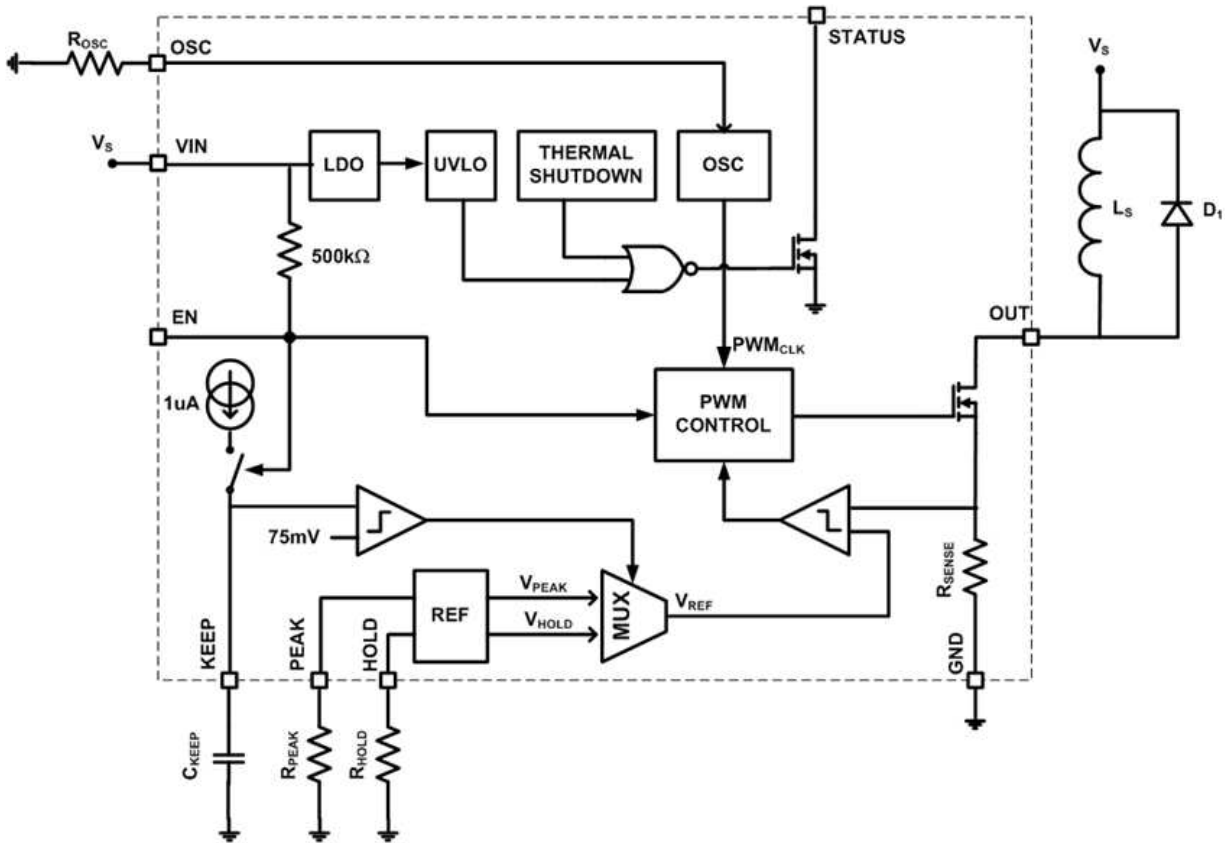
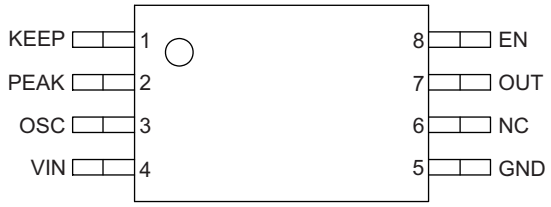


Table 1. TERMINAL FUNCTIONS

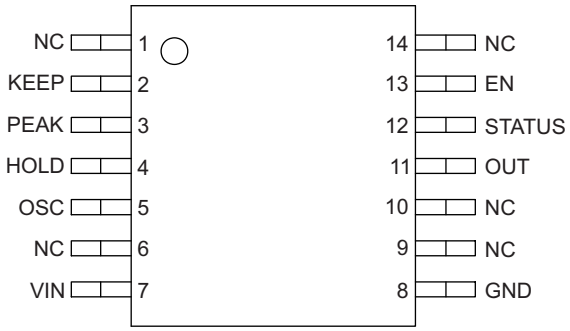
NAME	PIN (8-PIN PW)(1)	PIN (14-PIN PW)	DESCRIPTION
NC	6	1, 6, 9, 10, 14	No connect
KEEP	1	2	Keep time set
PEAK	2	3	Peak current set
HOLD	-	4	Hold current set
OSC	3	5	PWM frequency set
VIN	4	7	6-V to 28-V supply
GND	5	8	Ground
OUT	7	11	Controlled current sink
STATUS	-	12	Open drain fault indicator
EN	8	13	Enable

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.

PW PACKAGE
8-PIN
(TOP VIEW)



PW PACKAGE
14-PIN
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

			VALUE	UNIT
VIN	Input voltage range		–0.3 to 28	V
	Voltage range on EN, STATUS, PEAK, HOLD, OSC, SENSE, RAMP		–0.3 to 7	V
	Voltage range on OUT		–0.3 to 28	V
	ESD rating	HBM (human body model)	2000	V
		CDM (charged device model)	500	
T_J	Operating virtual junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{OUT}	Average solenoid DC current			125	mA
V_{IN}	Supply voltage	6	12	26	V
C_{IN}	Input capacitor	1	4.7		µF
L	Solenoid inductance		1		H
T_A	Operating ambient temperature	-40		105	°C

THERMAL INFORMATION

THERMAL METRIC		DRV120 PW 8 PINS	DRV120 PW 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	183.8	122.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	69.2	51.2	
θ_{JB}	Junction-to-board thermal resistance(3)	112.6	64.3	
ψ_{JT}	Junction-to-top characterization parameter(4)	10.4	6.5	
ψ_{JB}	Junction-to-board characterization parameter(5)	110.9	63.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	N/A	N/A	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

V_{IN} = 14 V, T_A = -40°C to 105°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Standby current	EN = 0, V_{IN} = 14 V		100	150	µA
	Quiescent current	EN = 1, V_{IN} = 14 V		300	400	
CURRENT DRIVER						
R_{OUT}	OUT to GND resistance	I_{OUT} = 200 mA		1.7	2.5	Ω
f_{PWM}	PWM frequency	OSC = GND	15	20	25	kHz
D_{MAX}	Maximum PWM duty cycle			100		%
D_{MIN}	Minimum PWM duty cycle			9		%
t_D	Start-up delay	Delay between EN going high until driver enabled(1), f_{PWM} = 20 kHz		25	50	µs
CURRENT CONTROLLER, INTERNAL SETTINGS						
I_{PEAK}	Peak current	PEAK = GND	160	200	240	mA
I_{HOLD}	Hold current	HOLD = GND	40	50	60	mA
CURRENT CONTROLLER, EXTERNAL SETTINGS						
t_{KEEP}(2)	Externally set keep time at peak current	C_{KEEP} = 1 µF		75		ms
I_{PEAK}	Externally set peak current	R_{PEAK} = 50 kΩ		250		mA
		R_{PEAK} = 200 kΩ		83		
I_{HOLD}	Externally set hold current	R_{HOLD} = 50 kΩ		100		mA
		R_{HOLD} = 200 kΩ		33		
f_{PWM}	Externally set PWM frequency	R_{OSC} = 50 kΩ		60		kHz
		R_{OSC} = 200 kΩ		20		
LOGIC INPUT LEVELS (EN)						
V_{IL}	Input low level				1.3	V
V_{IH}	Input high level		1.65			V
R_{EN}	Input pull-up resistance		350	500		kΩ
LOGIC OUTPUT LEVELS (STATUS)						
V_{OL}	Output low level	Pull-down activated, I_{STATUS} = 2 mA			0.3	V
I_{IL}	Output leakage current	Pull-down deactivated, V(STATUS) = 5 V			1	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold			4.6		V
THERMAL SHUTDOWN						
T_{TSD}	Junction temperature shutdown threshold			160		°C
T_{TSU}	Junction temperature startup threshold			140		°C

(1) Logic HIGH between 4 V and 7 V. Note: absolute max voltage rating is 7 V.
(2) Either internal or external t_{KEEP} time setting is selected to be activated during manufacturing of production version of DRV120.

FUNCTIONAL DESCRIPTION

DRV120 controls the current through the solenoid as shown in Figure 3. Activation starts when EN pin voltage is pulled high either by an external driver or internal pull-up. In the beginning of activation, DRV120 allows the load current to ramp up to the peak value I_{PEAK} and it regulates it at the peak value for the time, t_{KEEP}, before reducing it to I_{HOLD}. The load current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV120 allows the solenoid current to decay to zero.

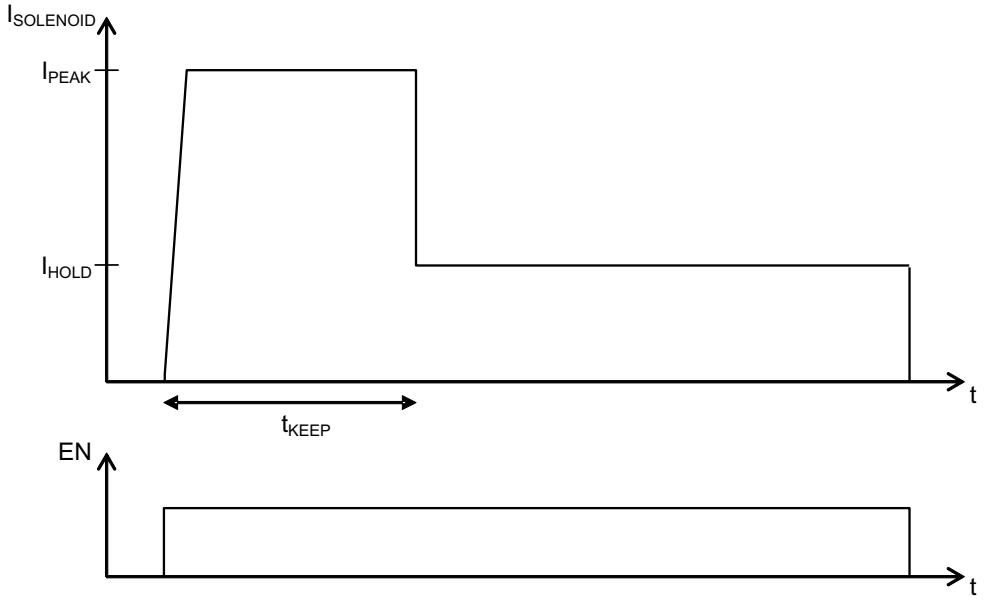


Figure 3. Typical Current Waveform Through the Solenoid

t_{KEEP} is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 75 mV, the current regulation reference voltage, V_{REF}, is switched from V_{PEAK} to V_{HOLD}. Dependency of t_{KEEP} from the external capacitor size can be calculated by:

$$t_{KEEP}\left[s\right] = C_{KEEP}\left[F\right] \cdot 75 \cdot 10^{3}\left[\frac{s}{F}\right] \quad (1)$$

The current control loop regulates, cycle-by-cycle, the solenoid current by using an internal current sensing resistor and MOSFET switch. During the ON-cycle, current flows from OUT pin to GND pin through the internal switch as long as voltage over current sensing resistor is less than V_{REF}. As soon as the current sensing voltage is above V_{REF}, the internal switch is immediately turned off until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the internal switch is turned on and stays on for at least the time determined by the minimum PWM signal duty cycle, D_{MIN}.

I_{PEAK} and I_{HOLD} depend on fixed resistance values R_{PEAK} and R_{HOLD} as shown in Figure 4. If the PEAK pin is connected to ground or if R_{PEAK} is below 33.33 kΩ (typ value), then I_{PEAK} is at its default value (internal setting). The I_{PEAK} value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 50-kΩ (= R_{PEAK}) resistor is connected between PEAK and GND, then the externally set I_{PEAK} level will be 250 mA. If R_{PEAK} = 200 kΩ is, then the externally set I_{PEAK} level will be 83 mA. HOLD current external setting, I_{HOLD}, works in the same way, but current levels are 40% of the I_{PEAK}. External settings for I_{PEAK} and I_{HOLD} are independent of each other. I_{PEAK} and I_{HOLD} values can be calculated by using the formula below.

$$I_{PEAK} = \frac{250mA}{R_{PEAK}} \cdot 66.67k\Omega; 66.67k\Omega < R_{PEAK} < 550k\Omega \quad (2)$$

$$I_{HOLD} = \frac{100mA}{R_{HOLD}} \cdot 66.67k\Omega; 66.67k\Omega < R_{HOLD} < 250k\Omega \quad (3)$$

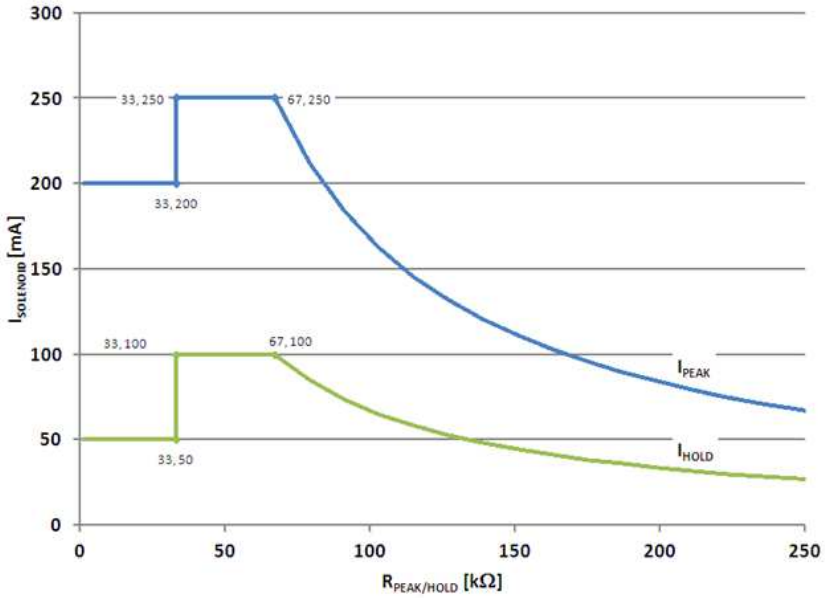


Figure 4. PEAK and HOLD Mode Current Settings

Frequency of the internal PWM clock signal, PWM_{CLK}, that triggers each ON-cycle can be adjusted by external resistor, R_{OSC}, connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 5. Default frequency is used when OSC is connected to GND directly. PWM frequency as a function of external fixed adjustment resistor value (greater than 66.67 kΩ) is given below.

$$f_{PWM} = \frac{60kHz}{R_{OSC}} \cdot 66.67k\Omega; 66.67k\Omega < R_{OSC} < 2M\Omega \quad (4)$$

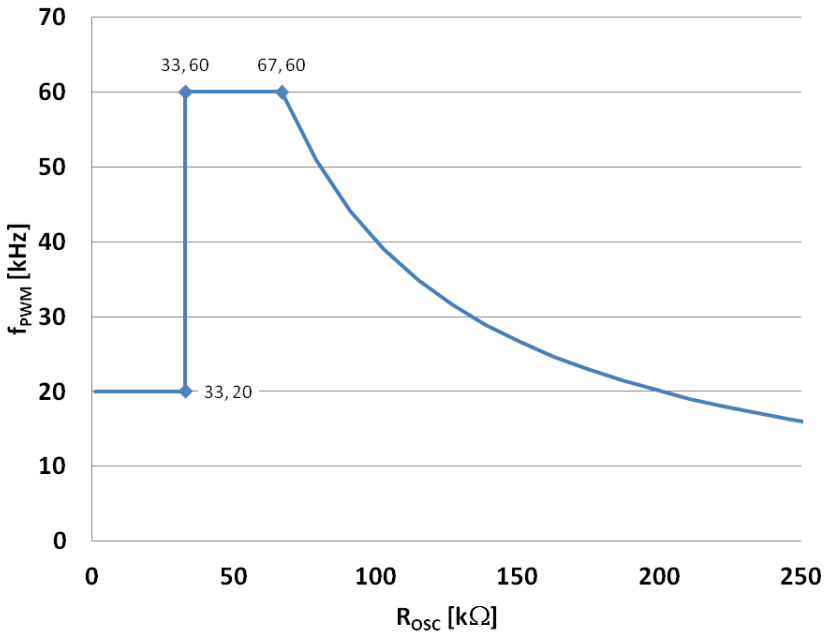


Figure 5. PWM Clock Frequency Setting

Open-drain STATUS output is deactivated if either under voltage lockout or thermal shutdown blocks have triggered.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV120APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV120PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

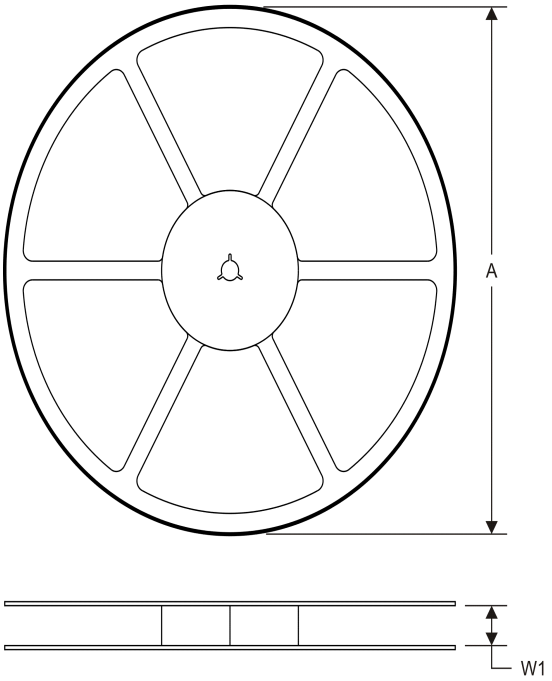
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

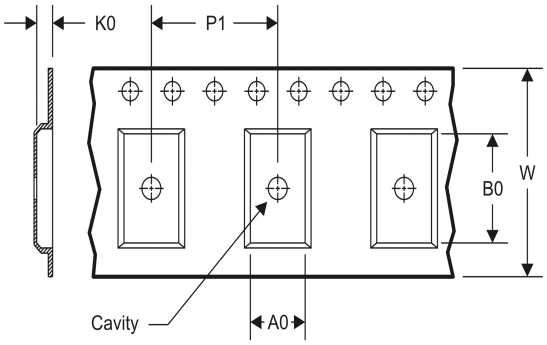
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



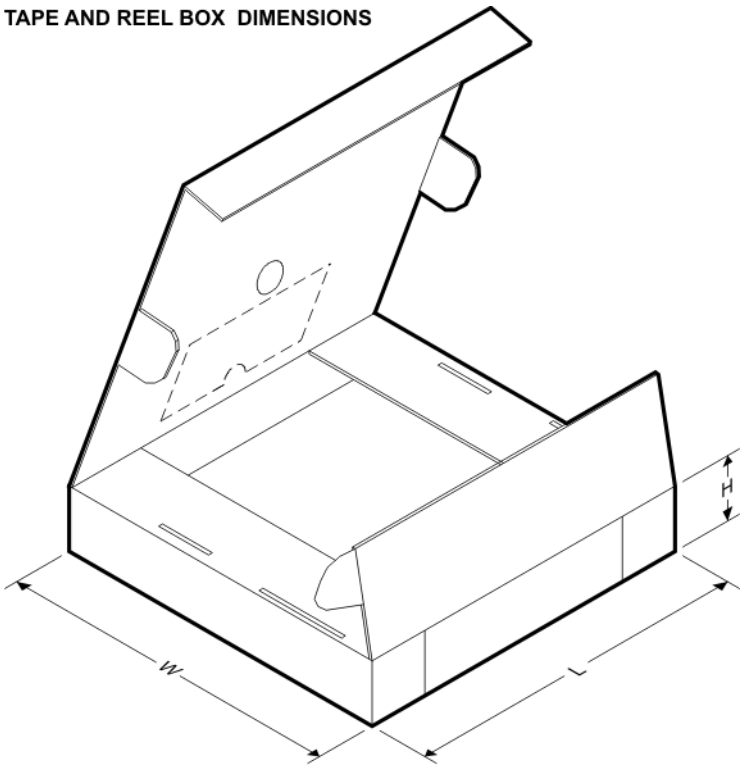
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV120APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV120PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

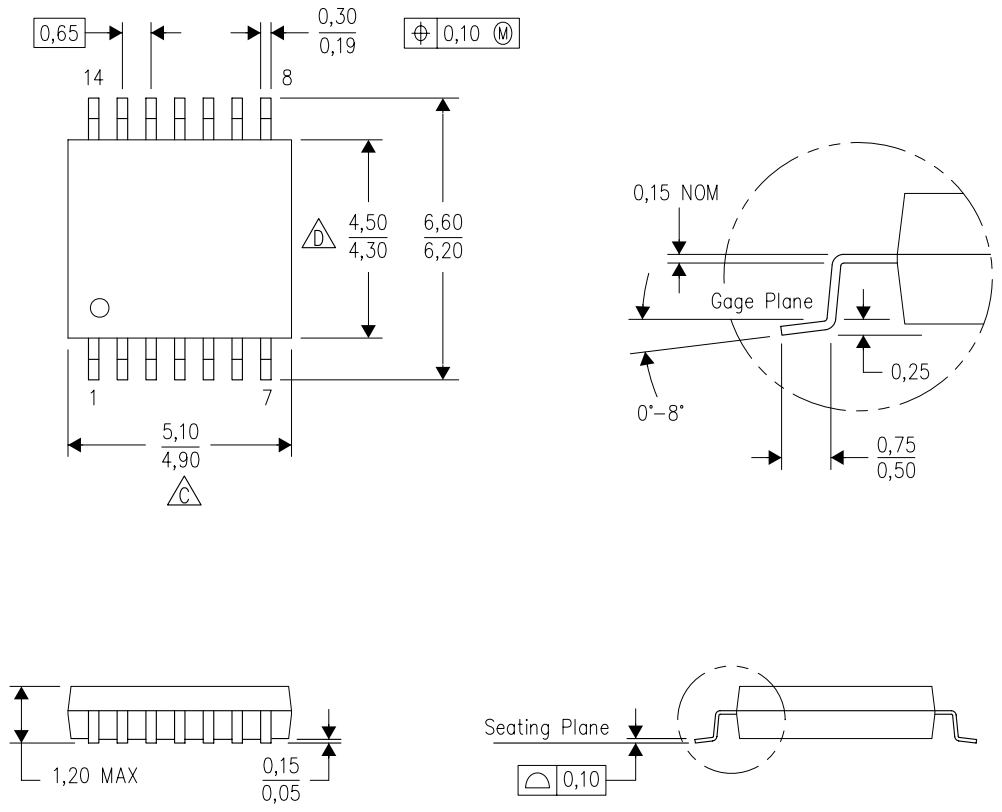
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV120APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
DRV120PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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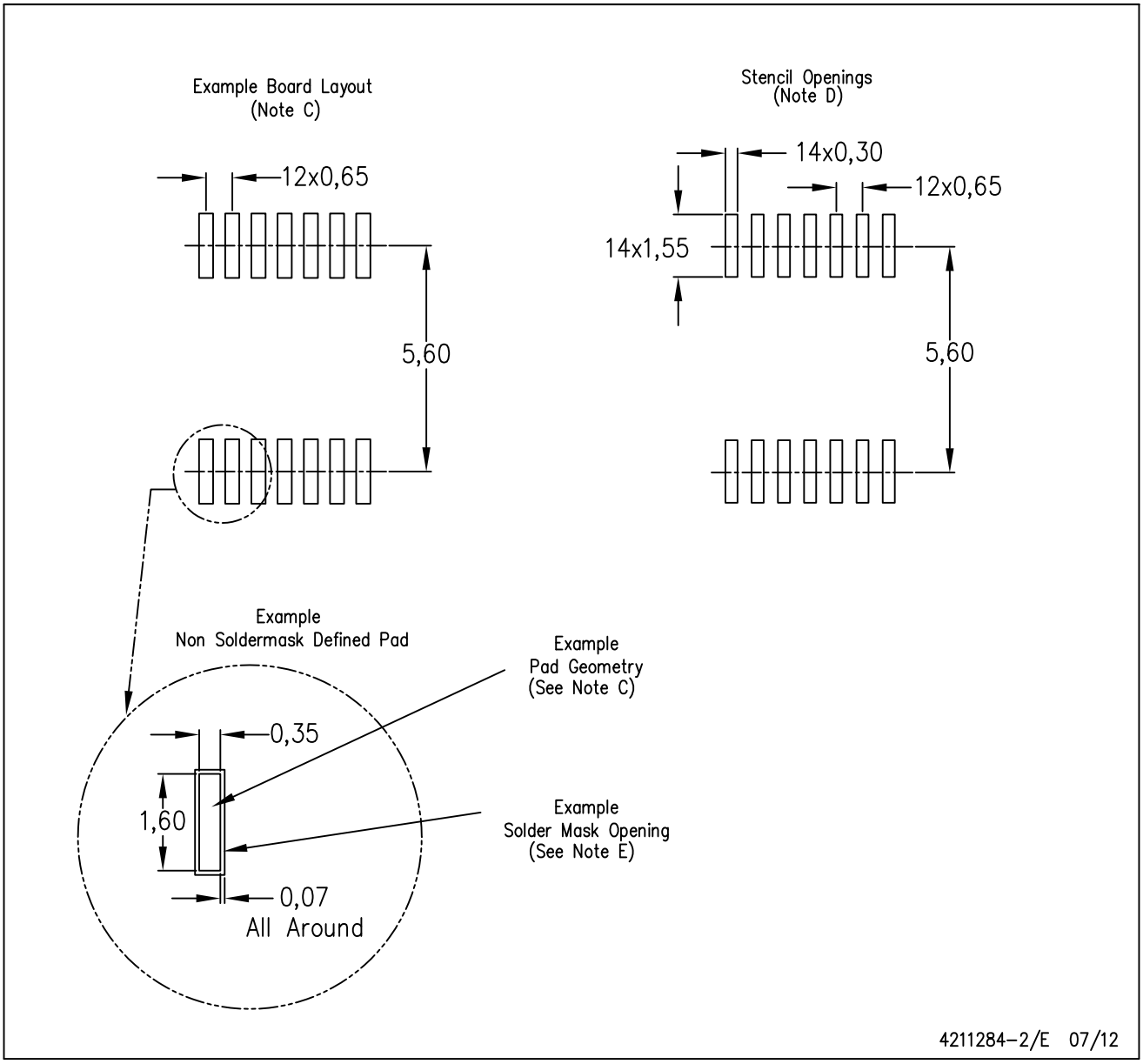
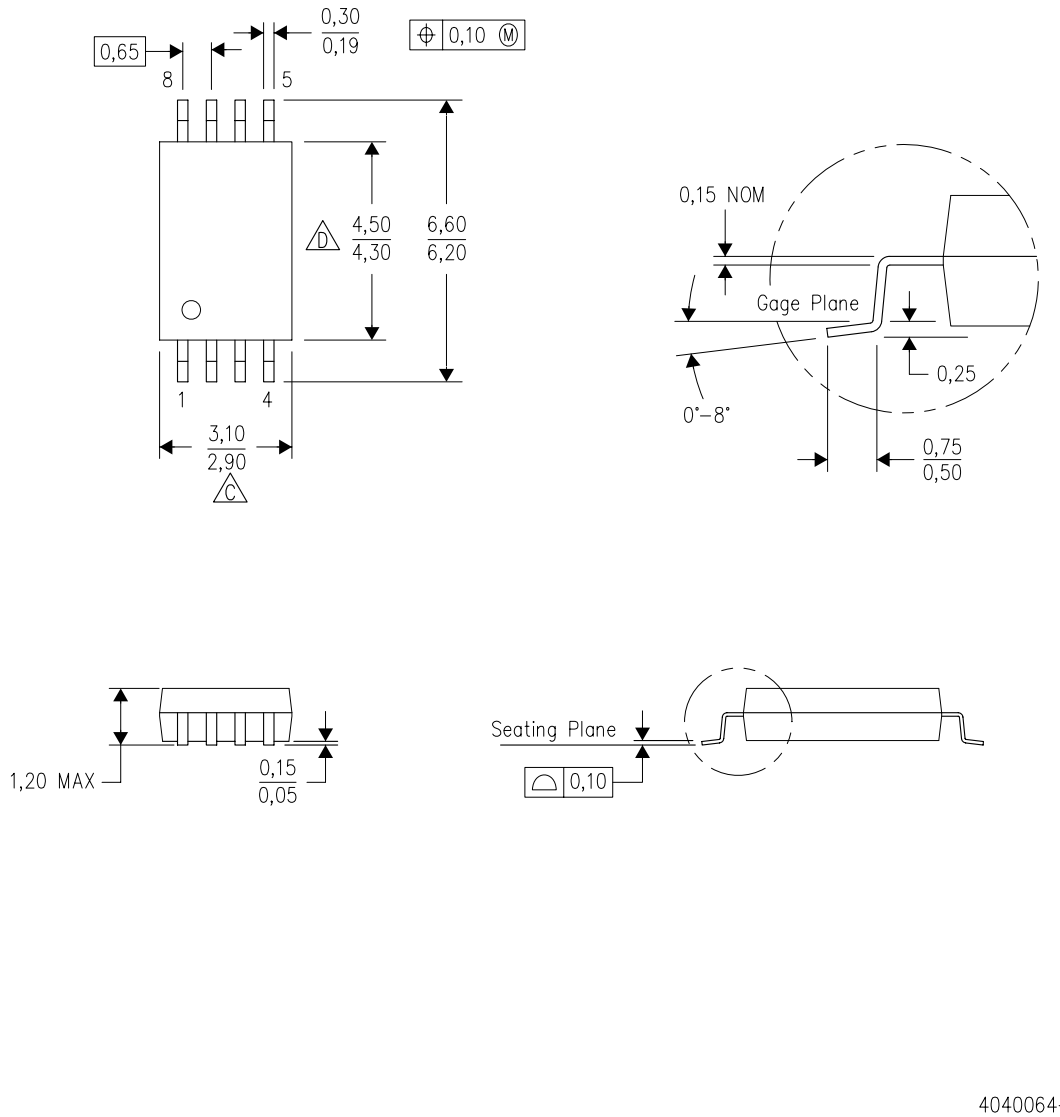
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
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D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265