Reliability Data Summary for DP8392



REF: TEST LAB FILES

RDT25406 RDT25500 RDT26562 RDT26627 RDT26638

ABSTRACT

DP8392 Coaxial Transceiver Interface parts from 8 lots were subjected to Operating Life Test, Temperature and Humidity Bias Test, Temperature Cycle Test, and Electrostatic Discharge Test.

PURPOSE OF TEST

Evaluation of new device and qualification of U.K. fab.

TESTS PERFORMED

Operating Life Test (OPL) (100°C; biased)

Operating Life Test (OPL) (125°C; biased)

Temperature and Humidity Bias Test (THBT) (85°C; 85% R.H.; biased)

Temperature Cycle Test (TMCL) (-40°C, +125°C; unbiased)

Electrostatic Discharge Test (ESD) (Human body model: R = 1500 $\Omega;$ C = 120 pF)

CONCLUSIONS

- 1. The DP8392AN exceeds the IEEE 802.3 specification of 1 million hours Mean Time Between Failure (MTBF).
- U.K. fab results are comparable to those of Santa Clara. On ESD testing all pins passed at 1000V except for pin 7 (TX⁺).

RESULTS

TEST SAMPLE DESCRIPTION/HISTOR	Y
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Lot	Device	Package	Date Code	Fab Location	Assembly Location
1	DP8392	N, 16 Leads	8509	NSSC	NSEB
2	DP8392	N, 16 Leads	8513	NSSC	NSEB
3	DP8392	N, 16 Leads	8526	NSSC	NSEB
4	DP8392	N, 16 Leads	8552	NSSC	NSEB
5	DP8392A(-4)	N, 16 Leads	8620	NSUK	NSEB
6	DP8392A(-5)	N, 16 Leads	8637	NSUK	NSEB
7	DP8392A(-5)	N, 16 Leads	8637	NSUK	NSEB
8	DP8392A(-5)	N, 16 Leads	8637	NSUK .	NSEB
9	DP8392C	N, 16 Leads	9106	NSUK	NSEB
10	DP8392C	N, 16 Leads	9106	NSUK	NSEB
11	DP8392C	N, 16 Leads	9106	NSUK	NSEB
12	DP8392C	N, 16 Leads	9106	NSUK	NSEB
13	DP8392C	N, 16 Leads	9106	NSUK	NSEB
14	DP8392C	N, 16 Leads	9106	NSUK	NSEB

				Time Point—Number of Failures					
Test	Temperature	Lot	Fab	Hours					
				168	336	500	1000	2000	
OPL	100°C	1	NSSC	0/50		0/50	0/50		
I.	100°C	2	NSSC	0/50		0/50	0/50		
	125°C	3	NSSC	0/74					
	125°C	4	NSSC	0/100	-	0/100	0/100	0/100	
	100°C	5	NSUK	0/60	l				
	100°C	6	NSUK		0/33	0/33	0/33	0/33	
	100°C	7	NSUK		0/31	0/31	0/31	0/31	
	100°C	8	NSUK		0/33	0/31	0/31	0/31	
	85°C	9	NSUK	Į		0/77	0/77		
	85°C	10	NSUK			0/77	0/77		
	85°C	11	NSUK		1	0/77	0/77	4	
	100°C	12	NSUK	0/64	}	0/64	0/64	0/64	
	100°C	13	NSUK	0/25		0/25	0/25	0/25	
	100°C	14	NSUK	0/10		0/10	0/10	0/10	
тнвт	85°C; 85% R.H.	1	NSSC	0/50		0/50	0/50		
		2	NSSC	0/50	Í	0/50	0/50		
		3	NSSC	0/75	ł	0/75	0/75	1	
		9	NSUK	0/30		0/30	0/30		
		10	NSUK	0/30	}	0/30	0/30]	
		11	NSUK	0/30		0/30	0/30		

			1		Time Poir	t-Number o	of Failures	
Test	Temperature	Lot	Fab	Hours				
				168	336	500	1000	2000
ACLV	121°C; 100% R.H.	9	NSUK	0/77		0/77		
		10	NSUK	0/66		0/66		
		11	NSUK	0/77		0/77		
	500 E				Cy	cles		
				500	1000	2000	3000	
TMCL	-40°C, +125°C	4	NSSC	0/70	0/70	0/70	0/70	
	-65°C, +150°C	9	NSUK	0/77	0/77	0/77	-	
	-65°C, +150°C	10	NSUK	0/66	0/66	0/66		a l
	-65°C, +150°C	11	NSUK	0/77	0/77	0/77	~	

ELECTROSTATIC DISCHARGE TEST (ESD) RESULTS

26 parts from 4 wafer lots were tested by the Human Body Model test condition; $R = 1500\Omega$; C = 120 pF. First ground was held common, then VEE. 5 positive and 5 negative pulses were applied for each pin/voltage combination.

Pin	Function	Voltage—Number of Fallures		
		500V	1000V	
1	CD+	0/26	0/20	
2	CD-	0/26	0/20	
3	RX+	0/26	0/20	
4	VEE	0/26	0/20	
5	VEE	0/26	0/20	
6	RX-	0/26	0/20	
7	TX+	6/26	13/20	
8	тх-	0/26	0/20	
9	HBE	0/26	0/20	
10	GND	0/26	0/20	
11	RR+	0/26	0/20	
12	V _{EE}	0/26	0/20	
13	VEE	0/26	0/20	
14	RXI	0/26	0/20	
15	тхо	0/26	0/20	
16	CDS	0/26	0/20	

Further characterization has been done to determine individual pin ESD damage thresholds. In particular, for pin 7 (TX+), 80 parts from 4 wafer lots were tested. Pin 7 ESD damage thresholds varied from 200V-300V to 2000V-3000V, with a mean of 1800V.

MTBF (MEAN TIME BEFORE FAILURE) CONSIDERATIONS

Results total:	212, 000 device hours at 125°C, 0 failures
	301,000 device hours at 100°C, 0 failures
Assume:	$E_{o} = 0.7 \text{ eV}^{\circ}$

 $P_d = 800 \text{ mW}$ $\theta_{ja} = 45^{\circ}C/W$

Chi-square statistics, 60% confidence

MTBF_{min} at 25°C ambient = 93,000,000 Then: device hours. MTBF_{min} at 70°C ambient = 5,100,000 device hours.