DN8643S

24-bit Shift Register Latch Driver IC

Overview

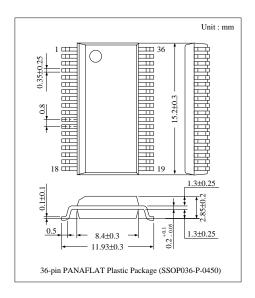
The DN8643S is an IC which incorporates a 24-bit shift register and a latch driver to meet high-speed operation, low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 24-step shift register block and latch block are composed of CMOS, and the 24-step parallel driver block is bipolar.

■ Features

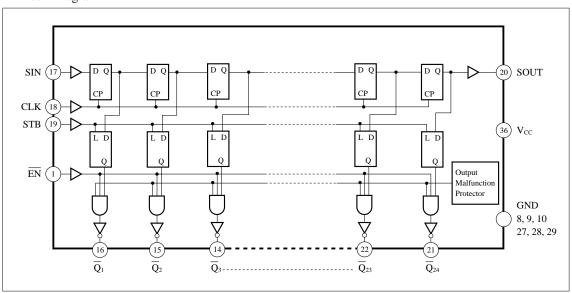
- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current at stanby $I_{CC}=\leq 100 \mu A$
- High-breakdown, large current drive type output steps

Breakdown : 30V Output current : 120mA

• Surface mountable USONF-36D package (pin pitch: 0.8mm)



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	0 to 7	V
Output voltage	Vo	0 to 30	V
Output current	Io	120	mA
Power dissipation	P_{D}	1.3 *	W
Operating ambient temperature	$T_{ m opr}$	-20 to + 75	°C
Storage temperature	T_{stg}	-55 to + 125	°C

^{*} When mounting onto the PCB, power dissipation is reduced at a rate of 10.4mW/°C from Ta=25°C

■ Recommended Operating Range (Ta=25°C)

Parameter		Symbol	Condition	mim	typ	max	Unit
Supply voltage	Supply voltage			4	5	6	V
Output voltage		Vo			_	30	V
Output current *		Io			_	100	mA
Clock frequency	Clock frequency		Input Duty 40 to 60%			10	MHz
Input pulse width	CLK	t _w -		40	_	_	ns
input puise width	STB			40	_	_	ns
Setup time	SIN			30	_	_	ns
Setup time	STB		- t _{su}			_	ns
Hold time	Hold time SIN			20	_	_	ns
Hold time	STB	t_h		0	_	_	ns
Clock pulse rise time		t _r				500	ns
Clock pulse fall time		t_{f}				500	ns

^{*} An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

■ Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V _{IH}	V _{CC} =4 to 6V	$0.7V_{CC}$		V_{CC}	V
input voltage	V _{IL}	V _{CC} =4 10 6 V	0		$0.3V_{CC}$	V
Input augrent	I _{IH}	V _{IH} =5V			25	μΑ
Input current	I_{IL}	V _{IL} =0V			-25	μΑ
Output voltage	V _{OH}	$I_O = -1\mu A$	4.9			V
Output voltage	V _{OL}	I _O =1μA	_		0.1	V
Output current	I_{OH}	V _{OH} =4.5V	-4			mA
	I_{OL}	V _{OL} =0.4V	4			mA
Output saturation voltage	V _{CE (sat) 1}	I _{OL} =100mA	_		0.4	V
	V _{CE (sat) 2}	I _{OL} =80mA			0.35	V
Output leakage current	I_{OLK1}	V _O =30V (output OFF)			50	μΑ
	I _{OLK2}	V _O =15V (output Off)	_		25	μΑ
Supply current	I_{CC1}	Total driver output OFF			100	μΑ
	I_{CC2}	Driver output 1 circuit ON			5	mA
Output malfunctioning preventive	V _{CCT} ⁺		2.9		3.9	V
circuit operating voltage *	V _{CCT}		2.6		3.6	V

^{*} Output malfunctioning preventive circuit operating voltage timing chart

Driver output

Vcc

Vcc

Vccr

Enable

OFF

Enable

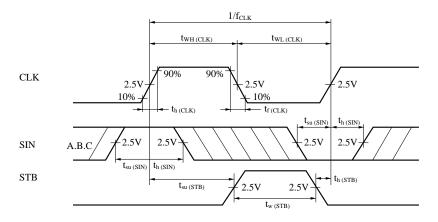
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■ Switching Characteristics (Ta=25°C)

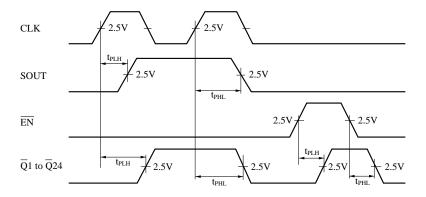
Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	f_{max}	CLK			10	_	_	MHz
Propagation delay time	t _{PLH}	CLK	SOUT	V _{CC} =5V			100	ns
	t _{PHL}			C _L =15pF			100	ns
	t _{PLH}	CLK	$ \overline{\overline{Q}n} \qquad V_{CC} = 5V $ $R_L = 100\Omega $ $\overline{Q}n \qquad C_L = 15pF $			_	2	μs
	t _{PHL}						0.5	μs
	t _{PLH}	EN				2	μs	
	t _{PHL}	LIV	ŲII	CL=13p1		_	0.5	μs

■ Timing Chart

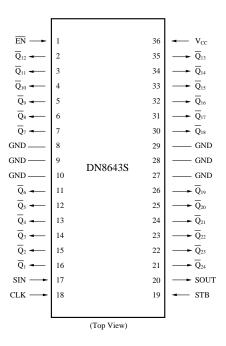
1. Input Timing



2. Propagation Delay Time



■ Pin Assignments



■ Functions Table

Input				Driver	SOUT	
CLK	EN	STB	SIN	$\overline{\mathbf{Q}}_{\mathbf{l}}$	$\overline{\mathbf{Q}}_{\mathrm{n}}$	3001
1	Н	×	×	Н	Н	Q'23
\downarrow	Н	×	×	Н	Н	nc
1	L	L	×	nc	nc	Q'23
1	L	Н	L	Н	$\overline{\overline{Q}}_{n-1}$	Q'23
1	L	Н	Н	L	$\overline{\overline{Q}}_{n-1}$	Q'23
\downarrow	L	Н	×	nc	nc	nc

Note) H=High level, L=Low level, \times = Either "H" or "L" will do, \uparrow = Transition from "H" or "L" , \downarrow = Transition from "H" to "L" , nc=No change, Q'_{23} =Status of the 23rd shift register

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