Tri-State Logic

DM7551/DM8551 tri-state quad-D flip flop

general description

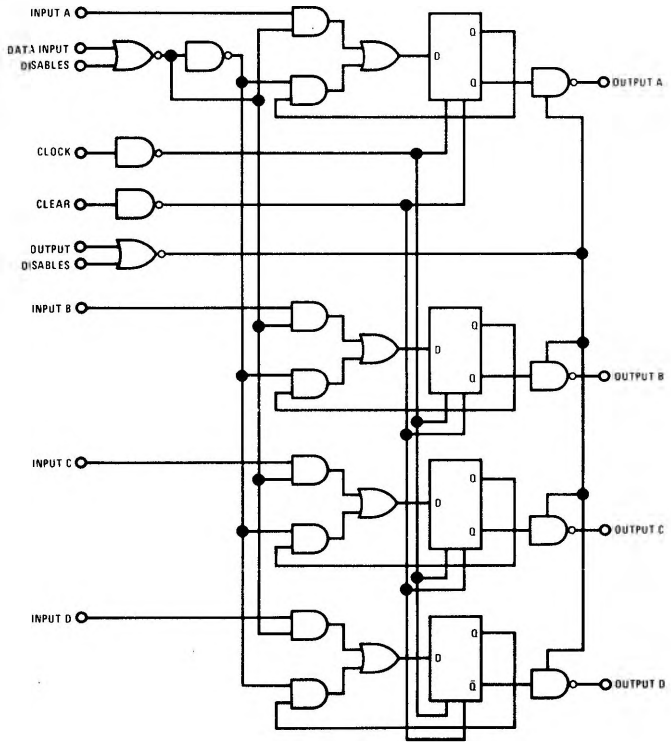
The DM7551/DM8551 is a tri-state logic device which provides four D-type flip flops in one package which operate synchronously from a common clock. Features of the device are:

- Series 54/74 compatible
- 23 ns typical propagation delay
- 250 mW typical power dissipation
- Outputs directly connectable for bus-line operation
- A "do-nothing" state accomplished without gating the clock
- Simple disable encoding

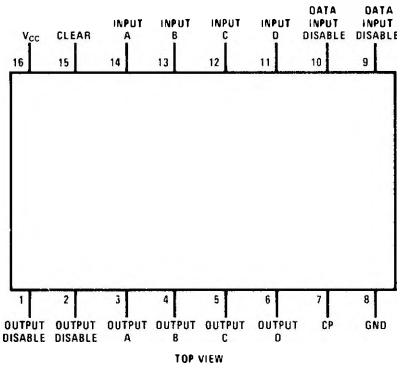
A unique three-state output allows the device to be used in bus-organized systems. The outputs can be directly wired to outputs of other DM7551/DM8551's without encountering the problems normally met with "collector-ORing" TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state.

(Continued on page 26)

logic and connection diagrams



Dual-In-Line Package



TRUTH TABLE (Both Output Disables Low)

t_n		t_{n+1} OUTPUT
DATA INPUT DISABLE	DATA INPUT	
Logical "1" on 1 or both inputs	X	On
Logical "0" on both inputs	1	1
Logical "0" on both inputs	0	0

X = Don't Care

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7551	−55°C to +125°C
	DM8551	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously		Indefinitely

electrical characteristics (Note 2)

PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7551	V_{CC} = 4.5V		2.0			V
	DM8551	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7551	V_{CC} = 4.5V				0.80	V
	DM8551	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7551	V_{CC} = 4.5V	I_{OUT} = −2.0 mA	2.4	3.3		V
	DM8551	V_{CC} = 4.75V	I_{OUT} = −5.2 mA				
Logical "0" Output Voltage	DM7551	V_{CC} = 4.5V	I_{OUT} = 16 mA		0.2	0.40	V
	DM8551	V_{CC} = 4.75V					
Logical "0" Input Current	DM7551	V_{CC} = 5.5V	V_{IN} = 0.40V		−1.0	−1.6	mA
	DM8551	V_{CC} = 5.25V					
Logical "1" Input Current	DM7551	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
	DM8551	V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Output Current	DM7551	V_{CC} = 5.5V	V_O = 2.4V			40	μA
In High Impedance State	DM8551	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Supply Current	DM7551	V_{CC} = 5.5V			50	72	mA
	DM8551	V_{CC} = 5.25V					
Output Short Current (Note 3)	DM7551	V_{CC} = 5.5V	V_{OUT} = 0.0V	−30		−70	mA
	DM8551	V_{CC} = 5.25V					
Maximum Clock Frequency		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C		25		MHz
Propagation Delay from Clock to Logical "0", t_{pd0}		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C	11	20	31	ns
Propagation Delay from Clock to Logical "1", t_{pd1}		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C	11	27	43	ns
Input Data Setup Time, $t_{S\,DATA}$		V_{CC} = 5.0V	T_A = 25°C		3	10	ns
Input Data Hold Time, $t_{H\,DATA}$		V_{CC} = 5.0V	T_A = 25°C		4	10	ns
Input Disable Setup Time, $t_{S\,DIS}$		V_{CC} = 5.0V	T_A = 25°C		10	17	ns
Input Disable Hold Time, $t_{H\,DIS}$		V_{CC} = 5.0V	T_A = 25°C		−4	2	ns
Delay from "Output Disable" to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V	T_A = 25°C	3	5	30	ns
Delay from "Output Disable" to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V	T_A = 25°C	3	11	30	ns
Delay from "Output Disable" to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V	T_A = 25°C	7	16	30	ns
Delay from "Output Disable" to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V	T_A = 25°C	7	21	30	ns
Propagation Delay from Clear to Output, t_{pdR}		V_{CC} = 5.0V	T_A = 25°C		18	27	ns

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply operating conditions.

Note 2: Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7551 and across the 0°C to 70°C temperature range for the DM8551. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only 1 output at a time should be shorted.

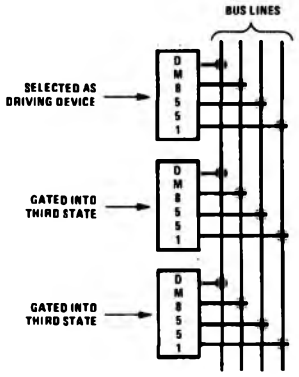


FIGURE 1

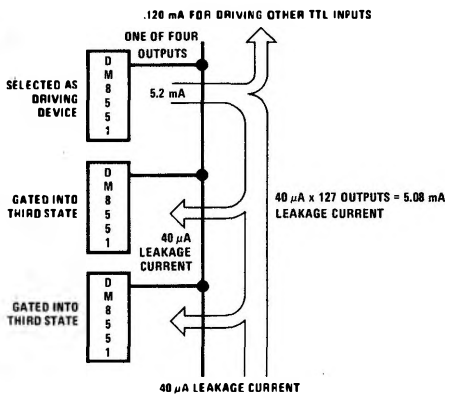


FIGURE 2

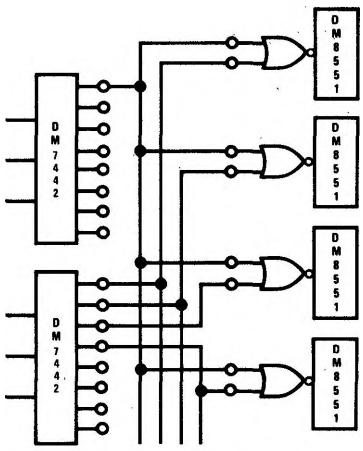


FIGURE 3

general description (con't)

The high impedance state occurs on all outputs of all devices except the four outputs of the one device selected (Figure 1). The result is that the selected device has a normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from a logical "0" to a logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs. Since the logical "1" output current of the selected device is 13 times that of a normal Series 54/74 output (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 connected devices and still retain enough drive for a full Series 54/74 fan-out of 3 at the end of the bus line (Figure 2).

A two-input NOR gate facilitates selection of the driving device through the use of only two octal decoders for as many as 64 DM7551/DM8551's (Figure 3).

A problem inherent in conventional D-type flip flops is that it is impossible to code the data input in such a way as to cause the flip flop to remain in its present state when clocked. Because flexibility is not as great as with a J-K flip flop (and its J=0, K=0 state), to keep a D-type flip flop in its present state it is usually necessary to gate the clock, which increases the danger of false-clocking. The DM7551/DM8551 contains a gated input disable which does not disrupt clocking, but rather recirculates information from the Q output to the D input. In this manner the flip flop does not change state and the possibility of false-clocking is eliminated.

The following logic levels control the device:

- Clocking occurs on the positive-going transition.
- Clearing is enabled by taking the input to a Logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a Logical "1" level.
- The flip flops will remain in their previous state when clocked so long as either of the two Data Input Disable inputs is taken to a Logical "1" level.

The DM7551/DM8551 is completely compatible with other Series 54/74 devices.

switching time waveforms