National Semiconductor

DM54LS461/DM74LS461 Octal Counter

General Description

The LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7–Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The output register (Q_7–Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

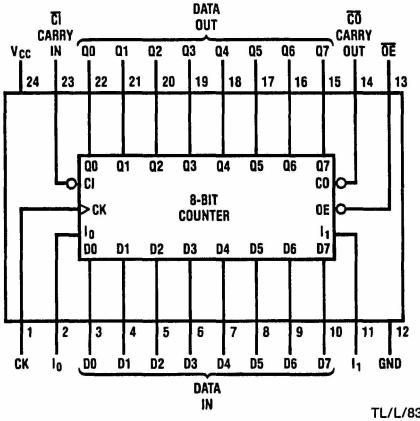
Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I_1 is HIGH, I_0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Features/Benefits

- Octal counter for microprogram-counter, DMA controller and general purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin Skinny Dip saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Connection Diagram

Top View



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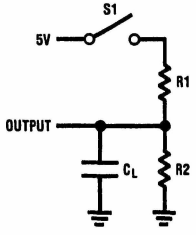
Order Number DM54LS461J, DM74LS461J or DM74LS461N
See NS Package Number J24F or N24C

Standard Test Load



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Function Table

$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_W	Width of Clock	Low	40			35			ns
		High	30			25			
t_{SU}	Set Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC}=MIN	I_I=−18 mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC}=MAX	V_I=0.4V				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC}=MAX	V_I=2.4V				25	μA
I_I	Maximum Input Current	V_{CC}=MAX	V_I=5.5V				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC}=MIN, V_{IL}=0.8V, V_{IH}=2V	MIL	I_{OL}=12 mA			0.5	V
			COM	I_{OL}=24 mA				
V_{OH}	High-Level Output Voltage	V_{CC}=MIN, V_{IL}=0.8V, V_{IH}=2V	MIL	I_{OH}=−2 mA	2.4			V
			COM	I_{OH}=−3.2 mA				
I_{OZL}	Off-State Output Current	V_{CC}=MAX, V_{IL}=0.8V, V_{IH}=2V		V_O=0.4V			−100	μA
I_{OZH}				V_O=2.4V			100	μA
I_{OS}	Output Short-Circuit Current*	V_{CC}=5.0V		V_{CC}=0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC}=MAX				120	180	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

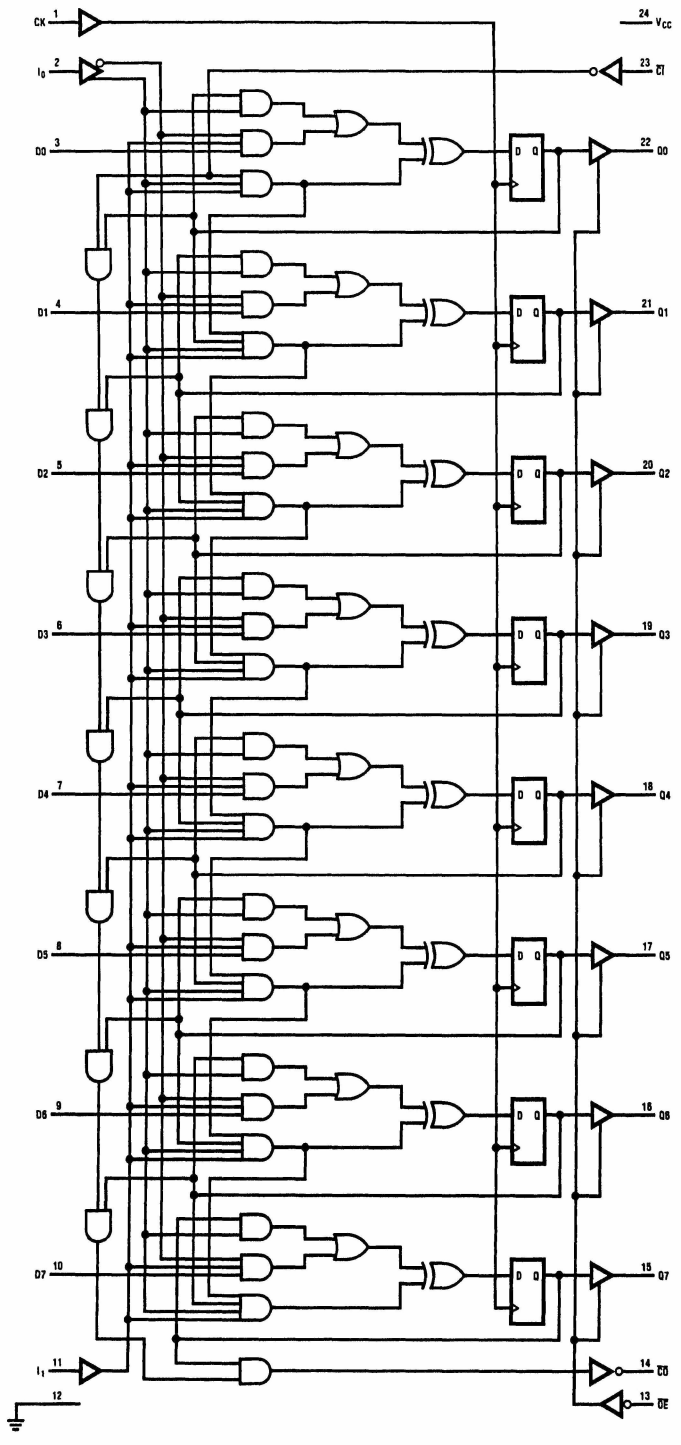
† All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	C_L=50 pF, R_1=200 Ω, R_2=390 Ω	10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ Delay			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CO}$			55	95		55	80	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram

LS461



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