DM5490/DM7490 (SN5490/SN7490)decade counter
DM5492/DM7492 (SN5492/SN7492) divide-by-twelve counter
DM5493/DM7493 (SN5493/SN7493) four-bit binary counter

general description

These TTL (Transistor-Transistor-Logic) monolithic counters are capable of counting pulses at a guaranteed frequency of 20 MHz. Gating is provided to reset the counters to the more popular states. Characteristics include high speed at moderate power dissipation, high noise immunity, and minimal variation in performance over temperature. These circuits are completely compatible with other series 54/74 devices.

To provide greater flexibility, the counters may be used in any of the modes as follows:

DM5490/DM7490

1. BCD decade counter—connect the A output to the BD input. This is the normal mode of operation.
2. Symmetrical divide-by-ten operation—connect the D output to the A input. When pulses are then applied to the BD input, a symmetrical waveform one tenth of the applied frequency will appear at the A output.
3. Divide-by-five operation—if no external connections are made a frequency division of five will result between the BD input and the D output. This allows the flip flop A to be used to divide-by-two if desired.

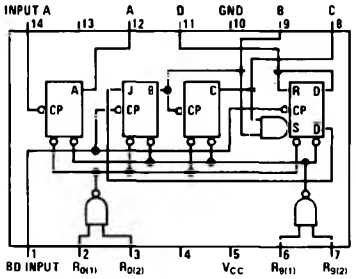
DM5492/DM7492

1. When used as a divide-by-twelve counter output A is connected to the BC input. In this mode outputs A, C, and D provide divisions by 2, 6, and 12 respectively.
2. When the connection is not made between A and BC, and when an input frequency is applied to the BC input, a frequency division of 3 and 6 results on the C and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

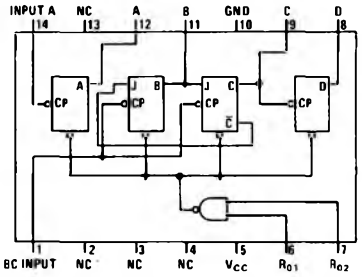
DM5493/DM7493

1. When used as a four-bit binary counter, output A is connected to the B input. In this mode outputs A, B, C, and D provide divisions by 2, 4, 8, and 16 respectively.
2. When the connection is not made between A and B and when an input frequency is applied to the B input, a frequency division of 2, 4 and 8 results on the B, C, and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

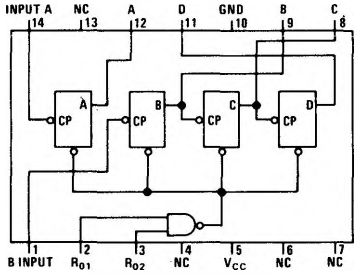
logic and connection diagrams



DM5490/DM7490



DM5492/DM7492



DM5493/DM7493

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM5490, DM5492, DM5493	−55°C to +125°C
DM7490, DM7492, DM7493	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA		−1.0	−1.5	mA
Logical "1" Input Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM5490, 92 ,93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V				.8	V
Logical "1" Output Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = 16 mA		.2	.4	V
Logical "1" Input Current	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Output Short Circuit Current	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 5.5V / V_{CC} = 5.25V	(Note 2)	20 18		55 55	mA
DM5490/DM7490							
Logical "1" Input Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						40	μA
A						80	μA
BD						160	μA
Logical "0" Input Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						1.6	mA
A						3.2	mA
BD						6.4	mA
Supply Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} = 5.25V			32	45	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16 35 50 35	35 60 80 60	ns ns ns ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19 35 50 35	35 60 80 60	ns ns ns ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns
DM5492/DM7492							
Logical "1" Input Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$						40	μA
A						80	μA
BC						160	μA

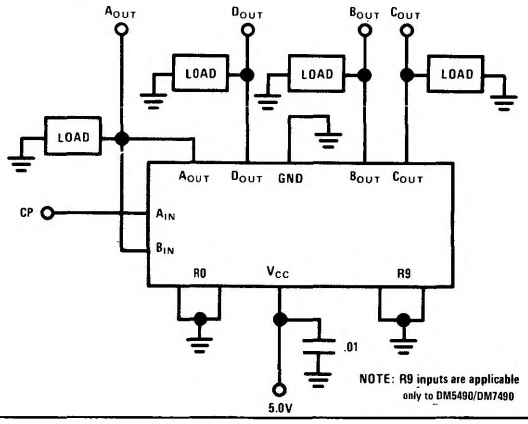
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DM5492/DM7492 (Continued)							
Logical "0" Input Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A						3.2	mA
BC						6.4	mA
Supply Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} (R_0) = 4.5V		30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input A to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16	35	ns
	B				35	60	ns
	C				35	60	ns
	D				50	80	ns
Propagation Delay Time to a Logical "0" Level From Input A to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19	35	ns
	B				35	60	ns
	C				35	60	ns
	D				50	80	ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns
DM5493/DM7493							
Logical "1" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$						40	μA
A, B						80	μA
Logical "0" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A, B						3.2	mA
Supply Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V			30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16	35	ns
	B				35	60	ns
	C				50	80	ns
	D				65	100	ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19	35	ns
	B				35	60	ns
	C				50	80	ns
	D				64	100	ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns

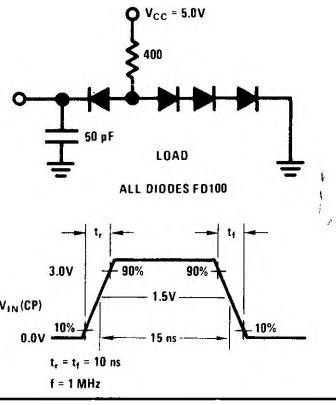
Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5490, DM5492 and DM5493 and 0°C to 70°C for the DM7490, DM7492 and DM7493 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Only one output may be shorted at a time.

Note 3: The flip flop will always recognize a 15 ns pulse.

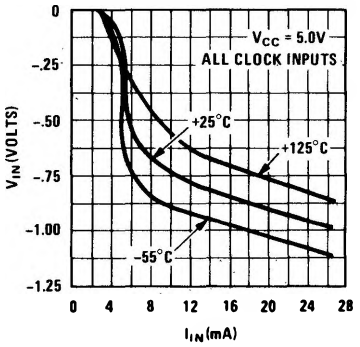
ac test circuit



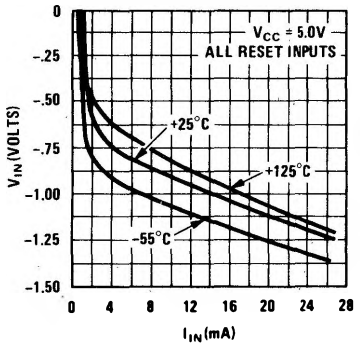


typical performance characteristics

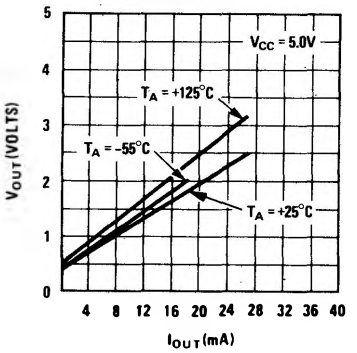
Input Clamp Diode Characteristic



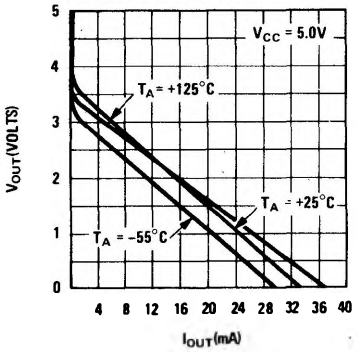
Input Clamp Diode Voltage



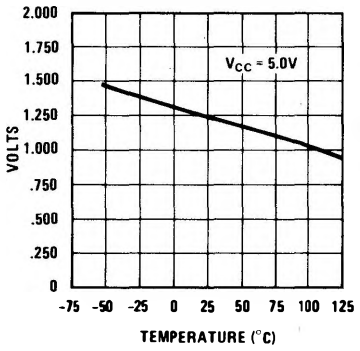
Logical "0" Output Voltage vs Sink Current



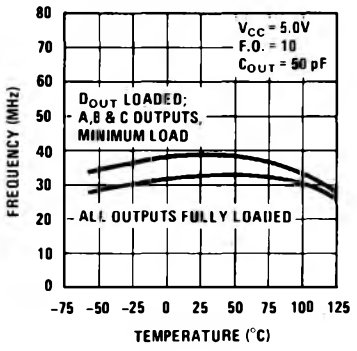
Logical "1" Output Voltage vs Source Current



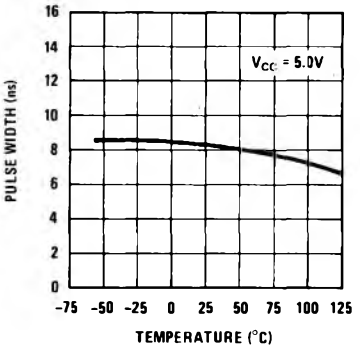
Clock Threshold vs Temperature



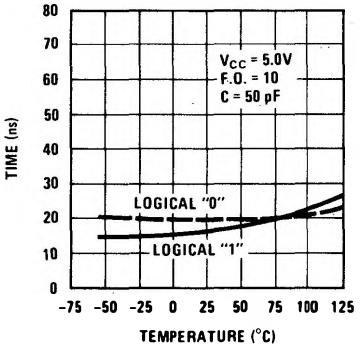
Maximum Frequency vs Temperature



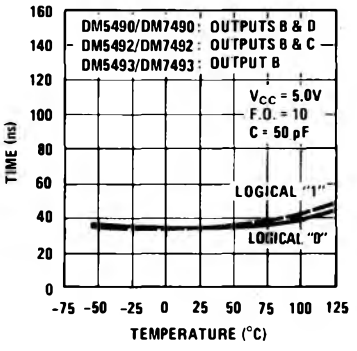
Minimum Clock Pulse Width vs Temperature



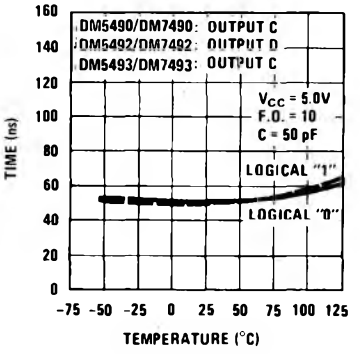
Transition Time to Output A



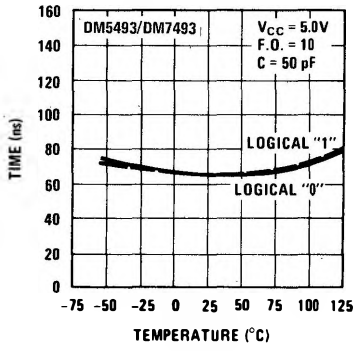
Transition Time to Outputs B, C, & D



Transition Time to Outputs C & D



Transition Time to Output D



BCD count sequence

DM5490/DM7490

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET OPERATION

To reset the counter to the BCD count of zero, both Reset 0 inputs must be at logical "1" levels while at least one Reset 9 input is at a logical "0" level.

To reset the counter to the BCD count of nine, both Reset 9 inputs must be at logical "1" levels; while at least one Reset 0 input is at a logical "0".

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs and at least one of the Reset 9 inputs must be at a logical "0" for proper counting.
3. For ÷ 10 counting, connect the A output to the BD input.

count sequence

DM5492/DM7492

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷12 counting, connect the A output to the BC input.

DM5493/DM7493

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷16 counting, connect the A output to the B input.