Tri-State Logic

DM7230/DM8230 tri-state demultiplexer general description

The DM7230/DM8230 demultiplexer is another device in National's tri-state logic family.

Digital signals applied to two input lines can be routed to two-of-four output lines depending upon the logic on the Address inputs. Outputs can be directly connected to other similar outputs for use in bus-organized systems.

features

- Series 54/74 compatible
- 20 ns propagation delay
- Data complement capability
- Very low output impedance—high drive capability
- Separate input disable controls
- High-impedance output state which allows many outputs to be connected to a common bus-line.

mode of operation

COMPLEMENT AND DATA INPUTS

When Complement A is a logical "1", Data A will appear inverted at the output. When Complement A is a logical "0", Data A will appear non-inverted at the output.

This function is accomplished on the chip through the use of a two-input exclusive-OR gate with Complement A and Data A as the two inputs. Therefore, the A information that is routed to the outputs is actually (Complement A ⊕ Data A). That this is the case may be verified by examining the logic diagram.

The two inputs of this exclusive-OR gate have identical characteristics, allowing the functions of these two inputs to be reversed. Also the propagation delay from either input to the output will be the same. This is also true for the Complement B and Data B inputs.

ADDRESS INPUTS

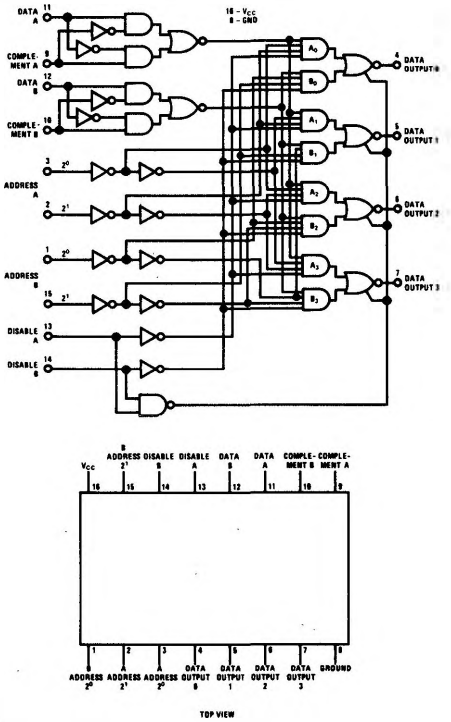
The Address A inputs select to which of the four outputs A information will be routed. The same is true for the Address B inputs and B information. If A and B information are both routed to the same output simultaneously, that output will be a logical "0" if either the A or B information is a logical "0". All outputs which are not selected for either A or B information will be in the logical "1" state.

DISABLE INPUTS

The Disable inputs are similar to higher order Address inputs in that when Disable A is a logical "1", A information is not routed to any output. All four outputs are nonselected for A information. The same is true for Disable B and B information. The Disable inputs have the additional feature that when both Disable A and Disable B are a logical "1" all outputs go to the High Impedance state. When multiple outputs are connected to a bus line, only one device at a time can be in the

(Continued on Page 22)

logic and connection diagrams



logic table

DATA A	COMP. A	DATA B	COMP. B	ADDRESS A 2^1	ADDRESS A 2^0	ADDRESS B 2^1	ADDRESS B 2^0	DIS. A	DIS. B	OUT 0	OUT 1	OUT 2	OUT 3
0	0	X	X	0	0	X	X	0	1	0	1	1	1
0	1	X	X	0	0	X	X	0	1	1	1	1	1
1	0	X	X	0	0	X	X	0	1	0	1	1	1
1	1	X	X	0	0	X	X	0	1	1	1	1	1
0	0	X	X	0	1	X	X	0	1	1	0	1	1
0	1	X	X	0	1	X	X	0	1	1	1	1	1
1	0	X	X	0	1	X	X	0	1	1	1	1	1
1	1	X	X	0	1	X	X	0	1	1	1	0	1
0	0	X	X	1	0	X	X	0	1	1	1	1	0
0	1	X	X	1	0	X	X	0	1	1	1	1	1
1	0	X	X	1	0	X	X	0	1	1	1	1	1
1	1	X	X	1	0	X	X	0	1	1	1	0	1
0	0	X	X	1	1	X	X	0	1	1	1	1	0
0	1	X	X	1	1	X	X	0	1	1	1	1	1
1	0	X	X	1	1	X	X	0	1	1	1	1	1
1	1	X	X	1	1	X	X	0	1	1	1	1	0
X	X	0	0	X	X	0	0	1	0	0	1	1	1
X	X	0	1	X	X	0	0	1	0	1	1	1	1
X	X	1	0	X	X	0	0	1	0	1	1	1	1
X	X	1	1	X	X	0	0	1	0	0	1	1	1
X	X	0	0	X	X	0	1	1	0	1	0	1	1
X	X	0	1	X	X	0	1	1	0	1	1	1	1
X	X	1	0	X	X	0	1	1	0	1	1	0	1
X	X	1	1	X	X	0	1	1	0	1	1	1	1
X	X	0	0	X	X	1	0	1	0	1	0	1	1
X	X	0	1	X	X	1	0	1	0	1	1	1	1
X	X	1	0	X	X	1	0	1	0	1	1	0	1
X	X	1	1	X	X	1	0	1	0	1	1	1	0
X	X	0	0	X	X	1	1	1	0	1	1	1	1
X	X	0	1	X	X	1	1	1	0	1	1	1	1
X	X	1	0	X	X	1	1	1	0	1	1	1	1
X	X	1	1	X	X	1	1	1	0	0	1	1	1
X	X	X	X	X	X	X	X	1	1	Hi Z	Hi Z	Hi Z	Hi Z

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously. (5% duty cycle)	10 msec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7230	−55°C to +125°C
DM8230	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7230	V_{CC} = 4.5V	2.0			V
	DM8230	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7230	V_{CC} = 4.5V			0.8	V
	DM8230	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7230	V_{CC} = 4.5V, I_{OUT} = −2 mA	2.4	3.5		V
	DM8230	V_{CC} = 4.75V, I_{OUT} = −5.2 mA				
Logical "0" Output Voltage	DM7230	V_{CC} = 4.5V				
	DM8230	V_{CC} = 4.75V I_{OUT} = 16 mA		0.2	0.4	V
Logical "0" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 0.4V				
		Disable inputs		−2.0	−3.2	mA
		All other inputs		−1.0	−1.6	mA
Logical "1" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 2.4V				
		Disable inputs			80	μA
		All other inputs			40	μA
Logical "1" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 5.5V			1.0	mA
Output Disable Current	DM7230	V_{CC} = 5.5V V_O = 2.4V			40	μA
	DM8230	V_{CC} = 5.25V V_O = 0.4V			−40	μA
Output Short Current (Note 2)	DM7230	V_{CC} = 5.5V	−30			
	DM8230	V_{CC} = 5.25V V_O = 0.0V	−28		−70	mA
Supply Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 5.0V		48	75	mA
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Output Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C				
		I_{OUT} = −12 mA			−1.5	V
		I_{OUT} = +12 mA			V_{CC} +1.5	V
Propagation Delay to Logical "1" from Data or Complement Input, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF				
		Noninverting		13	24	ns
		Inverting		20	36	ns
Propagation Delay to Logical "0" from Data or Complement Input, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF				
		Noninverting or Inverting		18	26	ns
Propagation Delay to Logical "1" from Address Input, t_{pd1} (Note 3)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		20	36	ns
Propagation Delay to Logical "0" from Address Input, t_{pd0} (Note 3)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		20	30	ns
Propagation Delay to Logical "1" from Disable Input, t_{pd1} (Note 4)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		13	25	ns
Propagation Delay to Logical "0" from Disable Input, t_{pd0} (Note 4)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		16	25	ns
Delay from Disable Input to High Impedance State (Note 5), t_{IH}		V_{CC} = 5.0V, T_A = 25°C		7	14	ns
t_{OH}				15	27	ns
Delay from Disable Input to Low Impedance State (Note 5), t_{HI}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		15	23	ns
t_{HO}				18	27	ns

Note 1: Min/max values apply across the −55°C to +125°C temperature range for the DM7230 and across the 0°C to 70°C range for the DM8230 unless otherwise specified. Typicals are given for T_A = 25°C and V_{CC} = 5.0V.

Note 2: Only one output at a time should be short circuited.

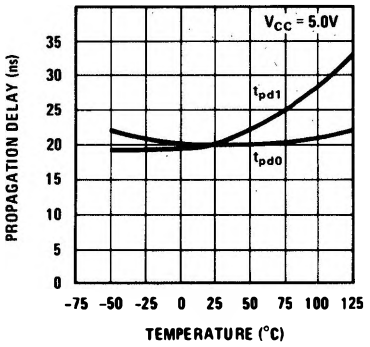
Note 3: The only conditions under which a t_{pd0} from the Address inputs can be observed is when an output goes from being nonselected to being selected and the information being routed to that output is a logical "0". If the information had been a logical "1", no change would have occurred and no measurement could have been made. Similarly, the only time a t_{pd1} from the Address inputs can be observed, is when an output goes from being selected to being nonselected and the information that had been routed to that output was a logical "0". If the information had been a logical "1", no change would have occurred and no measurement could have been made.

Note 4: Information in Note 3 concerning t_{pd0} and t_{pd1} from the address inputs are applicable here also.

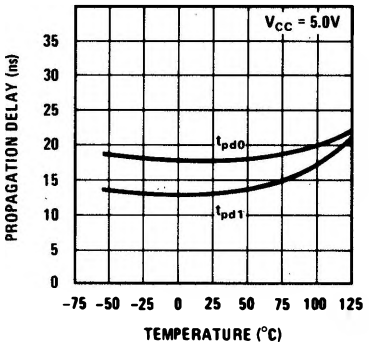
Note 5: All delays involving transitions to or from the High Impedance state are measured with respect to the Disable inputs. For example, with A information at a logical "0" and Disable B at a logical "1" the selected output will go from a logical "0" to the High Impedance state some time, t_{OH}, after Disable A has gone from a logical "0" to a logical "1"

typical performance

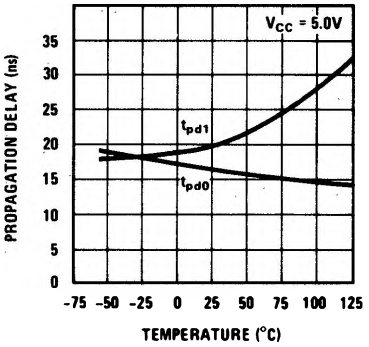
Propagation Delay from Address to Output (Inverted)



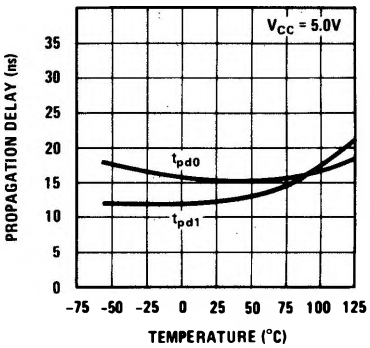
Propagation Delay from Data or Complement to Output (Noninverted)



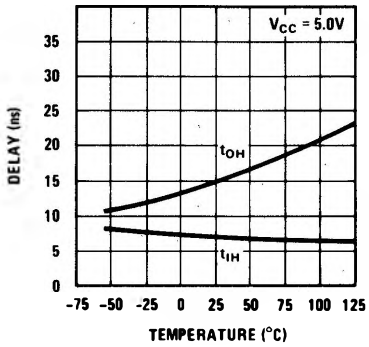
Propagation Delay from Data or Complement to Output (Inverted)



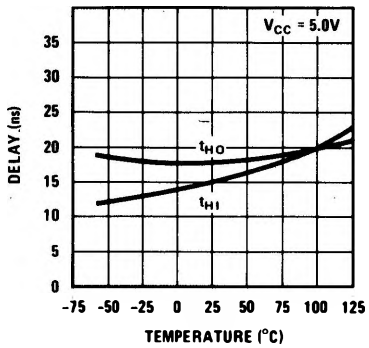
Propagation Delay from Disable to Output



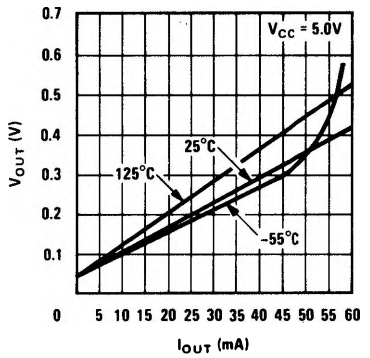
Delay from Disable to High Impedance State



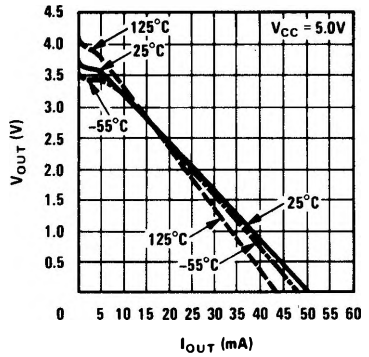
Delay from Disable to Low Impedance State



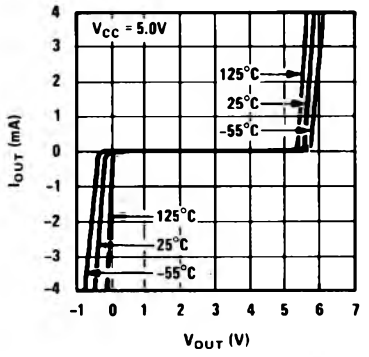
Logical "0" Output Voltage vs Sink Current



Logical "1" Output Voltage vs Source Current



I_{OUT} vs V_{OUT} High Impedance Output State



mode of operation (cont.)

normal low impedance state. All others should be gated into the high impedance state (Figure 1). The selected device therefore has the normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current of the selected device is 13 times that of a conventional Series 54/74 device (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 other DM7230/DM8230's and still have available drive for the bus-line. (Figure 2)

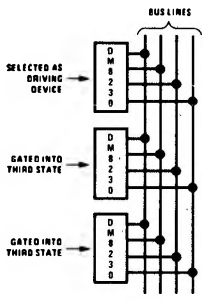


Figure 1

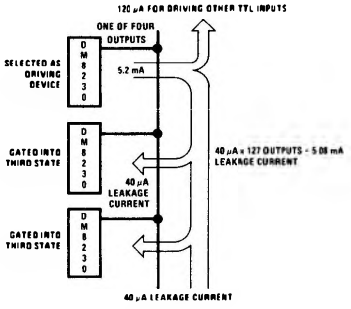
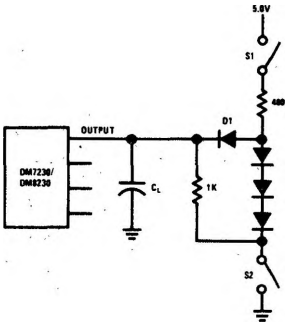


Figure 2

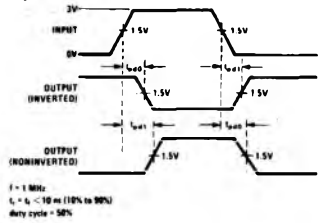
ac test circuit



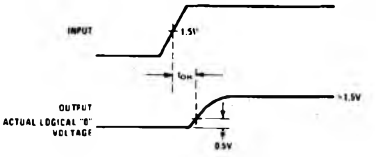
	SWITCH S1	SWITCH S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	5 pF
t_{IH}	closed	closed	5 pF
t_{HO}	closed	open	50 pF
t_{HI}	open	closed	50 pF

switching time waveforms

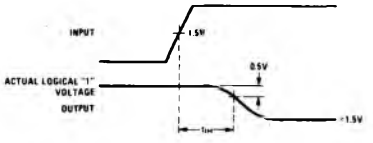
t_{pd1} & t_{pd0}



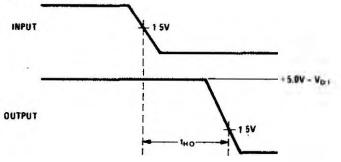
t_{OH}



t_{IH}



t_{HO}



t_{HI}