DM54LS377,DM74LS377

DM54LS377 DM74LS377 Octal D Flip-Flop with Common Enable and Clock

Literature Number: SNOS308A

National Semiconductor

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DM54LS377/DM74LS377
Octal D Flip-Flop with Common Enable and Clock

General Description

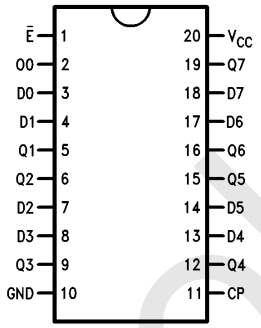
The 'LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

Features

- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

Connection Diagram

Dual-In-Line Package



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Order Number DM54LS377E, DM54LS377J, DM54LS377W, DM74LS377WM or DM74LS377N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q7	Flip-Flop Outputs

Obsolete

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS377			DM74LS377			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0			5.0 5.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	10 20			10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0			5.0 5.0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				28	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Obsolete

Switching Characteristics $V_{CC} = +5.0V, T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega, C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		25 25	ns

Functional Description

The 'LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

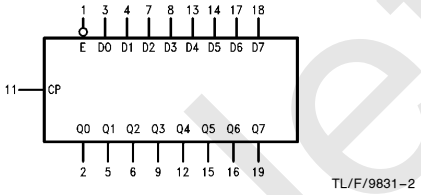
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	X	X	No Change
L	⌐⌐	H	H
L	⌐⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Symbol



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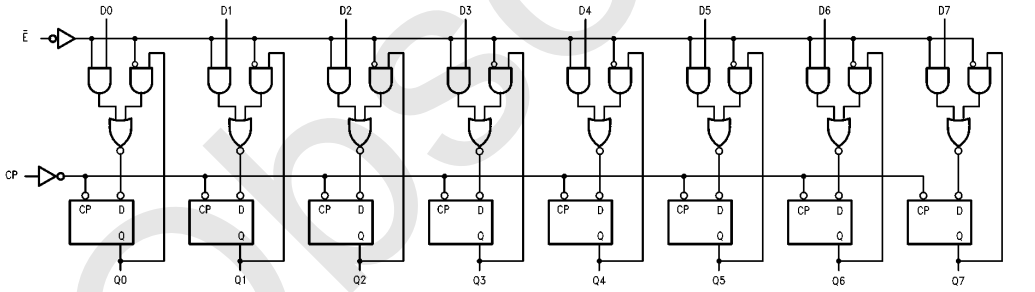
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram



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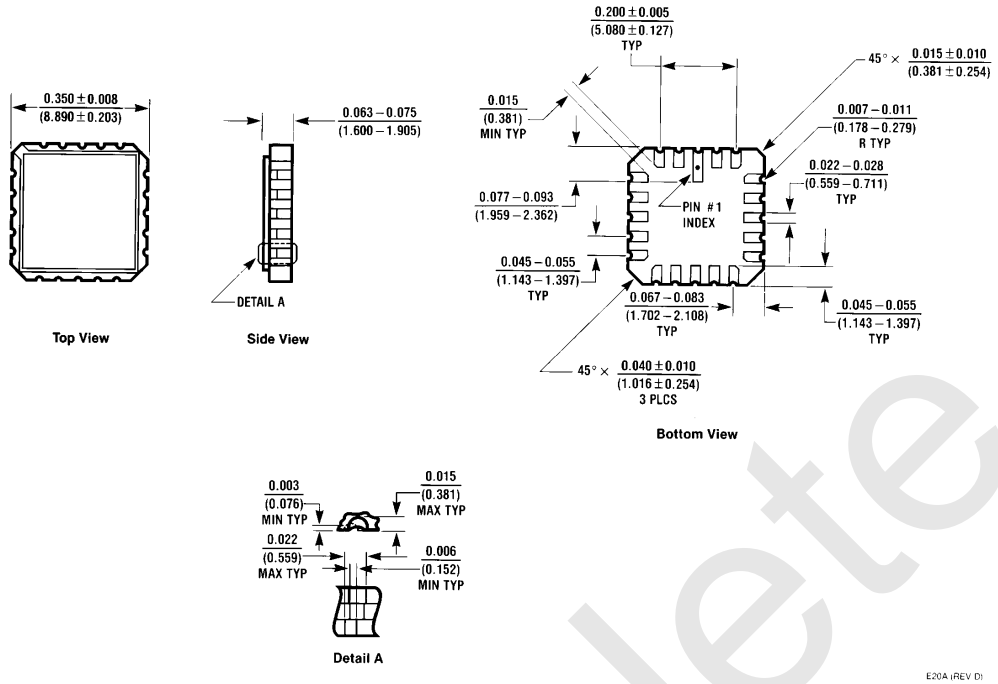
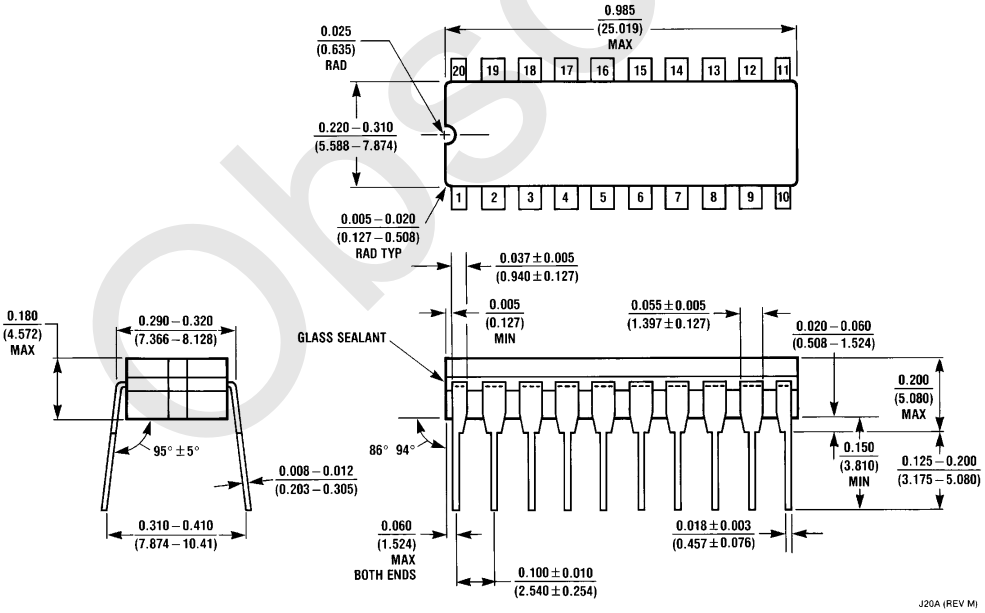
Obsolete

Physical Dimensions inches (millimeters)



E20A (REV D)

Ceramic Leadless Chip Carrier (E)
Order Number DM54LS377E
NS Package Number E20A

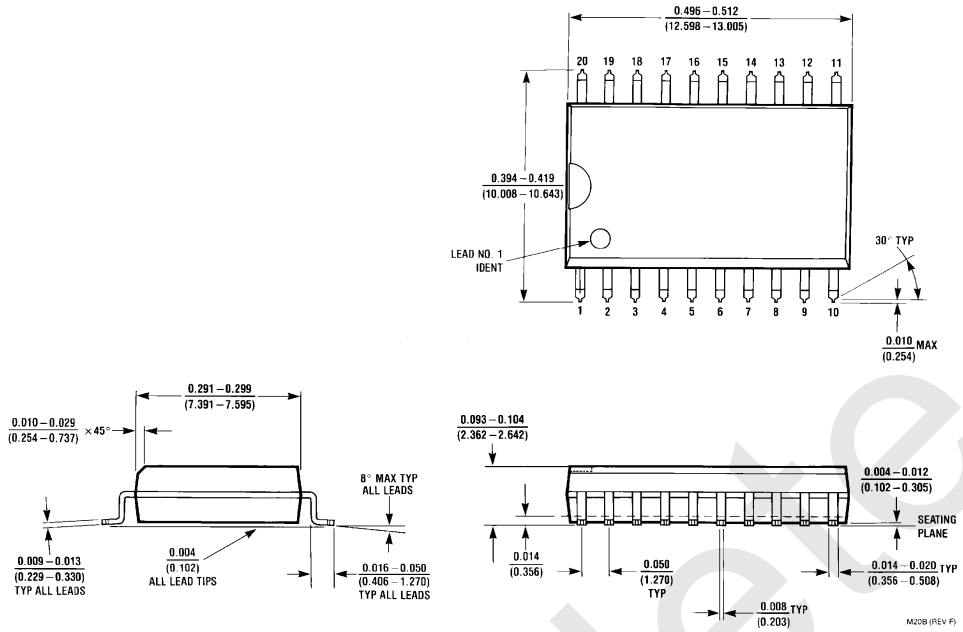


J20A (REV M)

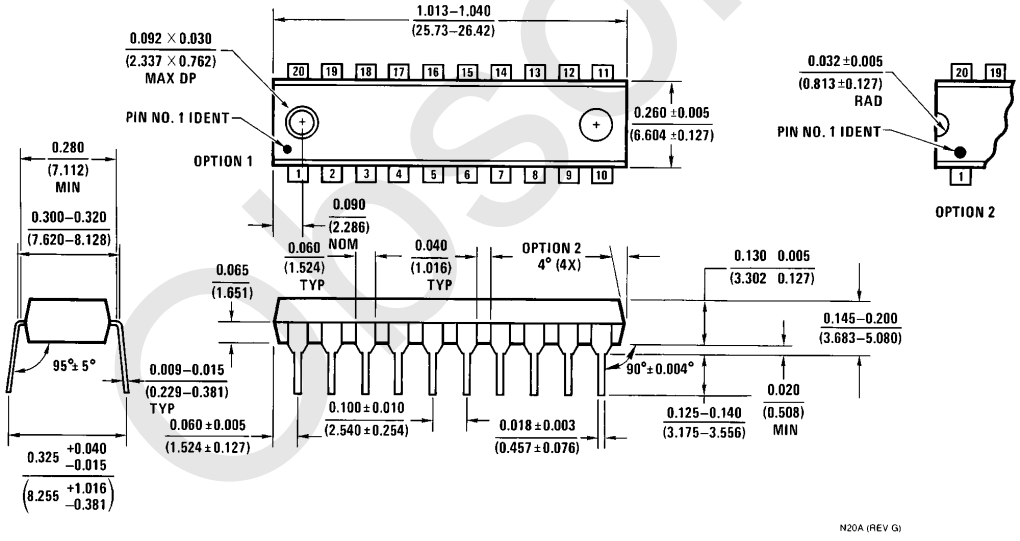
20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS377J
NS Package Number J20A

Obsolete

Physical Dimensions inches (millimeters) (Continued)



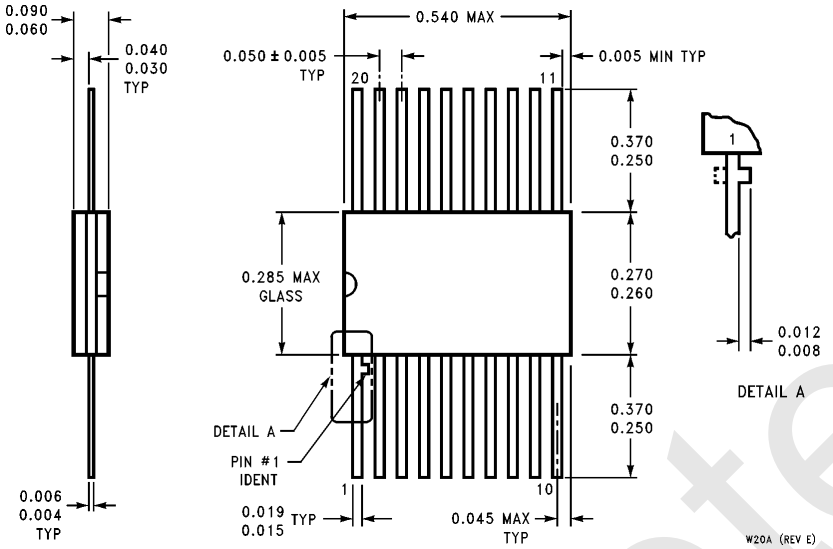
20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS377WM
NS Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS377N
NS Package Number N20A

Obsolete

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS377W
NS Package Number W20A

Obsolete

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

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