DG5143

Low-Power, High-Speed CMOS Analog Switch

Features

- ± 15-V Input Range
- On-Resistance: 50 Ω
- Fast Switching Action—t_{ON}: 100 ns
- Low Power—P_D: <350 µW
- TTL and CMOS Compatible

Benefits

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

Applications

- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery Powered Systems

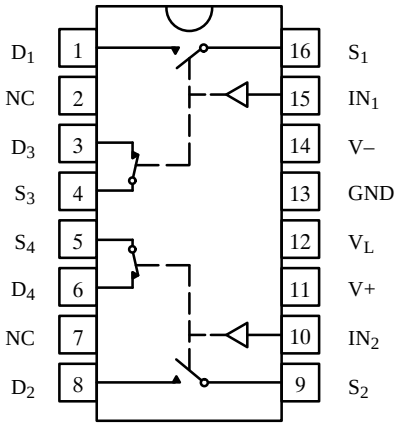
Description

The DG5143 solid state analog switch is built on the Siliconix proprietary high-voltage silicon gate process to achieve high voltage rating and superior switch time on/off performance. Break-before-make switching action guarantees that an on-channel will be turned off before the off-channel can turn on. The DG5143 features ultra-low power supply requirements and TTL and CMOS compatibility.

Each switch conducts equally well in both directions when on and blocks input voltages to the supply values when off. This switch is ideal for battery powered industrial applications with a maximum power supply current of 1 µA. An expitaxial layer prevents latchup.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5143CJ

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70060.

Absolute Maximum Ratings

(V+) – (V–) . . . . . < 36 V
(V+) – (V_D)[a] . . . . . < 30 V
(V_D) – (V–)[a] . . . . . < 30 V
(V_D) – (V_S)[a] . . . . . < ± 22 V
(V_L) – (V–) . . . . . < 33 V
(V_L) – (V_{IN}) . . . . . < 30 V
V_L . . . . . < 20 V
V_{IN}[a] . . . . . < 20 V

Continuous Current, Any Terminal . . . . . 30 mA
Peak Current, S or D (pulsed a 1 ms, 10% duty cycle max) . . . 100 mA
Storage Temperature . . . . . –65 to 125°
Power Dissipation (Package)[b]
16-Pin Plastic DIP . . . . . 450 mW

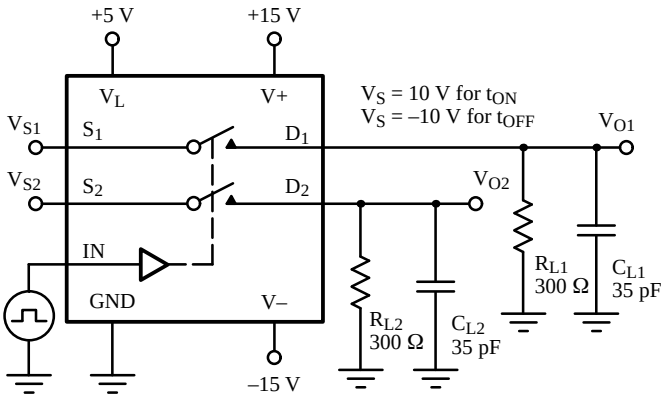
Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_L = 5 V V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	 Typ[b]	 Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ± 10 V, I_S = – 10 mA	Room Full			75 100	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ∓ 10 V, V_S = ± 10 V	Room Full	–5 –20		5 20	nA
	$I_{D(off)}$		Room Full	–5 –20		5 20	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = –10 to 10 V	Room Full	–2 –40		2 40	
Digital Control							
Input Current with V_{IN} Low	I_{IL}		Full	–1		1	µA
Input Current with V_{IN} High	I_{IH}		Full	–1		1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 1	Room			175	ns
Turn-Off Time	t_{OFF}		Room			150	
Break-Before-Make	$t_{ON} - t_{OFF}$		Room			5	
Charge Injection[d]	Q	C_L = 10,000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room			150	pC
Off Isolation[d]	OIRR	R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	Room	–50			dB
Channel-to-Channel Crosstalk[d]	X_{TALK}	Any Other Channel Switches R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	Room			–50	
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or 5 V Switch Duty Cycle <10%	Room			10	µA
Negative Supply Current	I–		Room	–10			
Logic Supply Current	I_L		Room			10	
Ground Current	I_{GND}		Room	–10			

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Test Circuits



C_L (includes fixture and stray capacitance)

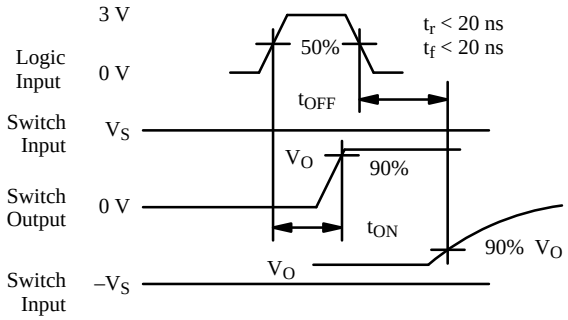


Figure 1. Switching Time