DG381A/384A/387A/390A

CMOS Analog Switches

Features

- ± 15-V Input Range
- Low $r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

Benefits

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Sytems

Description

The DG381A–DG390A series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat on-resistance over the entire voltage range.

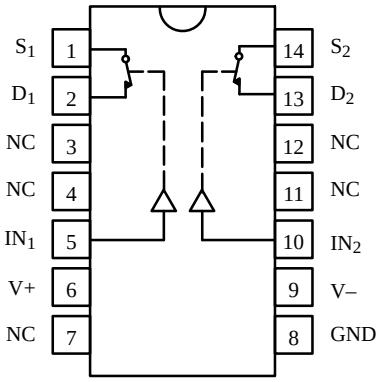
Designed on Siliconix' PLUS-40 CMOS process, these devices achieve low power consumption (3.5 mW typical) and excellent on/off switch performance. These switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the V– rail to 0 V.

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS and quasi TTL logic compatible.

Functional Block Diagram and Pin Configuration

DG381A

Dual-In-Line



Top View

Truth Table

Logic	Switch
0	ON
1	OFF

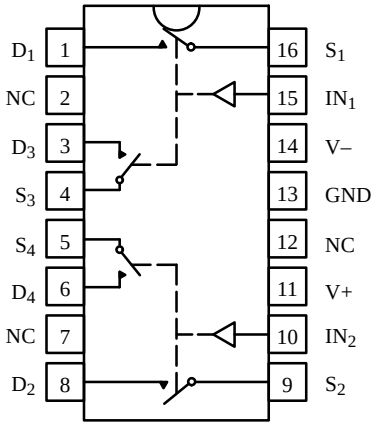
Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70048.

Functional Block Diagram and Pin Configuration (Cont'd)

DG384A

Dual-In-Line



Top View

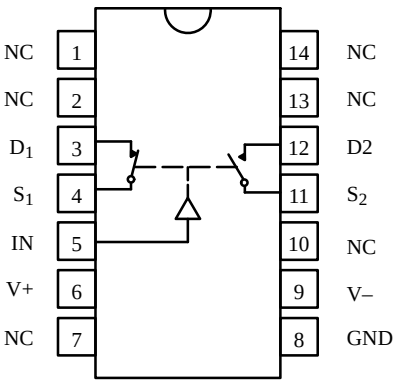
Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

DG387A

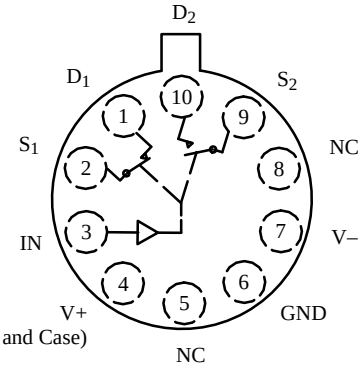
Dual-In-Line



Top View

DG387A

Metal Can



(Substrate and Case)

Top View

Truth Table

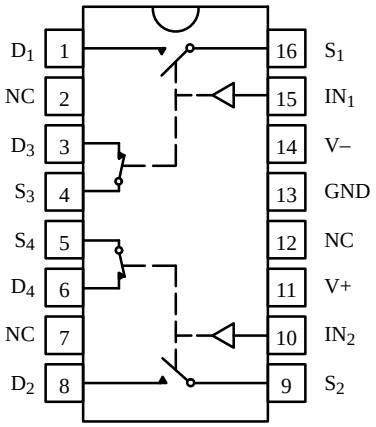
Logic	SW_1	SW_2
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Functional Block Diagram and Pin Configuration (Cont'd)

DG390A

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Ordering Information

Temp Range	Package	Part Number
DG381A		
0 to 70°C	14-Pin Plastic DIP	DG381ACJ
–55 to 125°C	14-Pin CerDIP	DG381AAK/883
DG384A		
0 to 70°C	16-Pin Plastic DIP	DG384ACJ
–55 to 125°C	16-Pin CerDIP	DG384AAK/883
DG387A		
0 to 70°C	14-Pin Plastic DIP	DG387ACJ
–55 to 125°C	14-Pin CerDIP	DG387AAK/883
	10-Pin Metal Can	DG387AAA/883
DG390A		
0 to 70°C	16-Pin Plastic DIP	DG390ACJ
–25 to 85°C	16-Pin CerDIP	DG390ABK
–55 to 125°C		DG390AAK
		DG390AAK/883

Absolute Maximum Ratings

Voltages Referenced to V–

V+ . . . . . 44 V

GND . . . . . 25 V

Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D . . . . . 30 mA

Continuous Current, S or D . . . . . 30 mA

(Pulsed at 1 ms, 10% duty cycle max) . . . . . 100 mA

Storage Temperature (AAA, AAK, ACK Suffix) . . –65 to 150°C

(ACJ Suffix) . . . . . –65 to 125°C

Power Dissipation[b]

14-Pin Plastic DIP[d] . . . . . 470 mW

14-Pin CerDIP[c] . . . . . 825 mW

10-Pin Metal Can[e] . . . . . 450 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 11 mW/°C above 75°C

d. Derate 6.5 mW/°C above 25°C

e. Derate 6 mW/°C above 75°C

Schematic Diagram (Typical Channel)

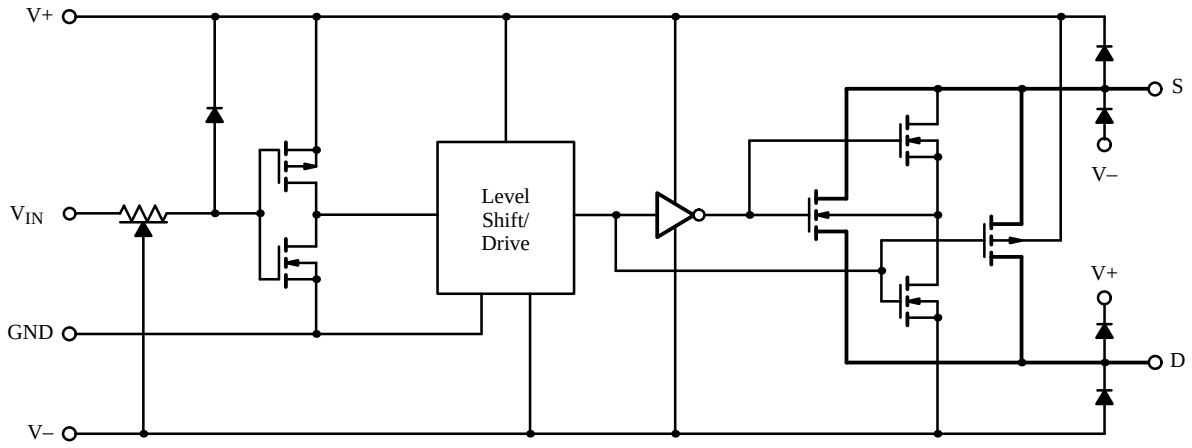


Figure 1.

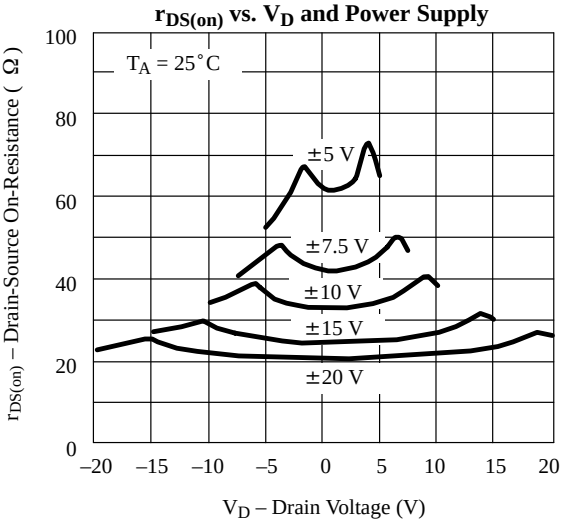
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 0.8 V or 4 V[f]		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	B, C Suffix 0 to 70°C, –25 to 85°C Min[d]	B, C Suffix 0 to 70°C, –25 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –10 mA		Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V		Room Hot	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V		Room Hot	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V		Room Hot	±0.1	–11 –100	1 100	–5 –100	5 100	nA
Digital Control										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V		Room Full	–0.001	–1 –1		–1		µA
		V_{IN} = 15 V		Room Full	0.001		1 1		1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V		Room Full	–0.001	–1 –1		–1		µA
Dynamic Characteristics										
Turn-On Time	t_{ON}	See Figure 2		Room	150		300			ns
Turn-Off Time	t_{OFF}	See Figure 2		Room	130		250			ns
Break-Before-Make Time	t_{OPEN}	See Figure 3		Room	50					ns
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 0 Ω V_{gen} = 0 V		Room	10					pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz; V_S, V_D = 0 V		Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz; V_S, V_D = 0 V		Room	14					pF
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz; V_S, V_D = 0 V		Room	40					pF
Input Capacitance	C_{IN}	f = 1 MHz	V_{IN} = 0 V	Room	6					pF
			V_{IN} = 15 V	Room	7					pF
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz		Room	62					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz		Room	74					dB
Power Supplies										
Positive Supply Current	I+	V_{IN} = 4 V (One Input) (All Others = 0)		Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I–	V_{IN} = 4 V (One Input) (All Others = 0)		Room Full	–0.001	–10 –100		–100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)		Room Full	0.001		10 100		100	µA
Negative Supply Current	I–	V_{IN} = 0.8 V (All Inputs)		Room Full	–0.001	–10 –100		–100		µA

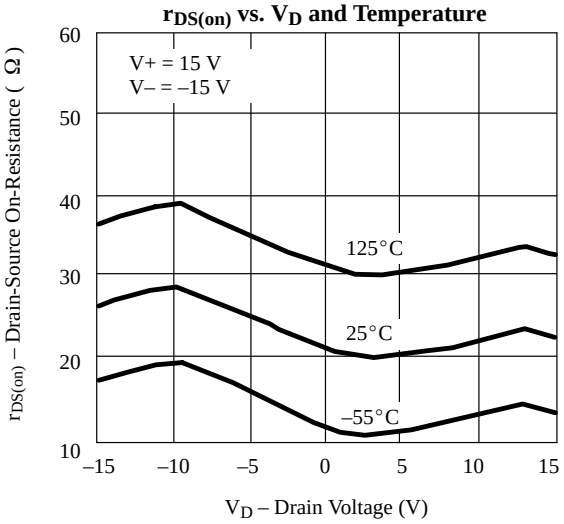
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

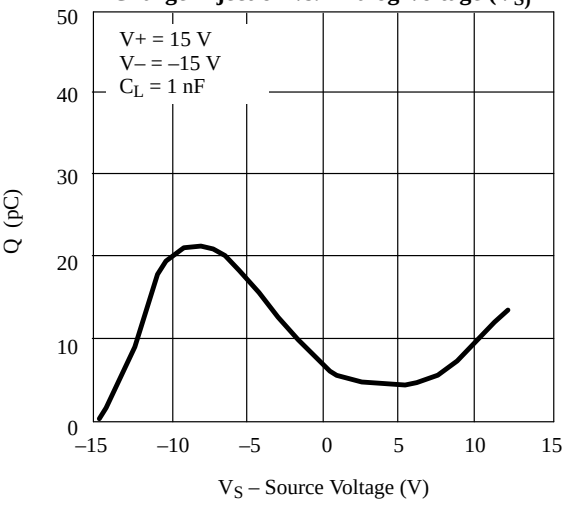
$r_{DS(on)}$ vs. V_D and Power Supply



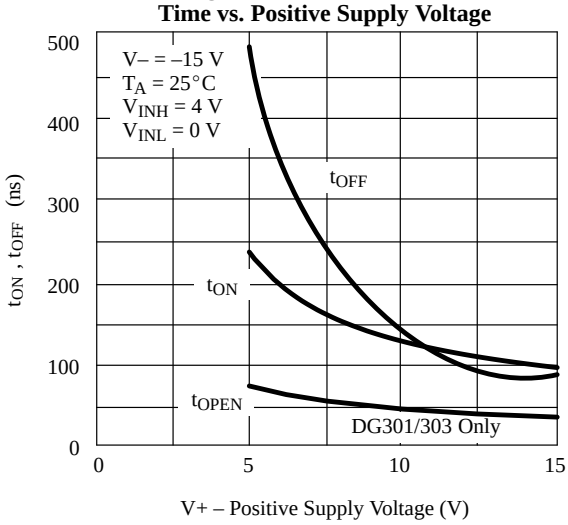
$r_{DS(on)}$ vs. V_D and Temperature



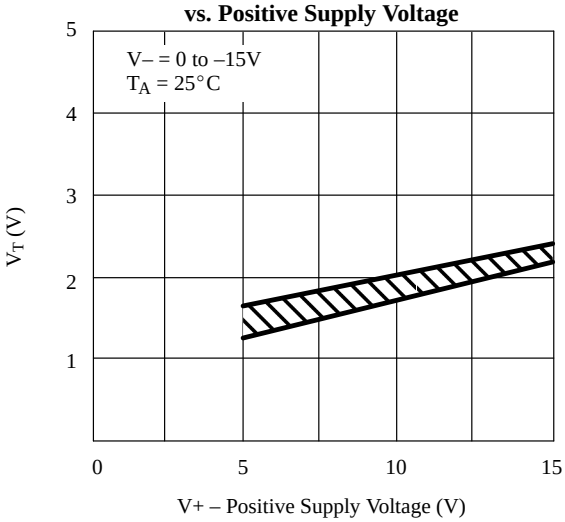
Charge Injection vs. Analog Voltage (V_S)



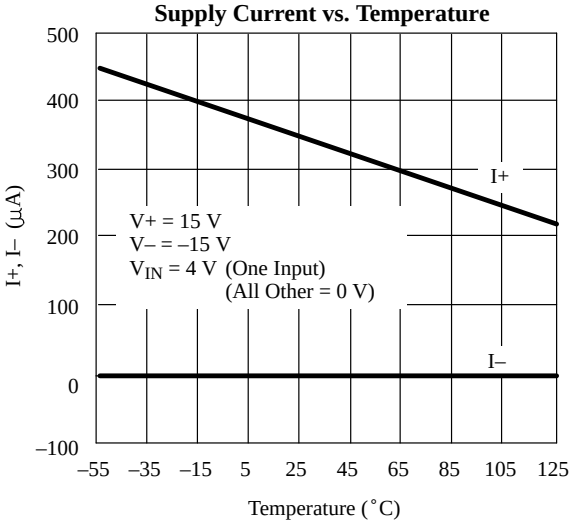
Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Input Switching Threshold vs. Positive Supply Voltage

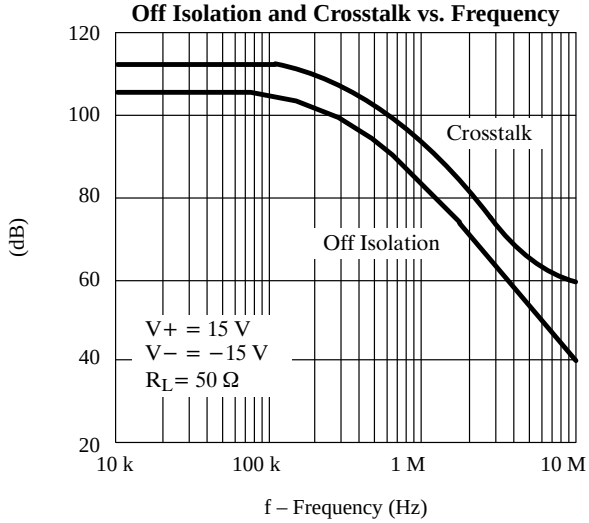


Supply Current vs. Temperature

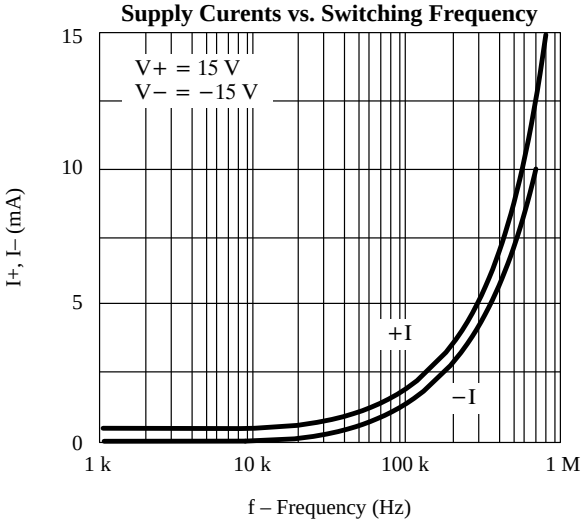


Typical Characteristic (Cont'd)

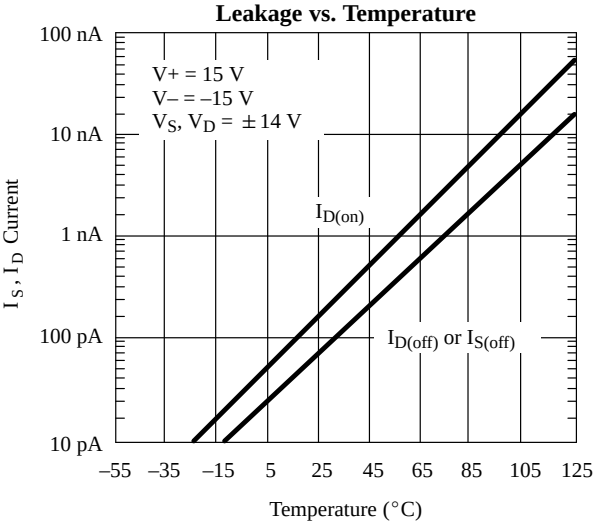
Off Isolation and Crosstalk vs. Frequency



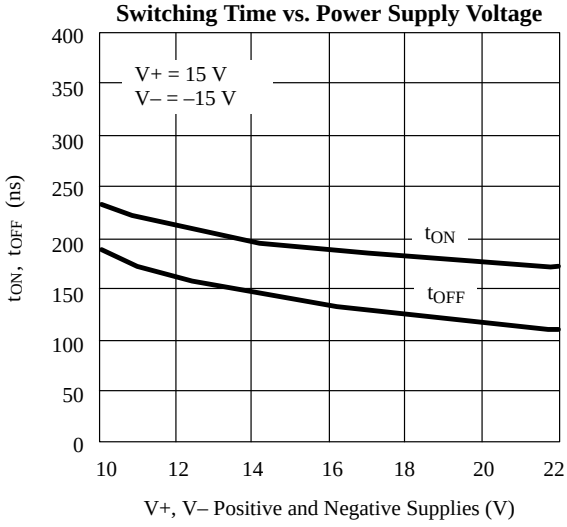
Supply Curents vs. Switching Frequency



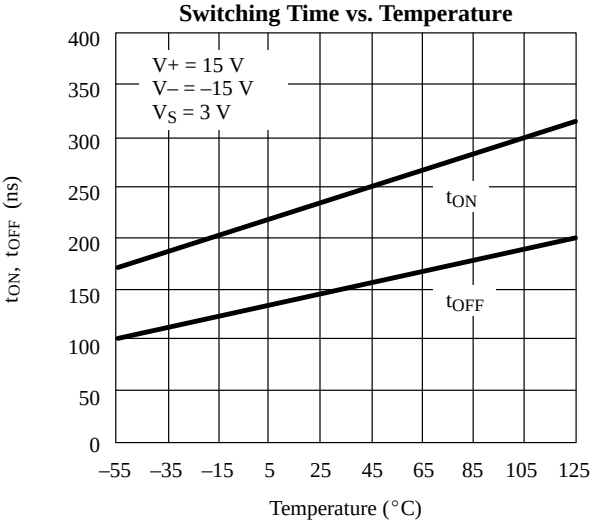
Leakage vs. Temperature



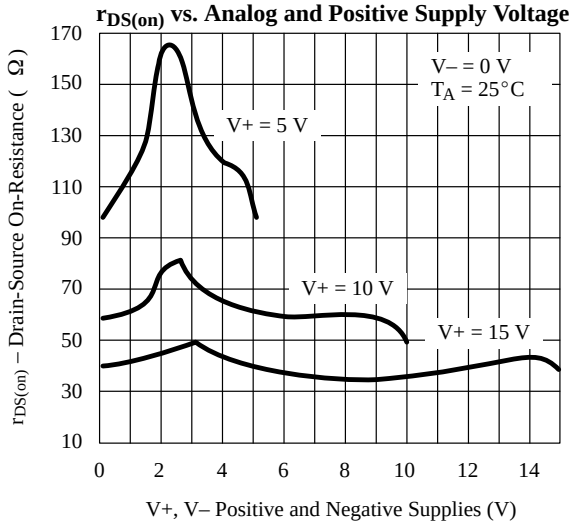
Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



$r_{DS(on)}$ vs. Analog and Positive Supply Voltage



Test Circuits

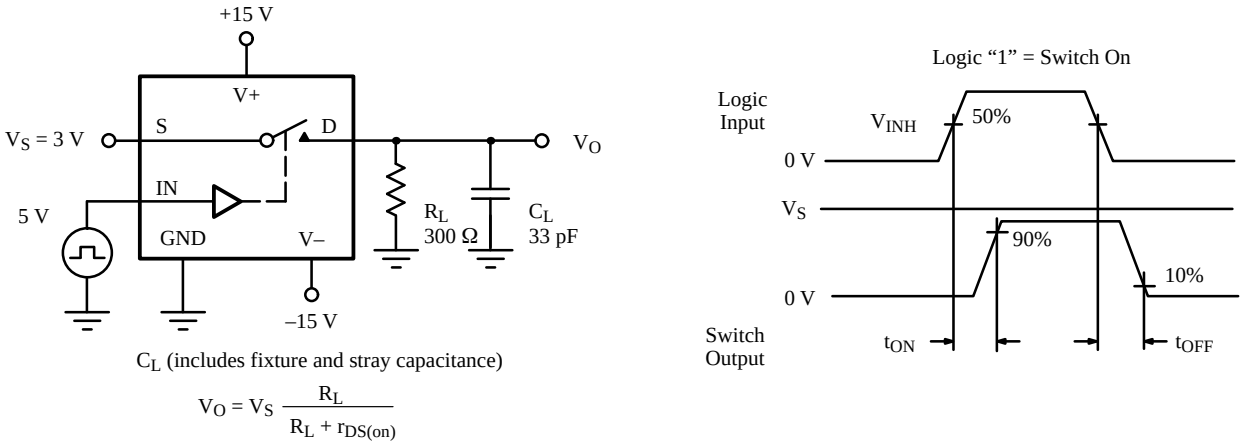


Figure 2. Switching Time

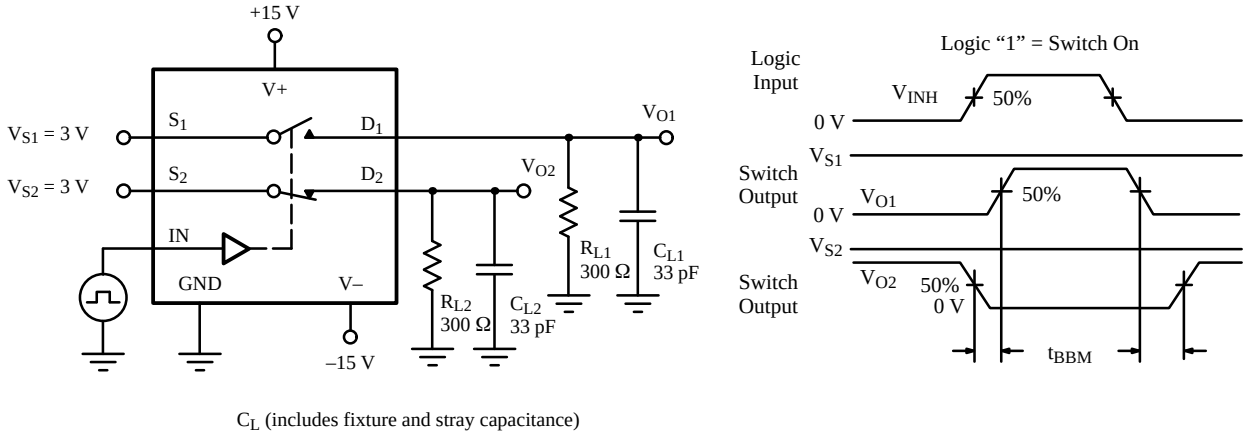


Figure 3. Break-Before-Make SPDT (DG301A, DG303A)

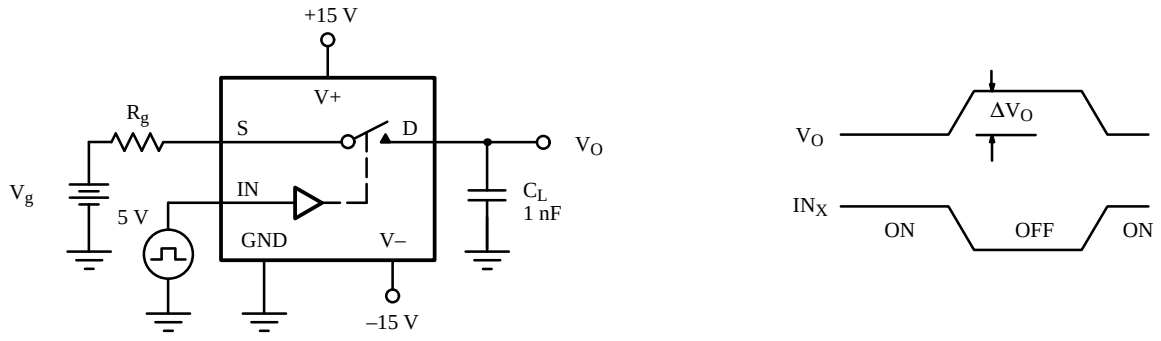


Figure 4. Charge Injection

Applications

The DG381A series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(on)}$, 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V.

In the integrator of Figure 4, R_D controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset SW_1 is closed and SW_2 is open. Opening SW_2 with SW_1 also open will hold the integrator output at its present value.

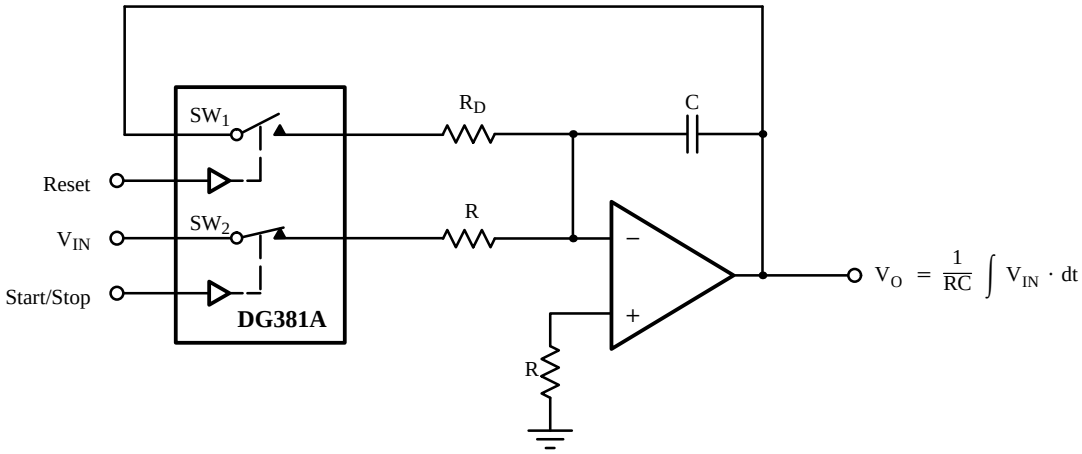


Figure 5. Integrator with Reset and Start/Stop