Dual 8-Bit CMOS D/A Converter with Voltage Output

DAC8229

FEATURES

- Two 8-Bit DACs In A Single Chip
- Adjustment-Free Internal CMOS Amplifiers
- Single or Dual Supply Operation
- TTL Compatible Over Full V_{DD} Range
- 5 Microsecond Settling Time
- Fast Interface Timing ..... t_{WR} = 50ns
- Improved Resistance to ESD
- Fits AD/PM-7528 And AD/PM-7628 Sockets
- Available In Small Outline Package
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available In Die Form

APPLICATIONS

- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Disk Drive Systems
- Multi-Channel Microprocessor-Controlled Systems

GENERAL DESCRIPTION

The DAC-8229 is a dual 8-bit, voltage output, multiplying CMOS D/A converter. Its reference input accepts a ±2.5V signal, inverts and delivers it to the output with an internal amplifier. It can also accept –10V at V_{REF} with a corresponding +10V output (the maximum positive input signal that it can accept is +2.5V).

The DAC-8229 was designed to operate with dual supplies; however, it can be operated with a single supply by connecting

Continued

ORDERING INFORMATION†

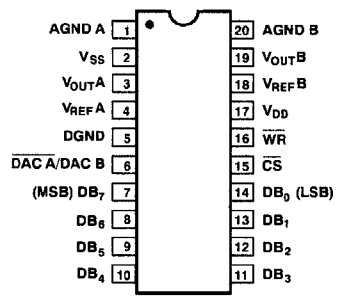
PACKAGE: 20-PIN DIP/SOL			
			EXTENDED††
MILITARY*			INDUSTRIAL
RELATIVE ACCURACY	GAIN ERROR	TEMPERATURE –55°C to +125°C	TEMPERATURE –40°C to +85°C
±1/2LSB	±2LSB	DAC8229AR	DAC8229ER
±1/2LSB	±2LSB	——	DAC8229FP
±1/2LSB	±2LSB	——	DAC8229FS

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in.

†† Cerdip and epoxy packaged devices available in the extended industrial temperature range.

PIN CONNECTIONS

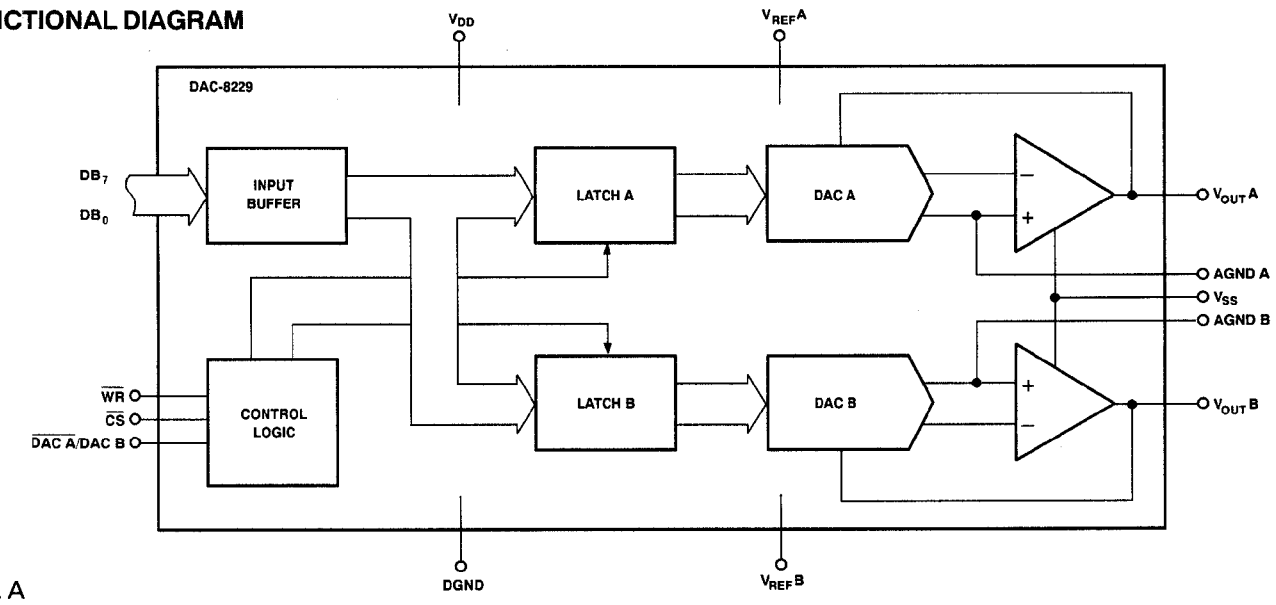


20-PIN 0.3"CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

FUNCTIONAL DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

GENERAL DESCRIPTION *Continued*

V_{SS}, AGND A, and AGND B to ground. Its operating characteristics will then be similar to that of the DAC-8228 (whose pin-out allows it to drop into the AD/PM-7528 and AD/PM-7628 sockets).

An internal regulator provides TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range. Also, each DAC input latch is addressable for easy microprocessor interfacing.

The DAC-8229 dissipates less than 109mW in the space-saving 20-pin 0.3" DIP or the 20-lead SO surface-mount package. Its compact size, low power, and economical cost per channel, make it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with PMI's highly-stable thin-film R-2R resistor ladder, offers superior matching and temperature tracking between DACs.

The DAC-8229 offers cerdip or epoxy packaged devices in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND or DGND ..... –0.3V, +17
VV_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
V_{REF} to AGND ..... –17V, +4V
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature Range
  DAC-8229AR Version ..... –55°C to +125°C
  DAC-8229ER/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. Use proper antistatic handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

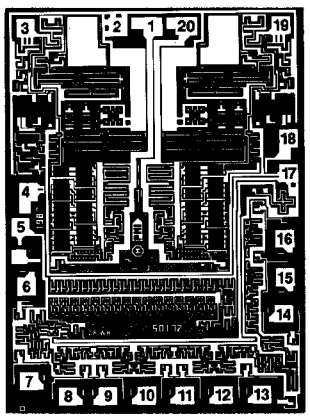
PARAMETER	SYMBOL	CONDITIONS	DAC-8229 MIN	DAC-8229 TYP	DAC-8229 MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2,10)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3, 10)	DNL		–	–	±1	LSB
Gain Error (Note 10)	G_{FSE}		–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4, 10)	TCG_{FS}		–	±0.0008	±0.002	%/°C
Zero Gain Error (Note 10)	V_{ZSE}		–	–	±10	mV
Zero Code Error Temperature Coefficient (Note 4, 10)	TCV_{ZS}		–	±5	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}		7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF

ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8229 MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Positive Supply Current (Note 6)	I_{DD}		–	–	6	mA
Negative Supply Current (Note 6)	I_{SS}		–	–	5	mA
DC Power Supply Rejection Ratio (Δ Gain/ΔV_{DD}) (Note 10)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = 25°C V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Notes 4,7)	t_S	V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	V_{REF}B to V_{OUT}A or V_{REF}A to V_{OUT}B V_{REF}B = V_{REF}A = 20V_{p-p} @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
AC Feedthrough (Notes 4, 11)	F_T	T_A = 25°C T_A = Full Temp. Range	– –	– –	–70 –65	dB
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–	–	ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and are not subject to production test.
5. Input resistance temperature coefficient = +300 ppm/°C.
6. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is +3V to –10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. V_{REF} = +2.5V, $R_{PULLDOWN}$ = 20kΩ (a pulldown resistor to V_{SS} is used for these tests).
11. V_{REF}A, V_{REF}B = 20V_{p-p} Sinewave @ f = 10kHz; V_{REF}A to V_{REF}B or V_{REF}B to V_{REF}A.

DICE CHARACTERISTICS



DIE SIZE 0.082 x 0.111 inch, 9,102 sq. mils
(2.08 x 2.82 mm, 5.87 sq. mm)

1. ANALOG GROUND (AGND A)
2. NEGATIVE POWER SUPPLY (V_{SS})
3. VOLTAGE OUTPUT (V_{OUT} A)
4. DAC A REFERENCE INPUT (V_{REF} A)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{\text{DAC A}}$/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{\text{CS}}$)
16. WRITE ($\overline{\text{WR}}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT (V_{REF} B)
19. VOLTAGE OUTPUT (V_{OUT} B)
20. ANALOG GROUND (AGND B)

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ± 10%; V_{REF} = ±2.5V; AGND = 0V; T_A = +25°C.

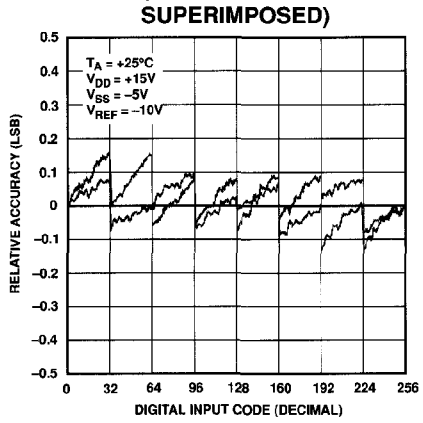
PARAMETER	SYMBOL	CONDITIONS	DAC-8229GBC LIMIT	UNITS
Relative Accuracy (Note 3)	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity (Notes 1, 3)	DNL		±1	LSB MAX
Gain Error (Note 3)	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Zero Code Error (Note 3)	V_{ZSE}		±10	mV MAX
Input Resistance	R_{IN}	Pad 4 and 18	7/15	kΩ MIN/kΩ MAX
V_{REF}A/V_{REF}B Input Resistance Match	$\frac{\Delta R_{IN}}{R_{IN}}$		1	% MAX
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
DC Supply Rejection (ΔGain/ΔV_{DD}) (Note 3)	PSRR	V_{DD} = ±5%	0.01	%/% MAX
Positive Supply Current (Note 2)	I_{DD}		6	mA MAX
Negative Supply Current (Note 2)	I_{SS}		5	mA MAX

NOTES:
1. All dice guaranteed monotonic over the full operating temperature range.
2. $V_{IN} = V_{INL}$ or V_{INH}; output unloaded.
3. V_{REF} = +2.5V, $R_{PULLDOWN}$ = 20kΩ (a pulldown resistor to V_{SS} is used for these tests).

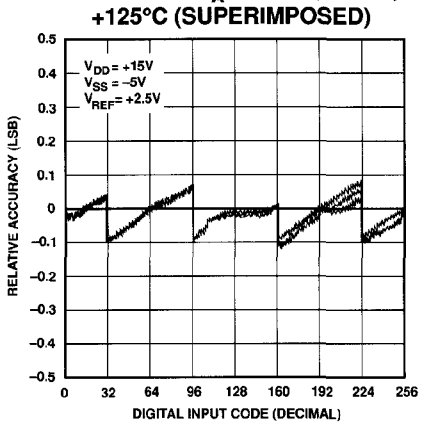
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERTISTICS

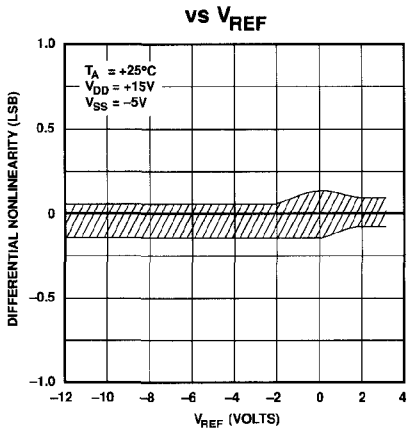
DAC A-TO-DAC B MATCHING (DACs A & B ARE SUPERIMPOSED)



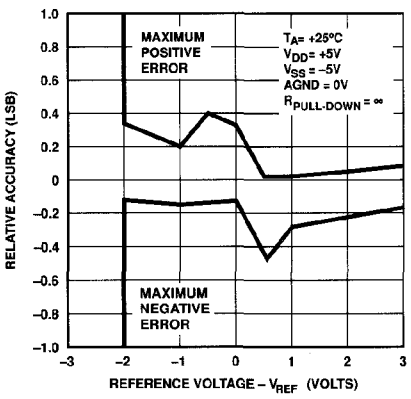
RELATIVE ACCURACY (DAC A) vs CODE AT T_A = –55°C, +25°C, +125°C (SUPERIMPOSED)



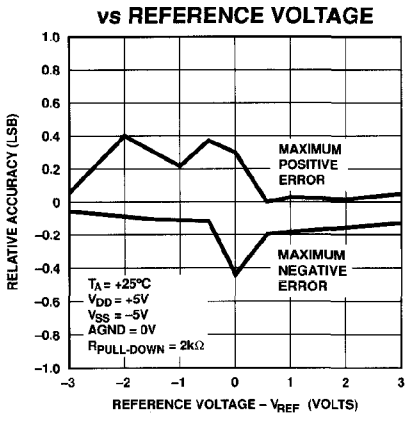
DIFFERENTIAL NONLINEARITY vs V_{REF}



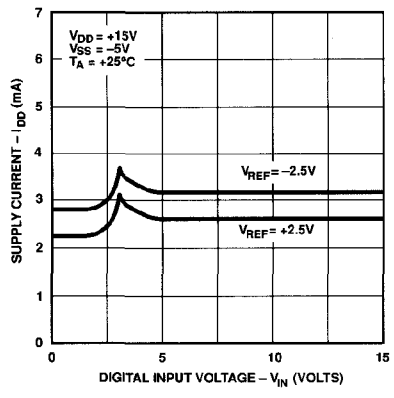
RELATIVE ACCURACY vs REFERENCE VOLTAGE



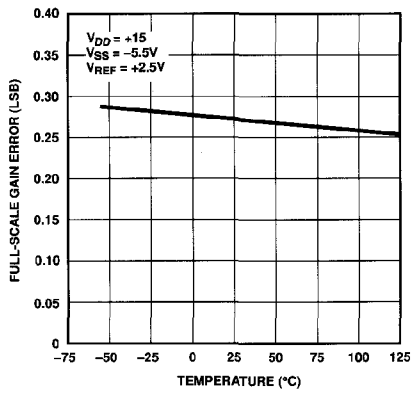
RELATIVE ACCURACY vs REFERENCE VOLTAGE



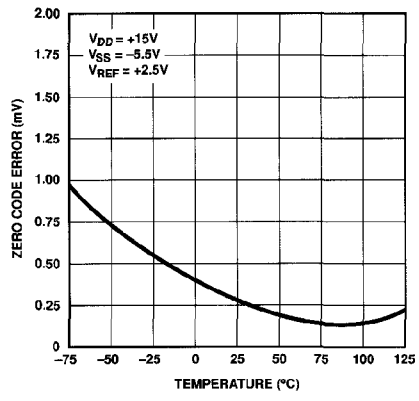
SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



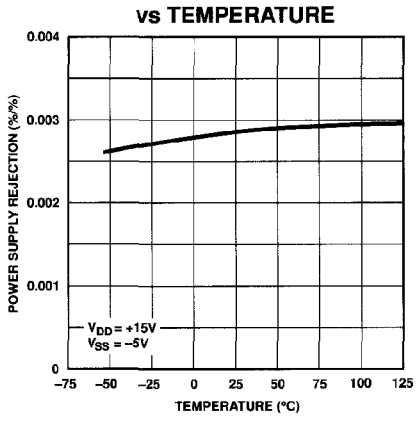
FULL-SCALE GAIN ERROR vs TEMPERATURE



ZERO CODE ERROR vs TEMPERATURE

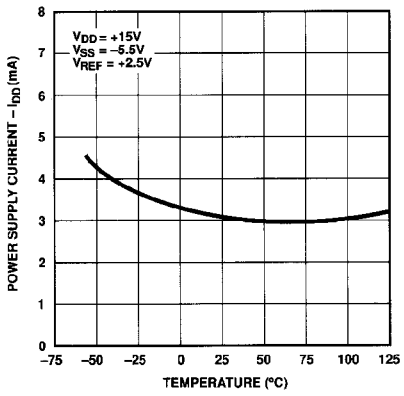


POWER SUPPLY REJECTION vs TEMPERATURE

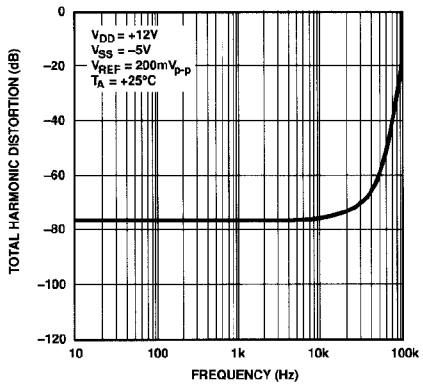


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

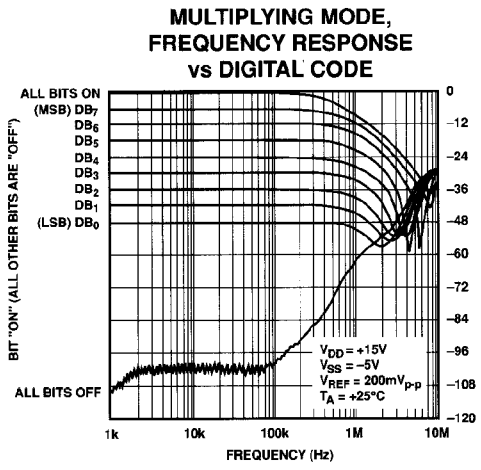
POWER SUPPLY CURRENT vs TEMPERATURE



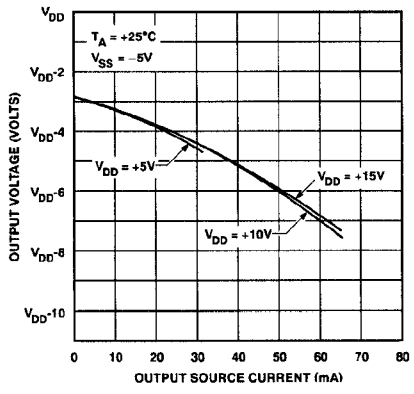
TOTAL HARMONIC DISTORTION vs FREQUENCY



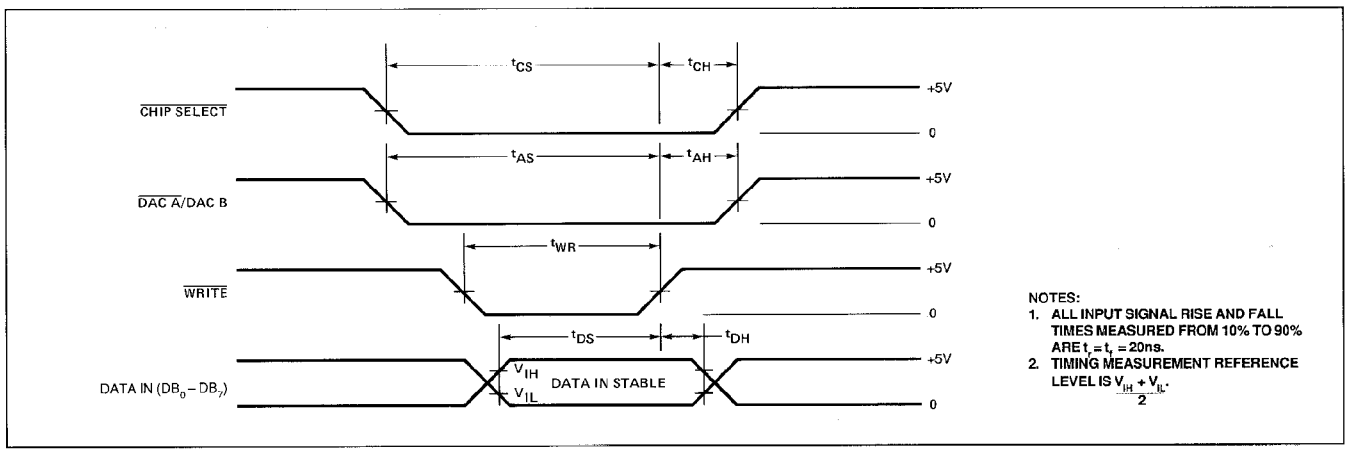
MULTIPLYING MODE, FREQUENCY RESPONSE vs DIGITAL CODE



OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

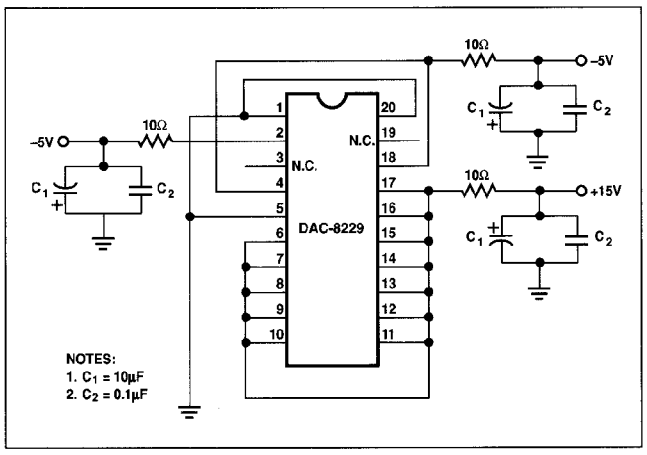


WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

BURN-IN CIRCUIT



PARAMETER DEFINITIONS

RESOLUTION (N)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be non-monotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal. Zero code error is not included in this measurement.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

The DAC-8229 consists of two voltage output amplifiers, two high accuracy R-2R resistor ladder networks, an 8-bit input buffer, two 8-bit DAC registers, and interface control logic circuitry.

Also included are 16 single-pole, double-throw NMOS transistor switches. These switches, which are controlled by the digital input code, were designed to switch each R-2R resistor leg between the amplifier inverting input and AGND.

A simplified circuit of the R-2R resistor ladder and output amplifier is illustrated in Figure 1. The signal is inverted from the V_{REF} input to the output. Note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section under Single Supply Operation.

REFERENCE INPUT

The DAC-8229's internal output amplifier has a maximum voltage swing in the negative direction of –2.5V (limited by V_{SS}). In

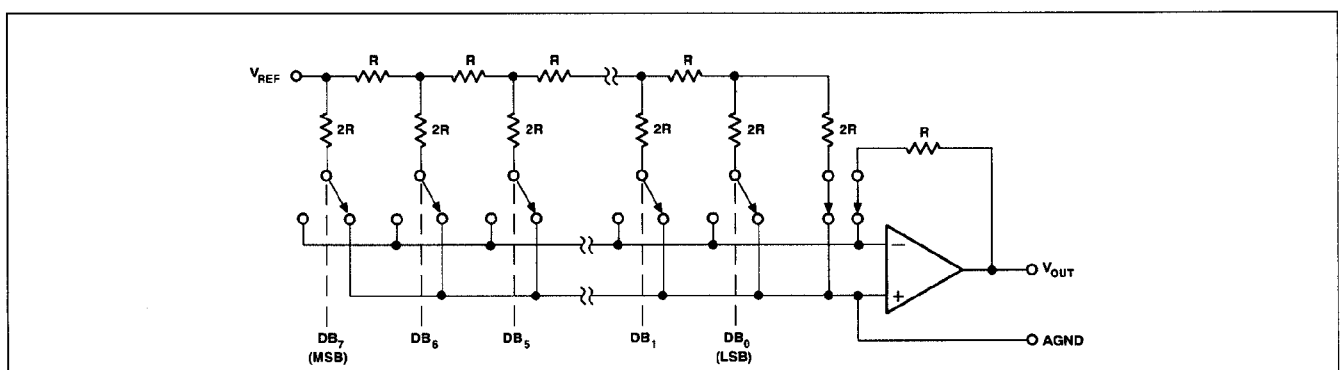


FIGURE 1: *Simplified single DAC configuration (switches shown for all digital inputs at logic "0").*

the positive direction, the voltage swing is limited to 4V less than V_{DD}. These limitations set the maximum levels that the reference input (V_{REF}) can accept. Note that the positive V_{REF} limit is set by the negative supply voltage, V_{SS}, and the negative V_{REF} limit is set by (V_{DD} –4V).

For example, maximum V_{REF} input in the positive direction is +2.5V and –11V with V_{DD} = +15V. The equation for the absolute value in the negative direction takes the form of:

$|-V_{REF}\ max| = V_{DD} - 4V$.

The equation shows that –8V is the maximum voltage that can be applied in the negative direction at V_{REF} with V_{DD} = +12V.

The DAC-8229's output voltage equation is:

$-V_{OUT} = V_{REF} \times D/256$

where D is the digital input code number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

The DAC-8229's amplifier output stage is an NPN bipolar transistor. This transistor provides a low-impedance high-output current capability. The emitter of the NPN transistor is loaded with a 450μA NMOS current source that is connected to V_{SS}; (see Figure 2). This current is sunk into the negative supply allowing the amplifier's output to go to –2.5V.

Figure 3 depicts a typical output current-sink versus voltage graph for the DAC-8229. It shows the output amplifier's current sink capability with V_{SS} = –5V and 0V. With V_{SS} = –5V, the amplifier still operates in the saturation region as the output goes to zero; however, with V_{SS} = 0V, the amplifier comes out of its saturation region and starts appearing resistive as the output approaches zero.

The DAC-8229's internal amplifiers can each drive +10 volts across a 2kΩ load, sourcing 5mA. In fact, they can drive up to 65mA, but with a reduced output amplitude. See the Output Source Current graph under the typical electrical characteristic curves. The user must use caution that the package power dissipation is not exeeded when driving low impedances and high currents. However, as seen in Figure 3, the amplifier has limited current sink capability. Signal waveforms can be improved considerably by adding a pull-down resistor at each amplifier output. For example, pulling a 2kΩ load down to –2.5V requires a 1kΩ pull-down resister (connected to –5V) The accompanying scope photographs show the effects of operating

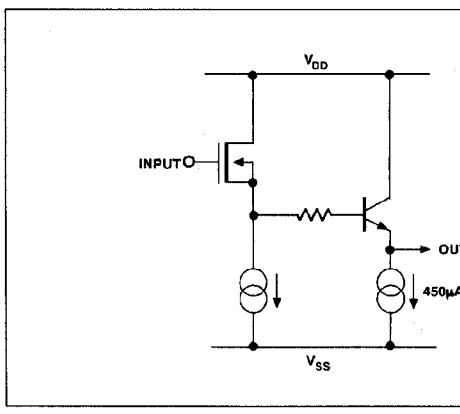


FIGURE 2: *Amplifier Output Stage*

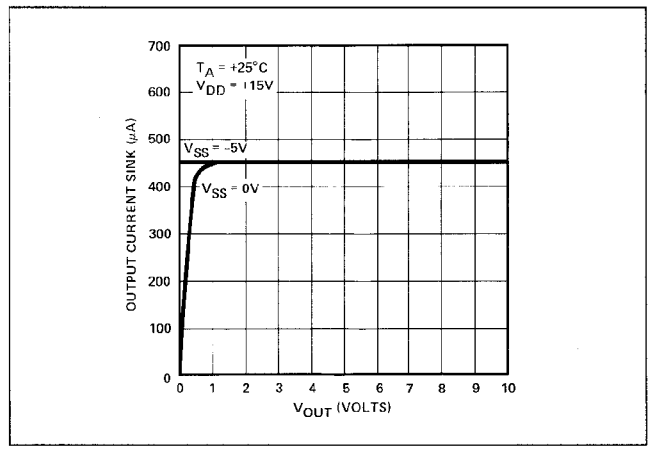


FIGURE 3: *DAC Output Current Sink*

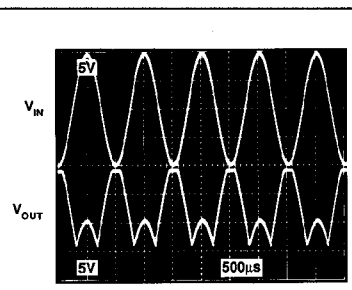


PHOTO A: *Multiplying Mode (f = 1kHZ, No Pull-down)*

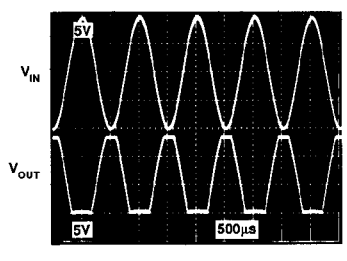


PHOTO B: *Multiplying Mode (f = 1kHZ, with 1kΩ Pull-down)*

the DAC-8229 with and without a 1kΩ pull-down resistor. Photo A is that without the pull-down resistor, and B with the 1kΩ pull-down resistor. Note signal improvement using the pull-down resistor. Figure 4 shows this circuit configuration and the table lists other resistor values.

PULL-DOWN RESISTOR vs LOAD RESISTOR VALUES

(V_{DD} = +15V; V_{SS} = –5V)

LOAD	PULL-DOWN
2kΩ	1kΩ
5kΩ	4kΩ
10kΩ	10kΩ
15kΩ	12kΩ
20kΩ	16kΩ
25kΩ	400kΩ
>30kΩ	None Required

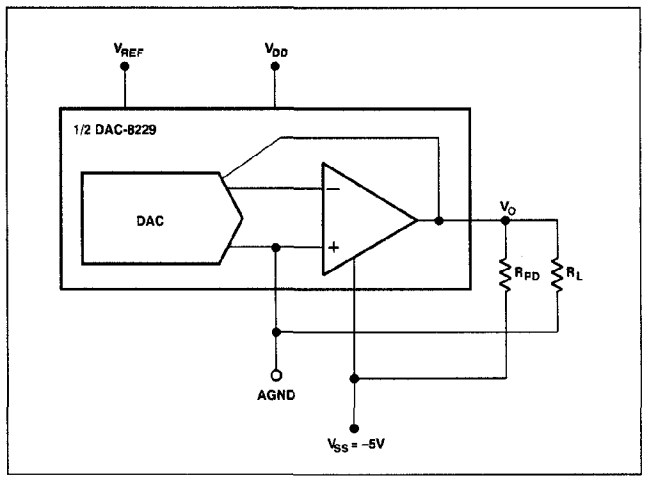


FIGURE 4: *R_{LOAD} and $R_{PULL-DOWN}$ Circuit Configuration with the DAC-8229*

The DAC-8229 can also operate with ±5V supplies, V_{DD} = +5V and V_{SS} = –5V. See the Relative Accuracy vs. Reference Voltage graphs under the typical characteristics curves. The graphs are shown with and without a 2kΩ pull-down resistor. Note how the DAC stays within the specified limit except when V_{REF} = –2V and without the pull-down resistor.

The amplifier's internal gain stages were designed to maintain sufficient gain over its common mode range. This results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during manufacturing. This eliminates user offset trimming in many applications.

DIGITAL SECTION

Figure 5 shows one digital input structure of the DAC-8229. A built-in 5V regulator and level shifter converts TTL digital input signals into CMOS levels to drive the internal circuitry. This provides full TTL compatibility over a V_{DD} range of 5 to 15V.

As shown in Figure 5, each digital input is protected from electrostatic-discharge with two internal diodes connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

INTERFACE CONTROL INFORMATION

DAC SELECTION

DAC A and DAC B both share a common 8-bit input port. The control input, $\overline{\text{DAC A}}$/DAC B, selects which DAC can accept data from the input port. A logic low selects DAC A and a logic high selects DAC B.

DAC OPERATION

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operation of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to the codes on the digital input pins.

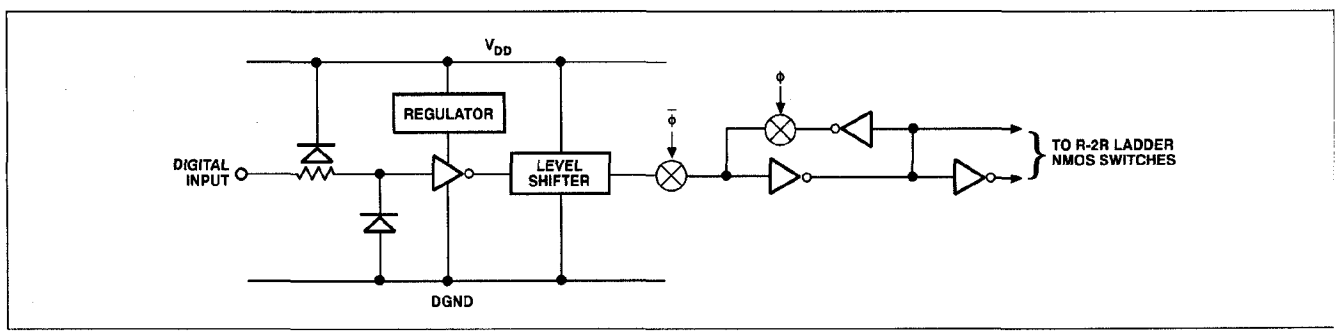


FIGURE 5: *Simplified Digital Input Structure*

HOLD MODE

The selected DAC register latches the data present on the digital input pins just prior to $\overline{CS}$ and $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

$\overline{DAC A}$/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 6 shows the DAC-8229 configured to operate in the unipolar mode, and Table 1 shows the corresponding code table. The equation for 1 LSB and the analog output voltage is:

$1\ LSB = V_{REF} \times 2^{-8}$, or $V_{REF} \times 1/256$

and

$-V_{OUT} = V_{REF} \times D/256$

where D is the digital input number between 0 and 255.

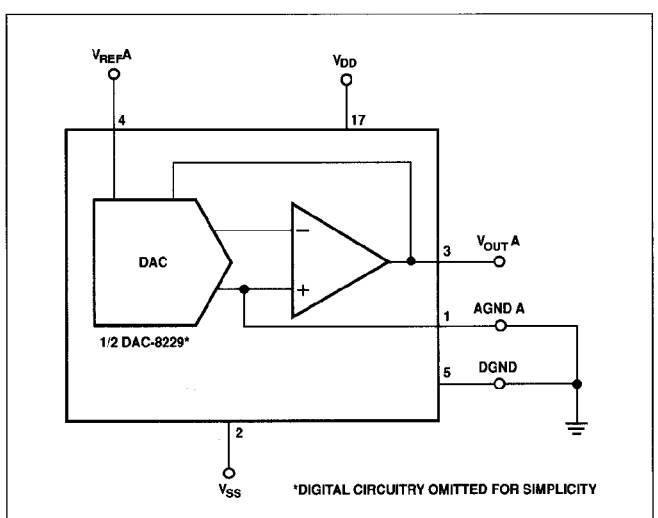


FIGURE 6: *Unipolar Operation*

TABLE 1: Unipolar Code Table (Refer to Figure 6)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = \frac{-V_{REF}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

BIPOLAR OPERATION

Figure 7 shows the DAC-8229 configured in the bipolar mode of operation. This configuration requires an external amplifier and four resistors. To keep gain and offset errors at a minimum, the external resistors should be matched to ±0.1% and track over the operating temperature range of interest.

Table 2 shows the corresponding code table.

TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 7)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

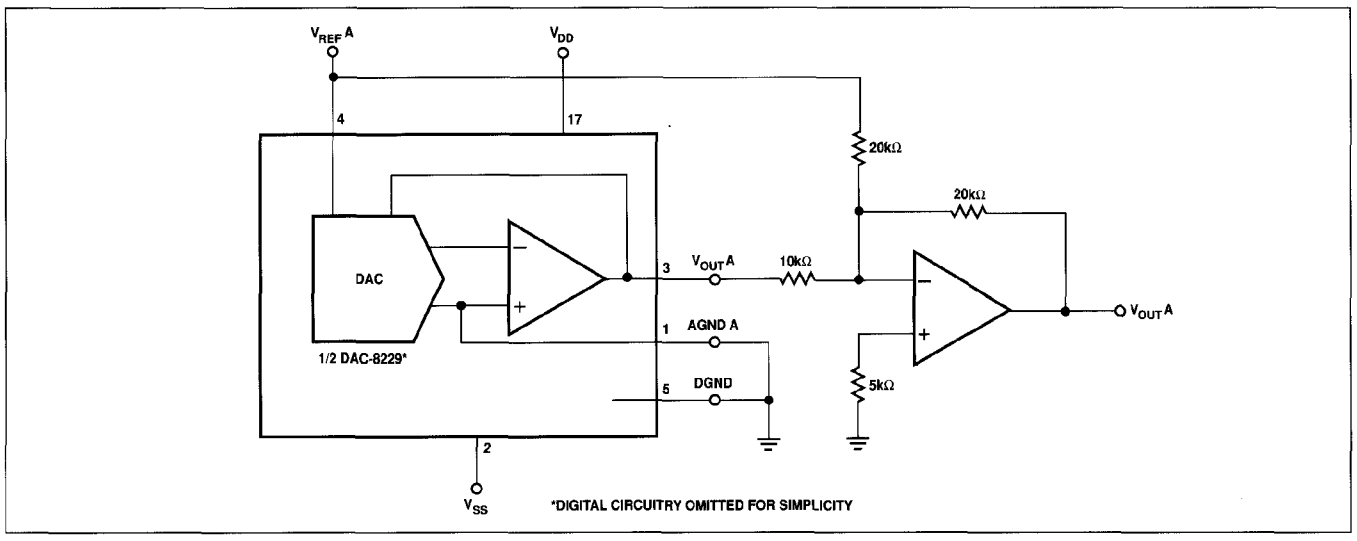


FIGURE 7: *Bipolar Operation*

SINGLE SUPPLY OPERATION

Some applications require the AGND pin to be biased above ground for single supply operation. A popular scheme is shown in Figure 8. It consists of connecting a +2.5 volt reference (such as PMI's REF-03) to the AGND pin, V_{REF} and V_{SS} pins grounded, and +12V to V_{DD}. Both DAC A and DAC B AGND pins are separate and can be independently biased.

The resulting transfer equation is:

$V_{OUT}(D) = 2.5(1 + D/256)$

where D is the whole number binary digital input.

V_{OUT} for the circuit of Figure 8 results in:

$V_{OUT}(255) = 2.5(1 + 255/256) = +5V$

$V_{OUT}(0) = +2.5V.$

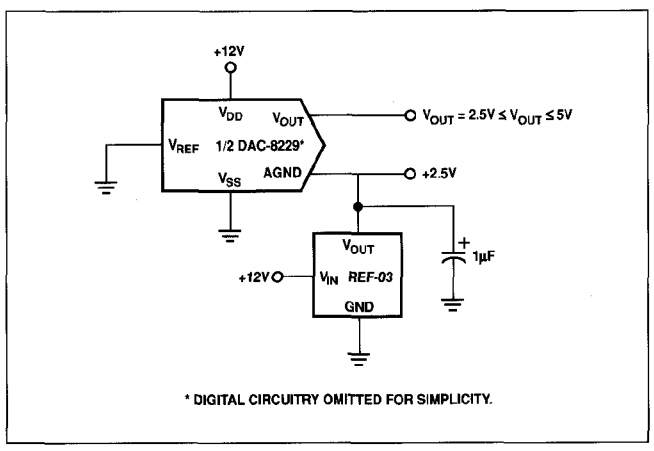


FIGURE 8: *Single Supply Configuration*

Figure 9 shows a typical plot of the DAC-8229 in the single-supply configuration of Figure 8. It is plotted for various values of AGND voltage biased above ground. It shows relative accuracy degrading as AGND is taken above +4V; however, it contributes only 1 LSB error at +5V.

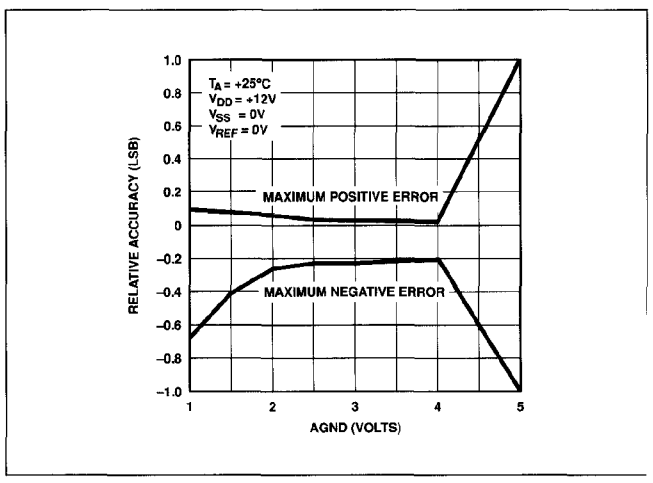


FIGURE 9: *Relative Accuracy vs. AGND*

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8229's versatile input structure allows direct interface to 8- or 16-bit microprocessors. Its simplicity reduces the number of required glue logic components. Figures 10 and 11 show the DAC-8229 interface configurations with the 6800 and 8085 microprocessors.

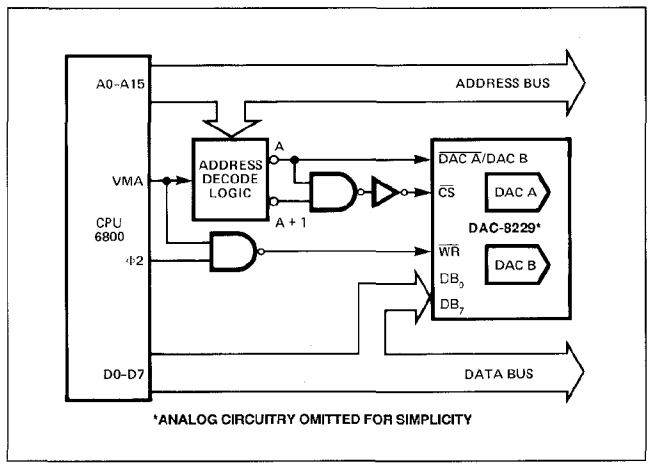


FIGURE 10: *DAC-8229 Interface to 6800 Microprocessor*

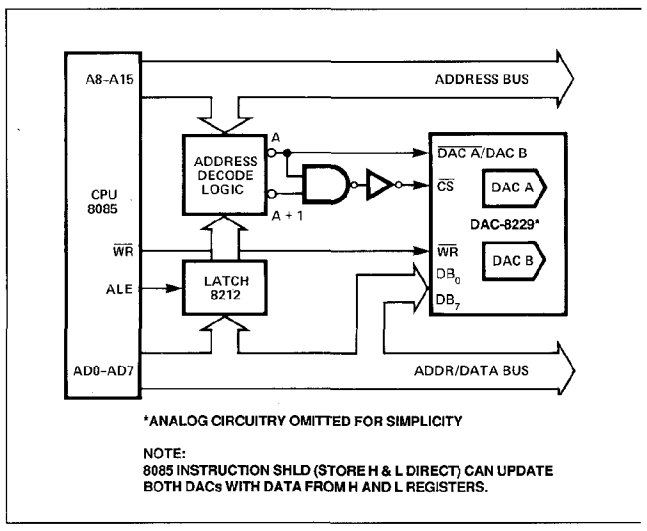


FIGURE 11: *DAC-8229 Interface to 8085 Microprocessor*