



12-BIT, QUAD, ULTRALOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 2.7-V to 5.5-V Single Supply
- 12-Bit Linearity and Monotonicity
- Rail-to-Rail Voltage Output
- Settling Time: 5 μ s (Max)
- Ultralow Glitch Energy: 0.1 nVs
- Ultralow Crosstalk: -100 dB
- Low Power: 880 μ A (Max)
- Per-Channel Power Down: 2 μ A (Max)
- Power-On Reset to Zero Scale
- SPI-Compatible Serial Interface: Up to 50 MHz
- Simultaneous or Sequential Update
- Specified Temperature Range: -40°C to 105°C
- Small 10-Lead MSOP Package

APPLICATIONS

- Portable Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Industrial Process Control

DESCRIPTION

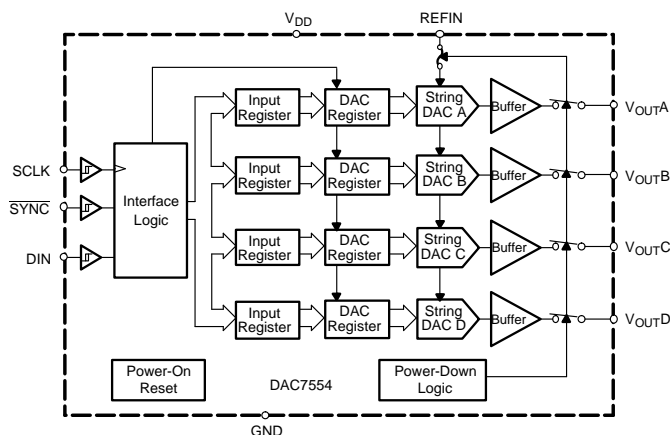
The DAC7554 is a quad-channel, voltage-output DAC with exceptional linearity and monotonicity. Its proprietary architecture minimizes undesired transients such as code to code glitch and channel to channel crosstalk. The low-power DAC7554 operates from a single 2.7-V to 5.5-V supply. The DAC7554 output amplifiers can drive a 2-k Ω , 200-pF load rail-to-rail with 5- μ s settling time; the output range is set using an external voltage reference.

The 3-wire serial interface operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards. The outputs of all DACs may be updated simultaneously or sequentially. The parts incorporate a power-on-reset circuit to ensure that the DAC outputs power up to zero volts and remain there until a valid write cycle to the device takes place. The parts contain a power-down feature that reduces the current consumption of the device to under 1 μ A.

The small size and low-power operation makes the DAC7554 ideally suited for battery-operated portable applications. The power consumption is typically 3.5 mW at 5 V, 1.65 mW at 3 V, and reduces to 1 μ W in power-down mode.

The DAC7554 is available in a 10-lead MSOP package and is specified over -40°C to 105°C .

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC7554	10 MSOP	DGS	–40°C TO 105°C	D754	DAC7554IDGS	80-piece Tube
					DAC7554IDGSR	2500-piece Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	UNIT
V_{DD} to GND	–0.3 V to 6 V
Digital input voltage to GND	–0.3 V to $V_{DD} + 0.3$ V
V_{out} to GND	–0.3 V to $V_{DD} + 0.3$ V
Operating temperature range	–40°C to 105°C
Storage temperature range	–65°C to 150°C
Junction temperature (T_J Max)	150°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 2.7\text{ V}$ to 5.5 V , $REFIN = V_{DD}$, $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications -40°C to 105°C , unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE ⁽¹⁾					
Resolution		12			Bits
Relative accuracy		±0.35 ±1			LSB
Differential nonlinearity	Specified monotonic by design	±0.08 ± 0.5			LSB
Offset error		±12			mV
Zero-scale error	All zeroes loaded to DAC register	±12			mV
Gain error		±0.15			%FSR
Full-scale error		±0.5			%FSR
Zero-scale error drift		7			µV/°C
Gain temperature coefficient		3			ppm of FSR/°C
PSRR	V _{DD} = 5 V	0.75			mV/V
OUTPUT CHARACTERISTICS ⁽²⁾					
Output voltage range		0	REFIN		V
Output voltage settling time	R _L = 2 kΩ; 0 pF < C _L < 200 pF	5			µs
Slew rate		1			V/µs
Capacitive load stability	R _L = ∞	470			pF
	R _L = 2 kΩ	1000			
Digital-to-analog glitch impulse	1 LSB change around major carry	0.1			nV-s
Channel-to-channel crosstalk	1-kHz full-scale sine wave, outputs unloaded	−100			dB
Digital feedthrough		0.1			nV-s
Output noise density (10-kHz offset frequency)		70			nV/rtHz
Total harmonic distortion	F _{OUT} = 1 kHz, F _S = 1 MSPS, BW = 20 kHz	−85			dB
DC output impedance		1			Ω
Short-circuit current	V _{DD} = 5 V	50			mA
	V _{DD} = 3 V	20			
Power-up time	Coming out of power-down mode, V _{DD} = 5 V	15			µs
	Coming out of power-down mode, V _{DD} = 3 V	15			
LOGIC INPUTS ⁽²⁾					
Input current		±1			µA
V _{IN_L} , Input low voltage	V _{DD} = 5 V	0.3 V _{DD}			V
V _{IN_H} , Input high voltage	V _{DD} = 3 V	0.7 V _{DD}			V
Pin capacitance		3			pF
POWER REQUIREMENTS					
V _{DD}		2.7	5.5		V
I _{DD} (normal operation) V _{DD} = 3.6 V to 5.5 V V _{DD} = 2.7 V to 3.6 V	DAC active and excluding load current V _{IH} = V _{DD} and V _{IL} = GND				µA
		700	880		
		550	830		
I _{DD} (all power-down modes) V _{DD} = 3.6 V to 5.5 V V _{DD} = 2.7 V to 3.6 V	V _{IH} = V _{DD} and V _{IL} = GND				µA
		0.2	2		
		0.05	2		
Reference input impedance		25			kΩ
POWER EFFICIENCY					
I _{OUT} /I _{DD}	I _{LOAD} = 2 mA, V _{DD} = 5 V	93%			

(1) Linearity tested using a reduced code range of 48 to 4048; output unloaded.

(2) Specified by design and characterization, not production tested.

TIMING CHARACTERISTICS⁽¹⁾⁽²⁾

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND; all specifications $-40^\circ\text{C to }105^\circ\text{C}$, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_1^{(3)}$	SCLK cycle time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	20			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	20			
t_2	SCLK HIGH time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	10			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	10			
t_3	SCLK LOW time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	10			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	10			
t_4	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	4			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	4			
t_5	Data setup time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	5			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	5			
t_6	Data hold time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	4.5			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	4.5			
t_7	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	0			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	0			
t_8	Minimum $\overline{\text{SYNC}}$ HIGH time	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	20			ns
		$V_{DD} = 3.6\text{ V to }5.5\text{ V}$	20			

(1) All input signals are specified with $t_R = t_F = 1\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

(2) See Serial Write Operation timing diagram Figure 1.

(3) Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7\text{ V to }5.5\text{ V}$.

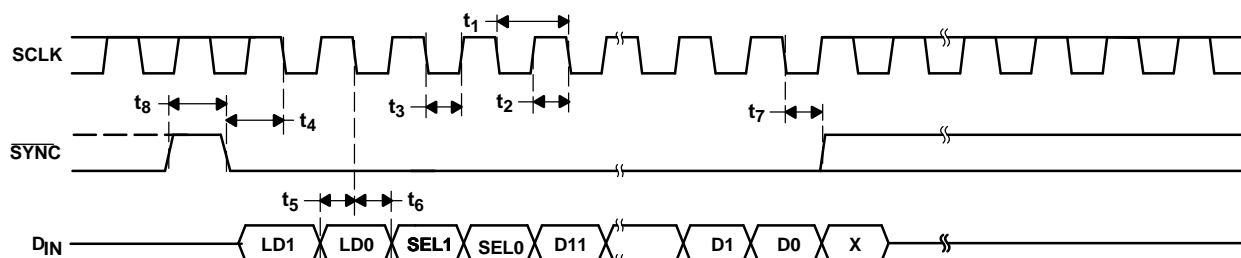
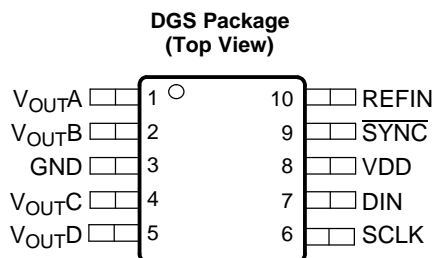


Figure 1. Serial Write Operation

PIN DESCRIPTION



Terminal Functions

TERMINAL		DESCRIPTION
NO.	NAME	
1	VOUTA	Analog output voltage from DAC A
2	VOUTB	Analog output voltage from DAC B
3	GND	Ground
4	VOUTC	Analog output voltage from DAC C
5	VOUTD	Analog output voltage from DAC D
6	SCLK	Serial clock input
7	DIN	Serial data input
8	VDD	Analog voltage supply input
9	SYNC	Frame synchronization input. The falling edge of the FS pulse indicates the start of a serial data frame shifted out to the DAC7554
10	REFIN	Analog input. External reference

TYPICAL CHARACTERISTICS

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

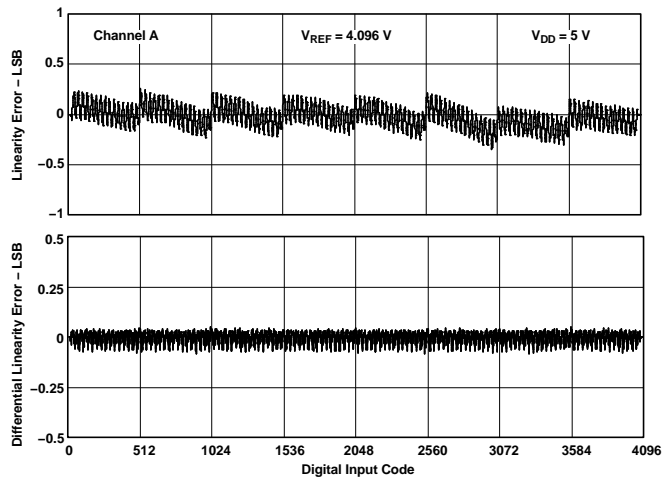


Figure 2.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

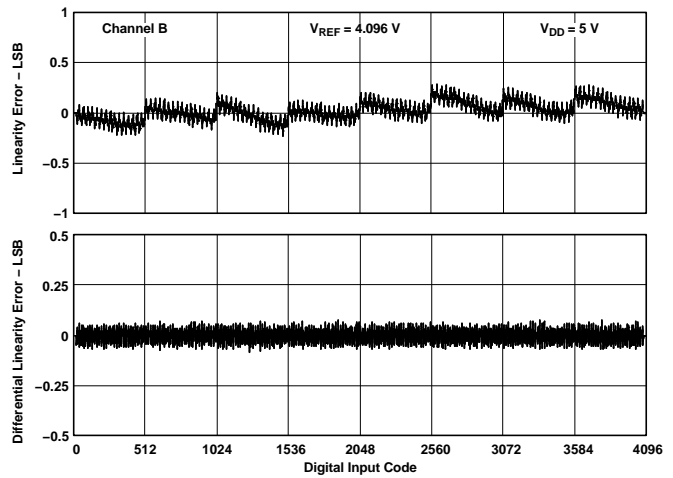


Figure 3.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

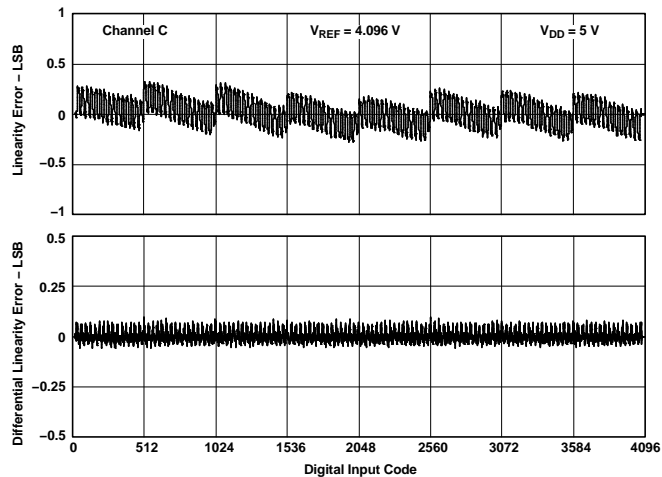


Figure 4.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

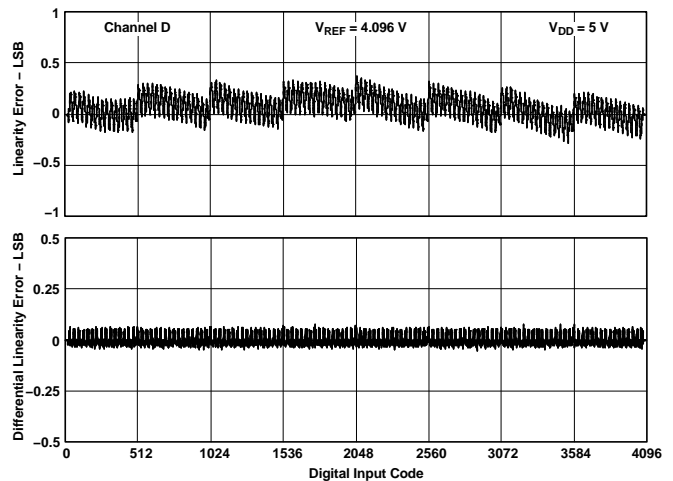


Figure 5.

TYPICAL CHARACTERISTICS (continued)

LINEARITY ERROR AND
 DIFFERENTIAL LINEARITY ERROR
 VS
 DIGITAL INPUT CODE

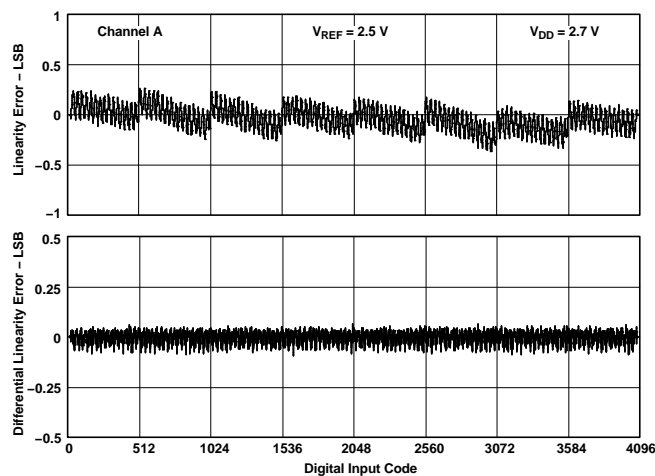


Figure 6.

LINEARITY ERROR AND
 DIFFERENTIAL LINEARITY ERROR
 VS
 DIGITAL INPUT CODE

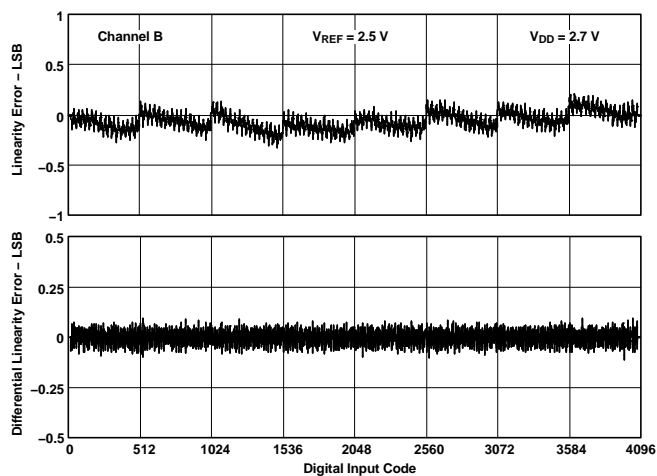


Figure 7.

LINEARITY ERROR AND
 DIFFERENTIAL LINEARITY ERROR
 VS
 DIGITAL INPUT CODE

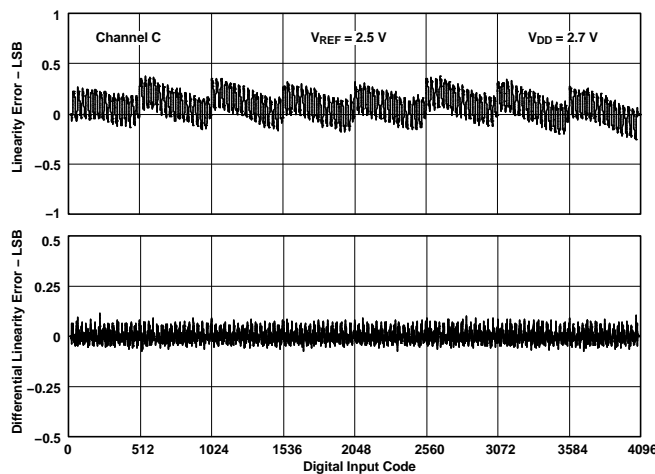


Figure 8.

LINEARITY ERROR AND
 DIFFERENTIAL LINEARITY ERROR
 VS
 DIGITAL INPUT CODE

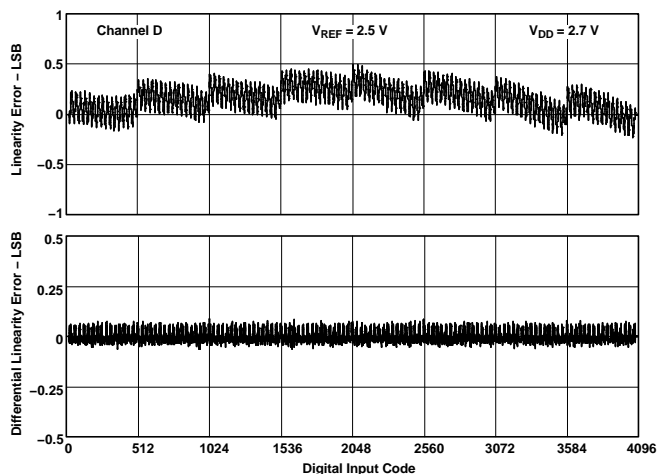


Figure 9.

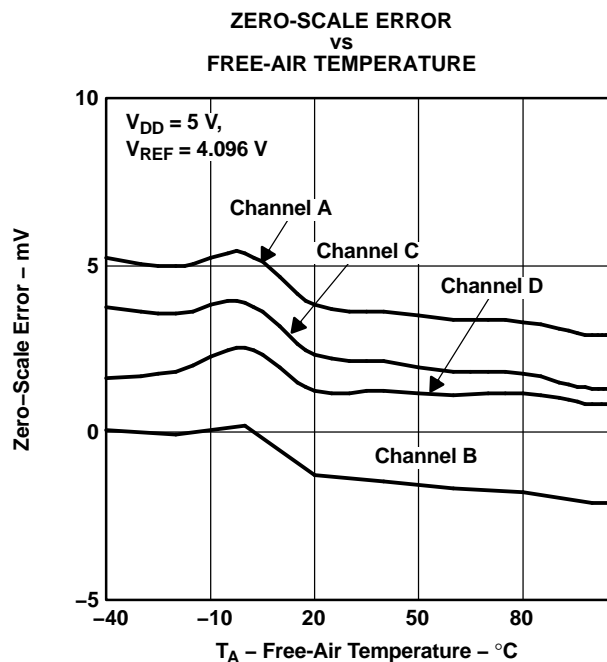
TYPICAL CHARACTERISTICS (continued)

Figure 10.

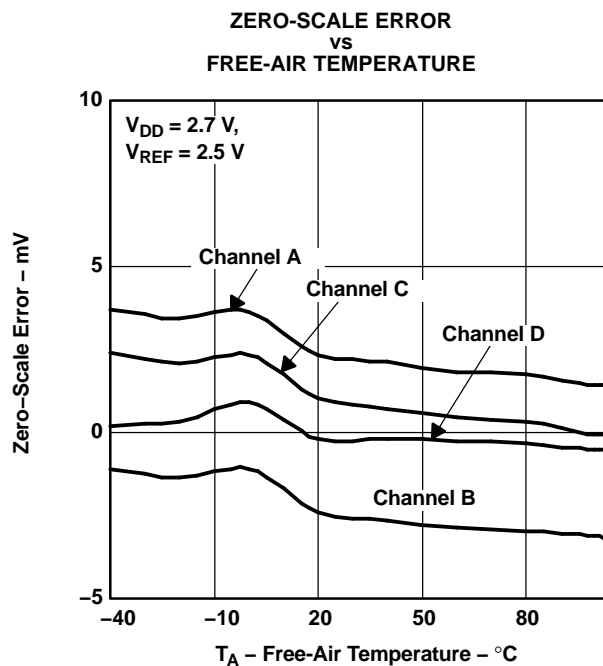


Figure 11.

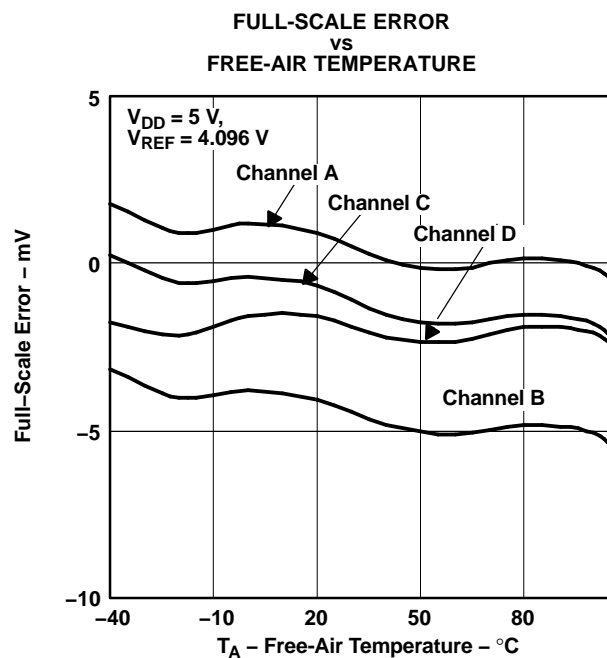


Figure 12.

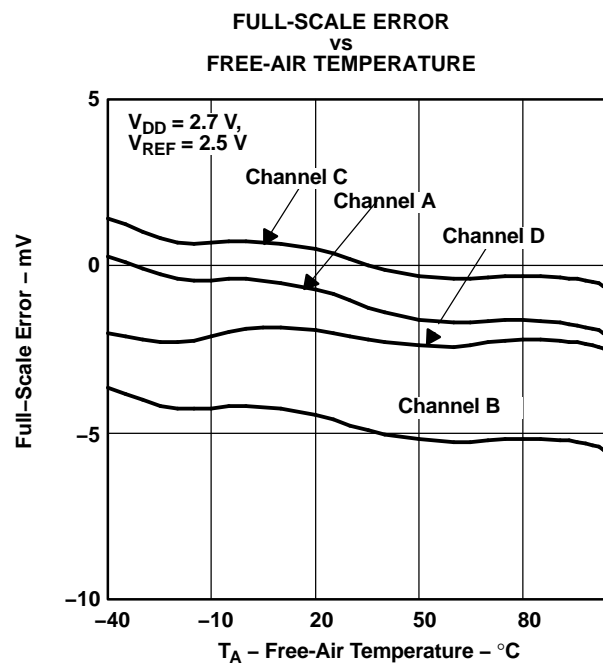


Figure 13.

TYPICAL CHARACTERISTICS (continued)

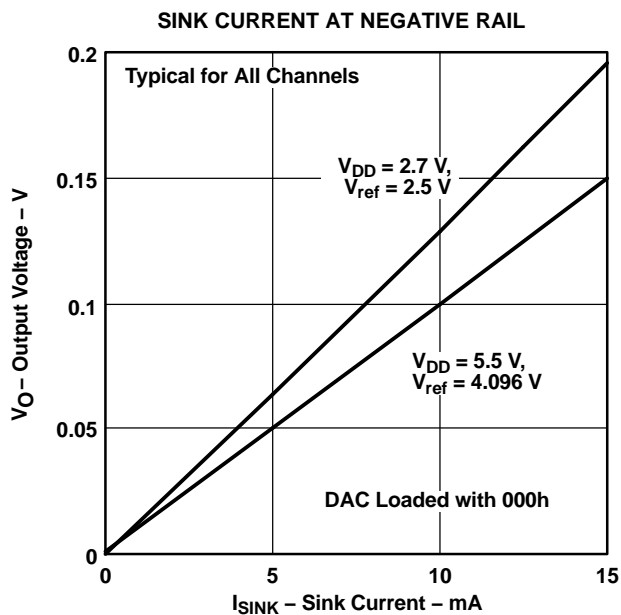


Figure 14.

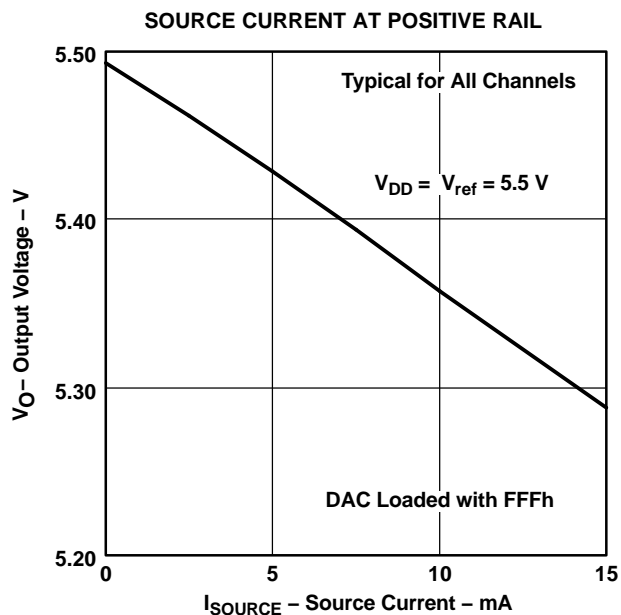


Figure 15.

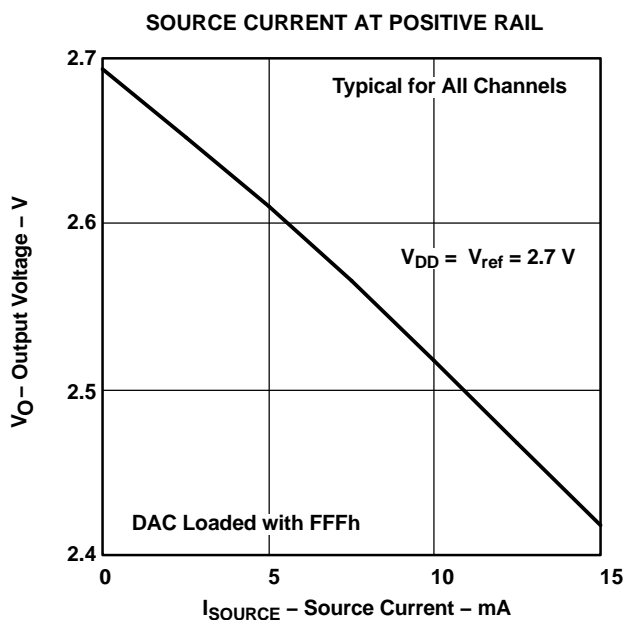


Figure 16.

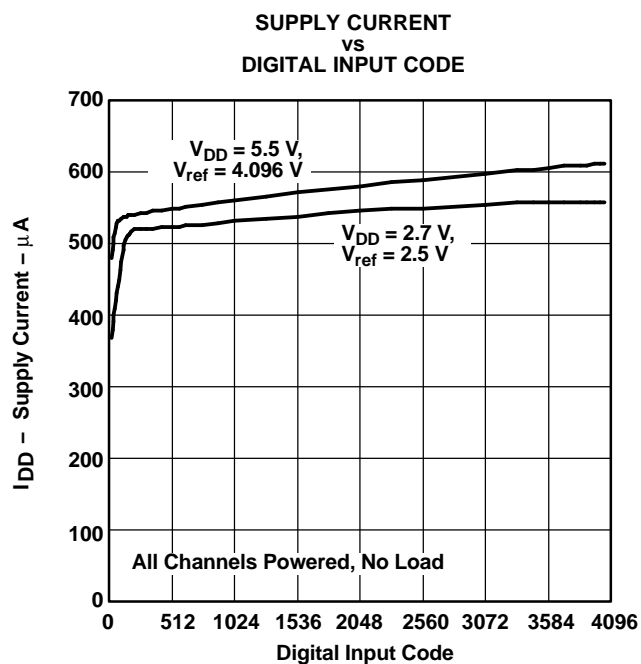


Figure 17.

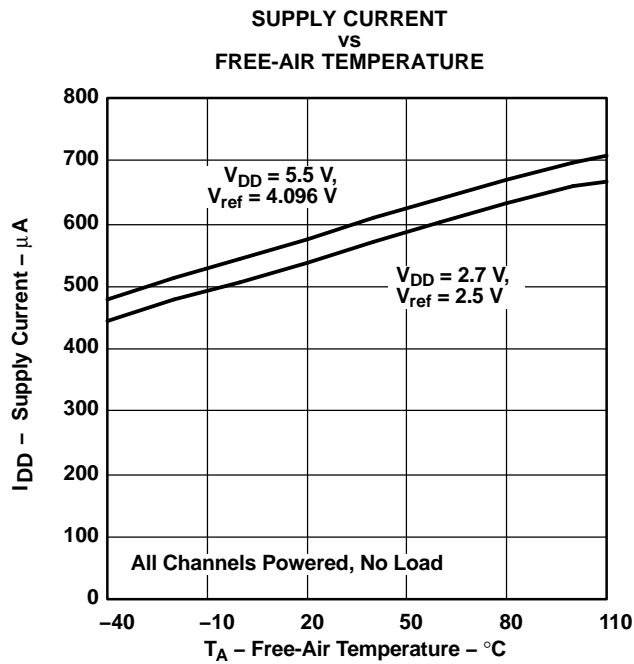
TYPICAL CHARACTERISTICS (continued)

Figure 18.

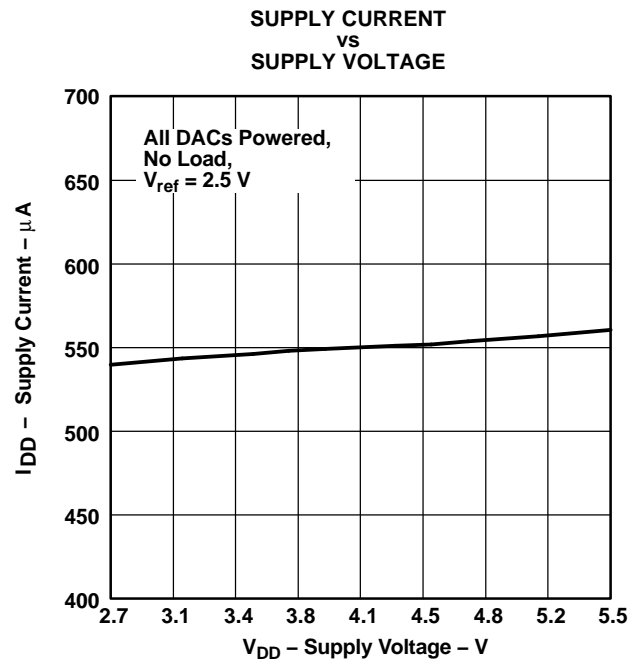


Figure 19.

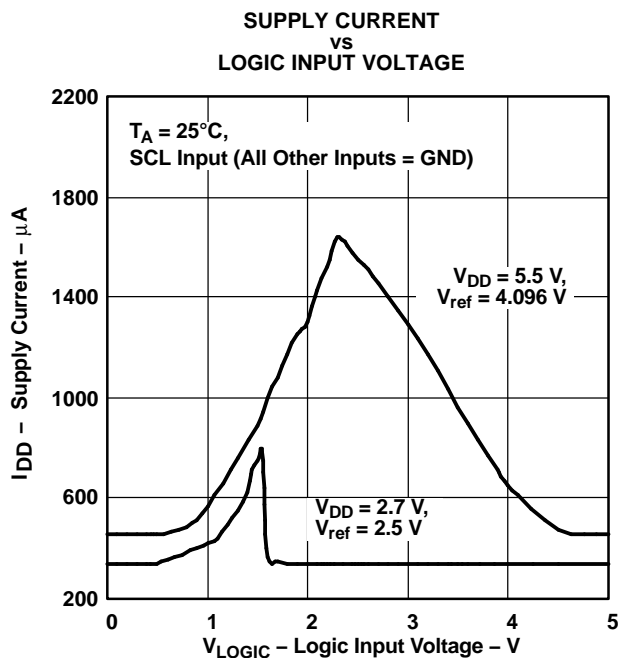


Figure 20.

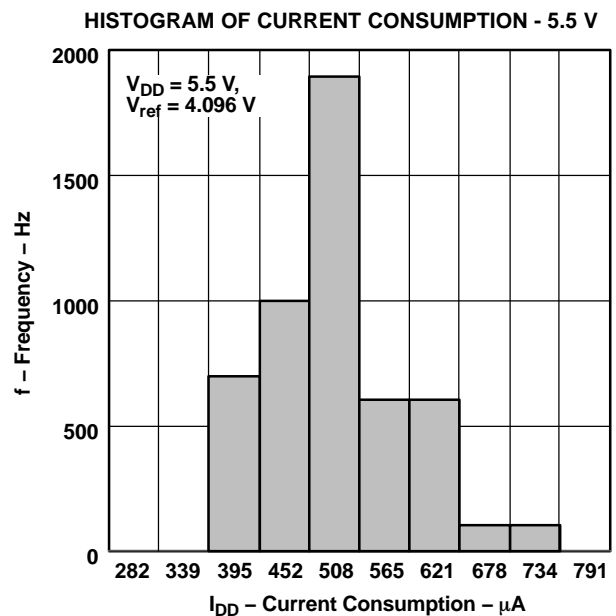


Figure 21.

TYPICAL CHARACTERISTICS (continued)

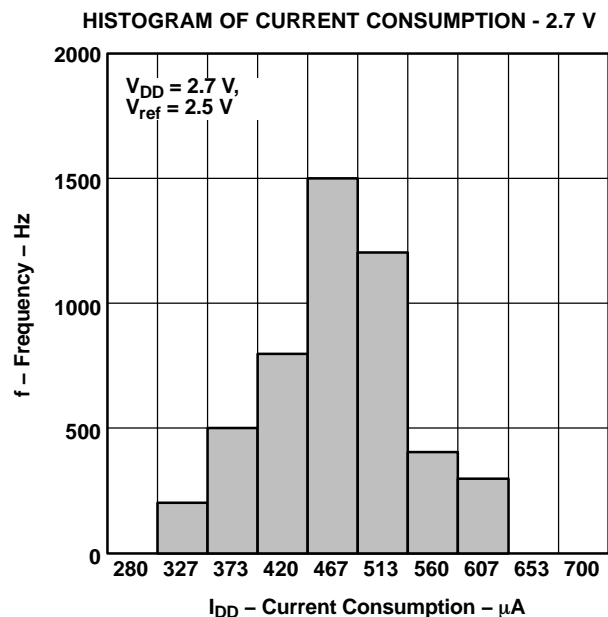


Figure 22.

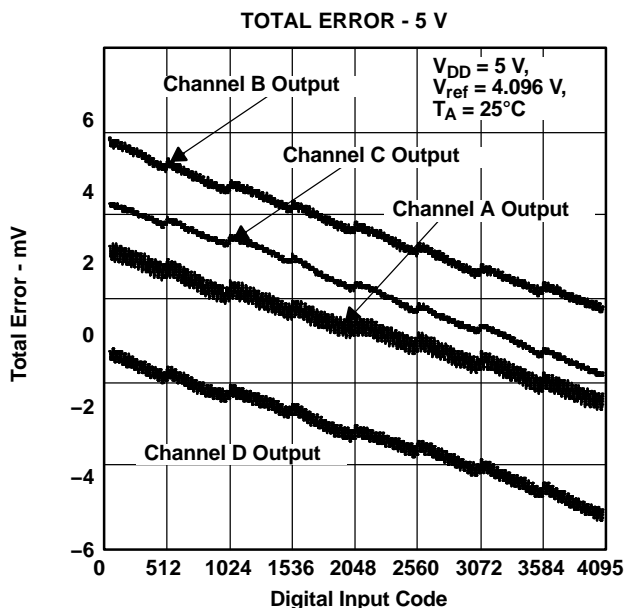


Figure 23.

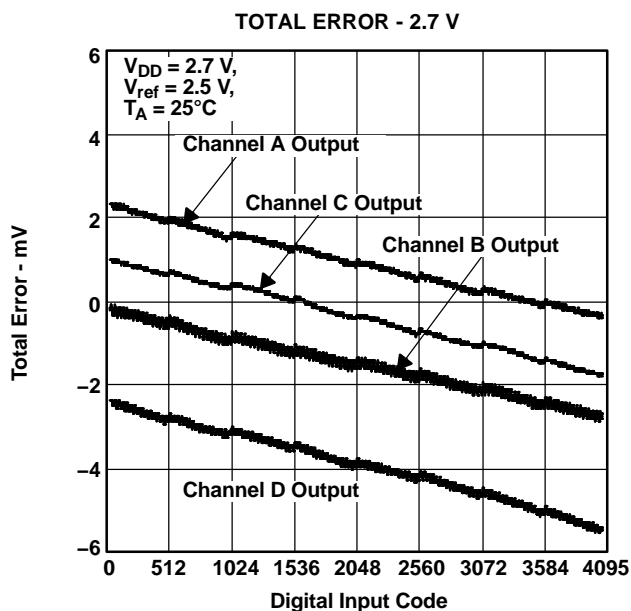


Figure 24.

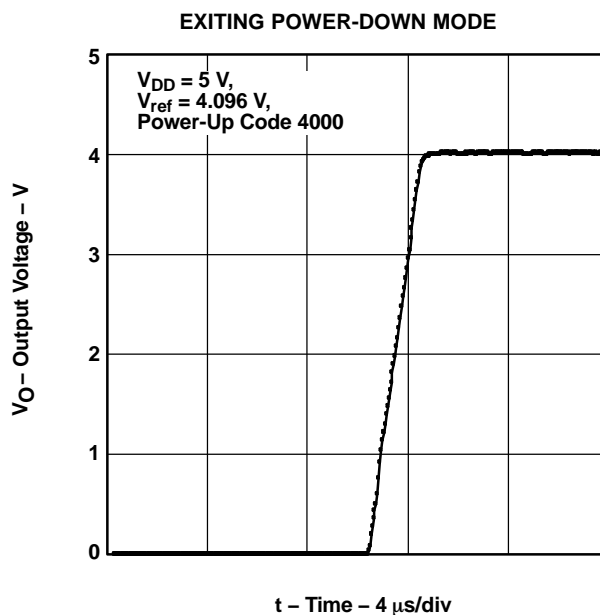


Figure 25.

TYPICAL CHARACTERISTICS (continued)

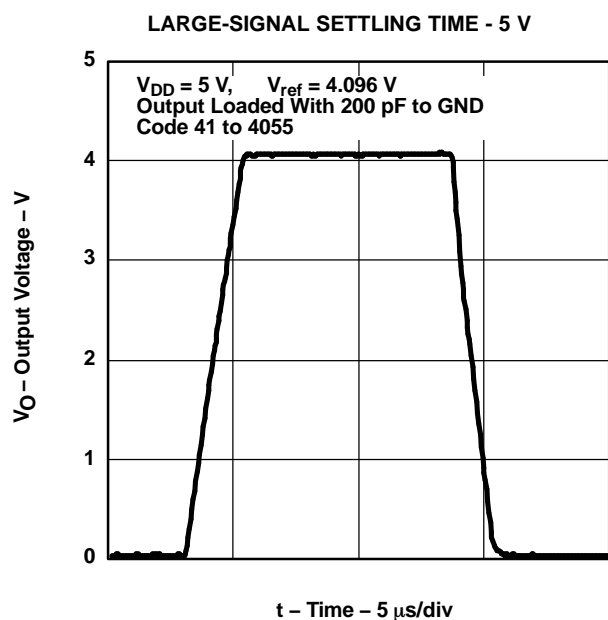


Figure 26.

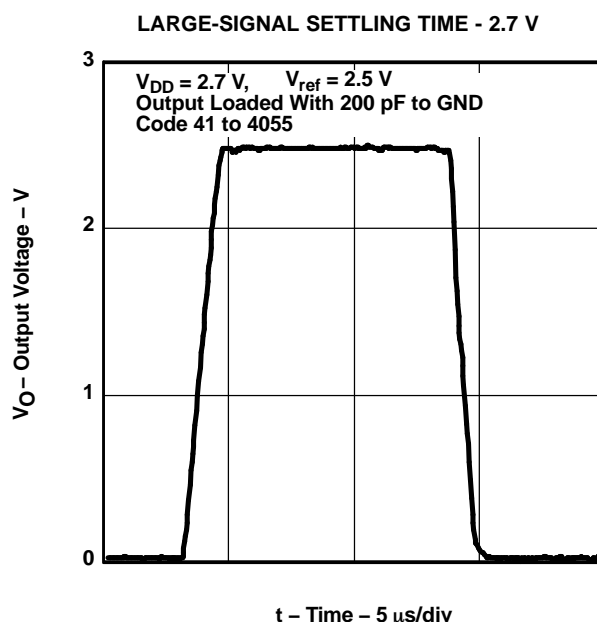


Figure 27.

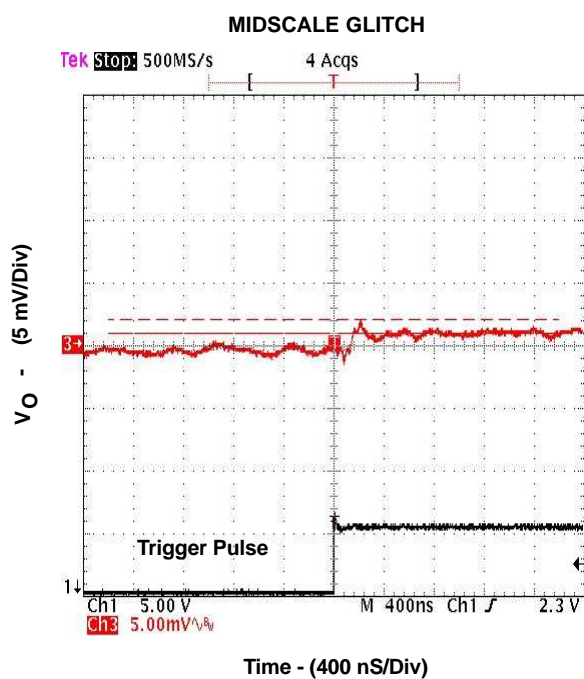


Figure 28.

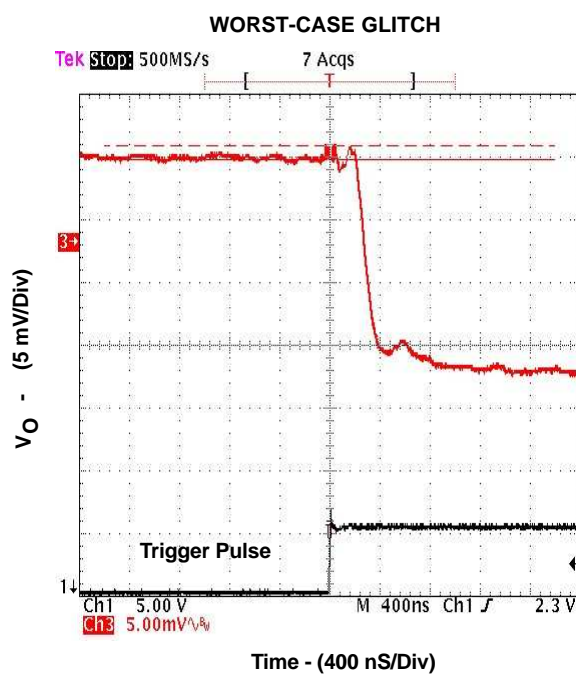


Figure 29.

TYPICAL CHARACTERISTICS (continued)

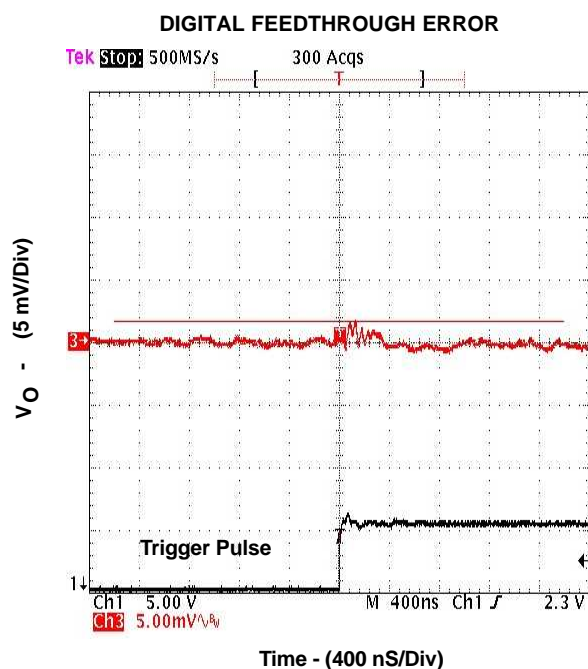


Figure 30.

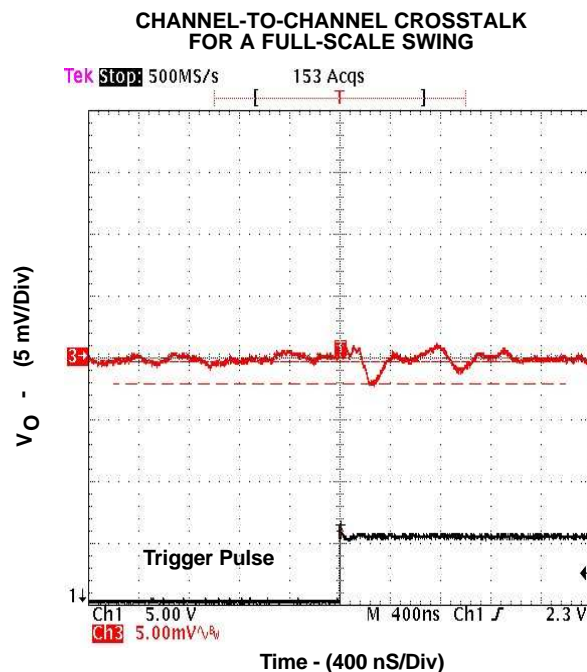


Figure 31.

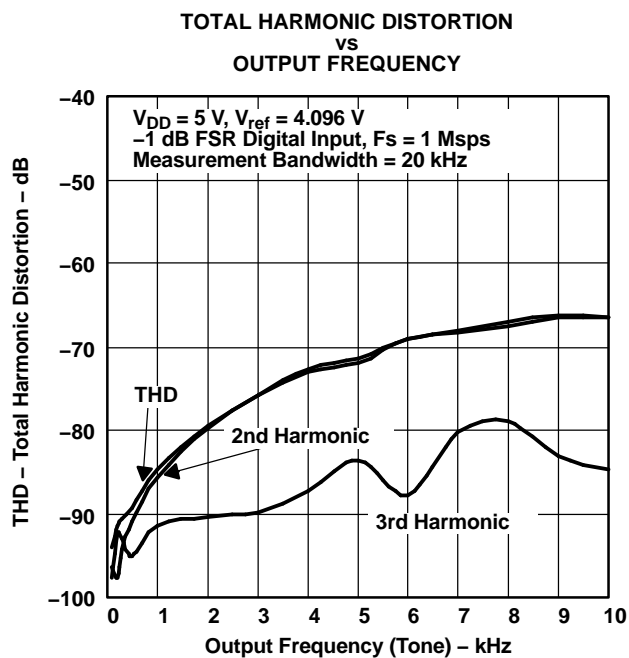


Figure 32.

3-Wire Serial Interface

The DAC7554 digital interface is a standard 3-wire SPI/QSPI/Microwire/DSP-compatible interface.

Table 1. Serial Interface Programming

CONTROL				DATA BITS	DAC(s)	FUNCTION
LD1	LD0	Sel1	Sel0	DB11-DB0		
0	0	0	0	data	A	Input register updated
0	0	0	1	data	B	Input register updated
0	0	1	0	data	C	Input register updated
0	0	1	1	data	D	Input register updated
0	1	0	0	data	A	DAC register updated, output updated
0	1	0	1	data	B	DAC register updated, output updated
0	1	1	0	data	C	DAC register updated, output updated
0	1	1	1	data	D	DAC register updated, output updated
1	0	0	0	data	A	Input register and DAC register updated, output updated
1	0	0	1	data	B	Input register and DAC register updated, output updated
1	0	1	0	data	C	Input register and DAC register updated, output updated
1	0	1	1	data	D	Input register and DAC register updated, output updated
1	1	0	0	data	A-D	Input register updated
1	1	0	1	data	A-D	DAC register updated, output updated
1	1	1	0	data	A-D	Input register and DAC register updated, output updated
1	1	1	1	data	--	Power-Down Mode - See Table 2
Sel1	Sel0	CHANNEL SELECT				
0	0	Channel A				
0	1	Channel B				
1	0	Channel C				
1	1	Channel D				
LD1	LD0	FUNCTION				
0	0	Single channel store. The selected input register is updated.				
0	1	Single channel DAC update. The selected DAC register is updated with input register information.				
1	0	Single channel update. The selected input and DAC register is updated.				
1	1	Depends on the Sel1 and Sel0 Bits				

POWER-DOWN MODE

In power-down mode, the DAC outputs are programmed to one of three output impedances, 1 k Ω , 100 k Ω , or floating.

Table 2. Power-Down Mode Control

EXTENDED CONTROL				DATA BITS						FUNCTION
LD1	LD0	Sel1	Sel0	DB11	DB10	DB9	DB8	DB7	DB6-DB0	
1	1	1	1	0	0	0	0	0	X	PWD Hi-Z (selected channel = A)
1	1	1	1	0	0	0	0	1	X	PWD 1 k Ω (selected channel = A)
1	1	1	1	0	0	0	1	0	X	PWD 100 k Ω (selected channel = A)
1	1	1	1	0	0	0	1	1	X	PWD Hi-Z (selected channel = A)
1	1	1	1	0	0	1	0	0	X	PWD Hi-Z (selected channel = B)
1	1	1	1	0	0	1	0	1	X	PWD 1 k Ω (selected channel = B)
1	1	1	1	0	0	1	1	0	X	PWD 100 k Ω (selected channel = B)
1	1	1	1	0	0	1	1	1	X	PWD Hi-Z (selected channel = B)
1	1	1	1	0	1	0	0	0	X	PWD Hi-Z (selected channel = C)
1	1	1	1	0	1	0	0	1	X	PWD 1 k Ω (selected channel = C)
1	1	1	1	0	1	0	1	0	X	PWD 100 k Ω (selected channel = C)
1	1	1	1	0	1	0	1	1	X	PWD Hi-Z (selected channel = C)
1	1	1	1	0	1	1	0	0	X	PWD Hi-Z (selected channel = D)
1	1	1	1	0	1	1	0	1	X	PWD 1 k Ω (selected channel = D)
1	1	1	1	0	1	1	1	0	X	PWD 100 k Ω (selected channel = D)
1	1	1	1	0	1	1	1	1	X	PWD Hi-Z (selected channel = D)
1	1	1	1	1	X	X	0	0	X	PWD Hi-Z (all channels)
1	1	1	1	1	X	X	0	1	X	PWD 1 k Ω (all channels)
1	1	1	1	1	X	X	1	0	X	PWD 100 k Ω (all channels)
1	1	1	1	1	X	X	1	1	X	PWD Hi-Z (all channels)
DB11	ALL CHANNELS FLAG									
0	See DB7–DB10									
1	DB10 and DB9 are Don't Care									
DB10	DB9	Channel Select								
0	0	Channel A								
0	1	Channel B								
1	0	Channel C								
1	1	Channel D								
DB8	DB7	Power-Down Mode								
0	0	Power-down Hi-Z								
0	1	Power-down 1 k Ω								
1	0	Power-down 100 k Ω								
1	1	Power-down Hi-Z								

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC7554 consists of a string DAC followed by an output buffer amplifier. Figure 33 shows a generalized block diagram of the DAC architecture.

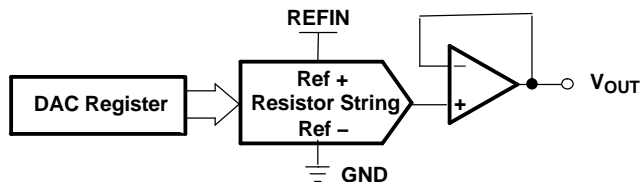


Figure 33. Typical DAC Architecture

The input coding to the DAC7554 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = REF_{IN} \times D/4096$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register which can range from 0 to 4095.

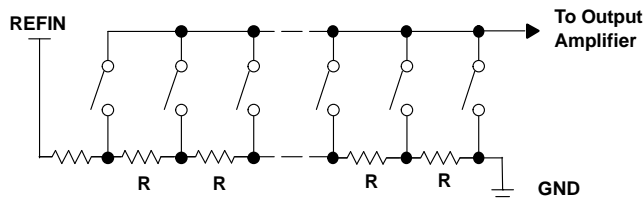


Figure 34. Typical Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 34. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is specified monotonic. The DAC7554 architecture uses four separate resistor strings to minimize channel-to-channel crosstalk.

OUTPUT BUFFER AMPLIFIERS

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD} . It is capable of driving a load of 2 k Ω in parallel with up to 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/ μ s with a half-scale settling time of 3 μ s with the output unloaded.

DAC External Reference Input

There is a single reference input pin for the four DACs. The reference input is unbuffered. The user can have a reference voltage as low as 0.25 V and as high as V_{DD} because there is no restriction due to headroom and footroom of any reference amplifier.

It is recommended to use a buffered reference in the external circuit (e.g., REF3140). The input impedance is typically 25 k Ω .

Power-On Reset

On power up, all internal registers are cleared and all channels are updated with zero-scale voltages. Until valid data is written, all DAC outputs remain in this state. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up. In order not to turn on ESD protection devices, V_{DD} should be applied before any other pin is brought high.

Power Down

The DAC7554 has a flexible power-down capability as described in Table 2. Individual channels could be powered down separately or all channels could be powered down simultaneously. During a power-down condition, the user has flexibility to select the output impedance of each channel. During power-down operation, each channel can have either 1-k Ω , 100-k Ω , or Hi-Z output impedance to ground.

SERIAL INTERFACE

The DAC7554 is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

16-Bit Word and Input Shift Register

The input shift register is 16 bits wide. DAC data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK, as shown in the Figure 1 timing diagram. The 16-bit word, illustrated in Table 1, consists of four control bits followed by 12 bits of DAC data. The data format is straight binary with all zeroes corresponding to 0-V output and all ones corresponding to full-scale output ($V_{REF} - 1$ LSB). Data is loaded MSB first (Bit 15) where the first two bits (LD1 and LD0) determine if the input register, DAC register, or both are updated with shift register input data. Bit 13 and bit 12 (Sel1 and Sel0) determine whether the data is for DAC A, DAC B, DAC C, DAC D, or all DACs. All channels are updated when bits 15 and 14 (LD1 and LD0) are high.

The $\overline{\text{SYNC}}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low, observing the minimum $\overline{\text{SYNC}}$ to SCLK falling edge setup time, t_4 . After $\overline{\text{SYNC}}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. Any data and clock pulses after the sixteenth falling edge of SCLK are ignored. No further serial data transfer occurs until $\overline{\text{SYNC}}$ is taken high and low again.

$\overline{\text{SYNC}}$ may be taken high after the falling edge of the sixteenth SCLK pulse, observing the minimum SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time, t_7 .

After the end of serial data transfer, data is automatically transferred from the input shift register to the input register of the selected DAC. If $\overline{\text{SYNC}}$ is taken high before the sixteenth falling edge of SCLK, the data transfer is aborted and the DAC input registers are not updated.

INTEGRAL AND DIFFERENTIAL LINEARITY

The DAC7554 uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within (+/-) 0.35 LSBs, and differential linearity error is typically within (+/-) 0.08 LSBs.

GLITCH ENERGY

The DAC7554 uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low, they are usually buried within the wide-band noise and cannot be easily detected. The DAC7554 glitch is typically well under 0.1 nV-s. Such low glitch energy provides more than 10X improvement over industry alternatives.

CHANNEL-TO-CHANNEL CROSSTALK

The DAC7554 architecture is designed to minimize channel-to-channel crosstalk. The voltage change in one channel does not affect the voltage output in another channel. The DC crosstalk is in the order of a few microvolts. AC crosstalk is also less than -100 dBs. This provides orders of magnitude improvement over certain competing architectures.

APPLICATION INFORMATION

Waveform Generation

Due to its exceptional linearity, low glitch, and low crosstalk, the DAC7554 is well suited for waveform generation (from DC to 10 kHz). The DAC7554 large-signal settling time is 5 μ s, supporting an update rate of 200 KSPS. However, the update rates

can exceed 1 MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, REF3140 (4.096 V) or REF02 (5.0 V) are recommended for reference voltage generation.

Generating ± 5 -V, ± 10 -V, and ± 12 -V Outputs For Precision Industrial Control

Industrial control applications can require multiple feedback loops consisting of sensors, ADCs, MCUs, DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

Loop Accuracy:

In a control loop, the ADC has to be accurate. Offset, gain, and the integral linearity errors of the DAC are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find it and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental change the loop can generate. A DNL error less than -1 LSB (non-monotonicity) can create loop instability. A DNL error greater than +1 LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop loses its stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ± 0.08 LSB typical DNL error, 755X DACs are great choices for precision control loops.

Loop Speed:

Many factors determine control loop speed. Typically, the ADC's conversion time, and the MCU's computation time are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop down only during the start-up. Once the loop reaches its steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop's transfer function, DAC glitches can also slow the loop down. With its 1 MSPS (small-signal) maximum data update rate, DAC7554 can support high-speed control loops. Ultra-low glitch energy of the DAC7554 significantly improves loop stability and loop settling time.

Generating Industrial Voltage Ranges:

For control loop applications, DAC gain and offset errors are not important parameters. This could be exploited to lower trim and calibration costs in a high-voltage control circuit design. Using a quad operational amplifier (OPA4130), and a voltage reference (REF3140), the DAC7554 can generate the wide voltage swings required by the control loop.

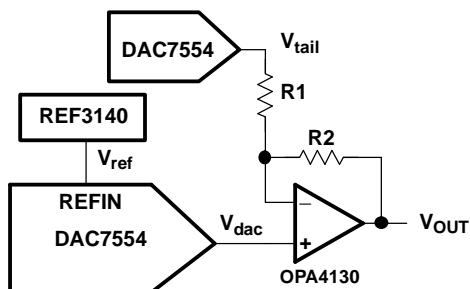


Figure 35. Low-cost, Wide-swing Voltage Generator for Control Loop Applications

The output voltage of the configuration is given by:

$$V_{out} = V_{ref} \left(\frac{R2}{R1} + 1 \right) \frac{D_{in}}{4096} - V_{tail} \frac{R2}{R1} \quad (1)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. Once R2 and R1 set the gain to include some minimal over-range, a DAC7554 channel could be used to set the required offset voltages. Residual errors are not an issue for loop accuracy because offset and gain errors could be tolerated. One DAC7554 channel can provide the Vtail voltage, while the other three DAC7554 channels can provide Vdac voltages to help generate three high-voltage outputs.

For ± 5 -V operation: R1=10 k Ω , R2 = 15 k Ω , Vtail = 3.33 V, Vref = 4.096 V

For ± 10 -V operation: R1=10 k Ω , R2 = 39 k Ω , Vtail = 2.56 V, Vref = 4.096 V

For ± 12 -V operation: R1=10 k Ω , R2 = 49 k Ω , Vtail = 2.45 V, Vref = 4.096 V

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DAC7554IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D754	Samples
DAC7554IDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D754	Samples
DAC7554IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D754	Samples
DAC7554IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D754	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7554IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7554IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

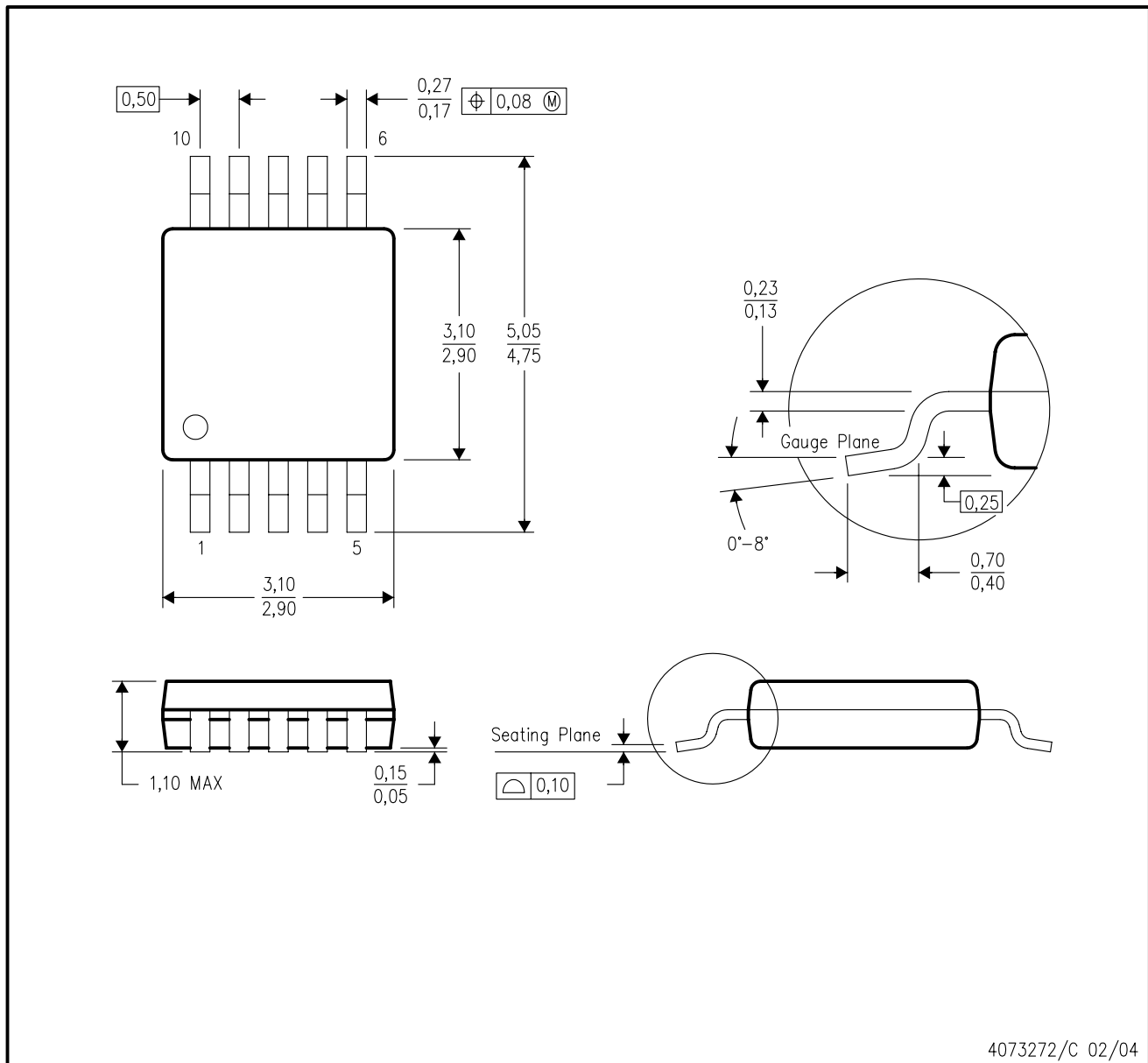


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7554IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
DAC7554IDGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com