# 36-Mbit (1 M × 36/2 M × 18) Pipelined SRAM with NoBL™ Architecture

## Features

- Pin-compatible and functionally equivalent to ZBT™
- Supports 250-MHz bus operations with zero wait states
  - Available speed grades are 250, 200 and 167 MHz
- Internally self-timed output buffer control to eliminate the need to use asynchronous $\overline{\text{OE}}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte Write capability
- 2.5 V core power supply
- 2.5 V/1.8 V I/O power supply
- Fast clock-to-output times
  - 2.6 ns (for 250-MHz device)
- Clock enable ($\overline{\text{CEN}}$) pin to suspend operation
- Synchronous self-timed writes
- CY7C1460AV25, CY7C1462AV25 available in JEDEC-standard Pb-free 100-pin TQFP package, Pb-free and non Pb-free 165-ball FBGA package.
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- Burst capability – linear or interleaved burst order
- “ZZ” sleep mode option and stop clock option

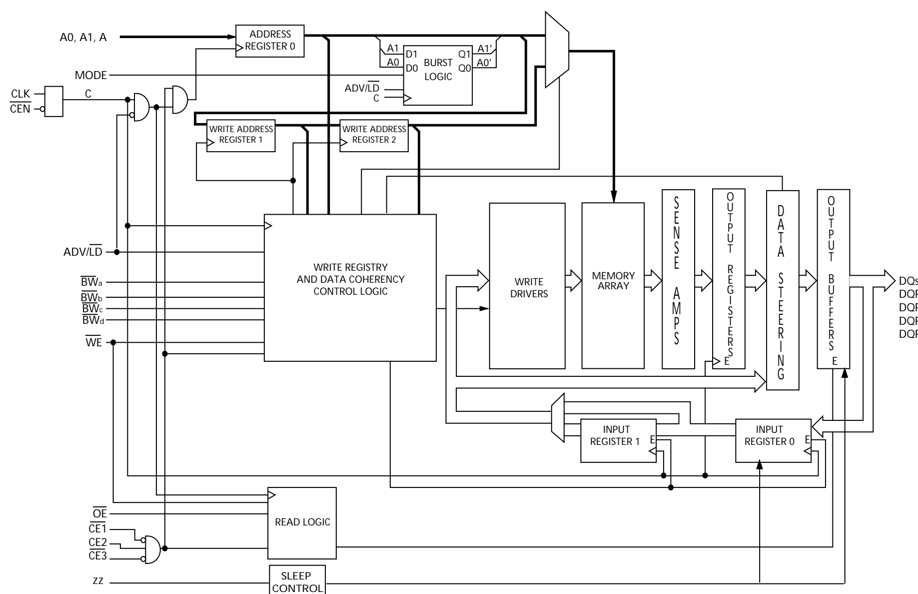
## Functional Description

The CY7C1460AV25/CY7C1462AV25 are 2.5 V, 1 M × 36/2 M × 18 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1460AV25/CY7C1462AV25 are equipped with the advanced NoBL logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The CY7C1460AV25/CY7C1462AV25 are pin-compatible and functionally equivalent to ZBT devices.

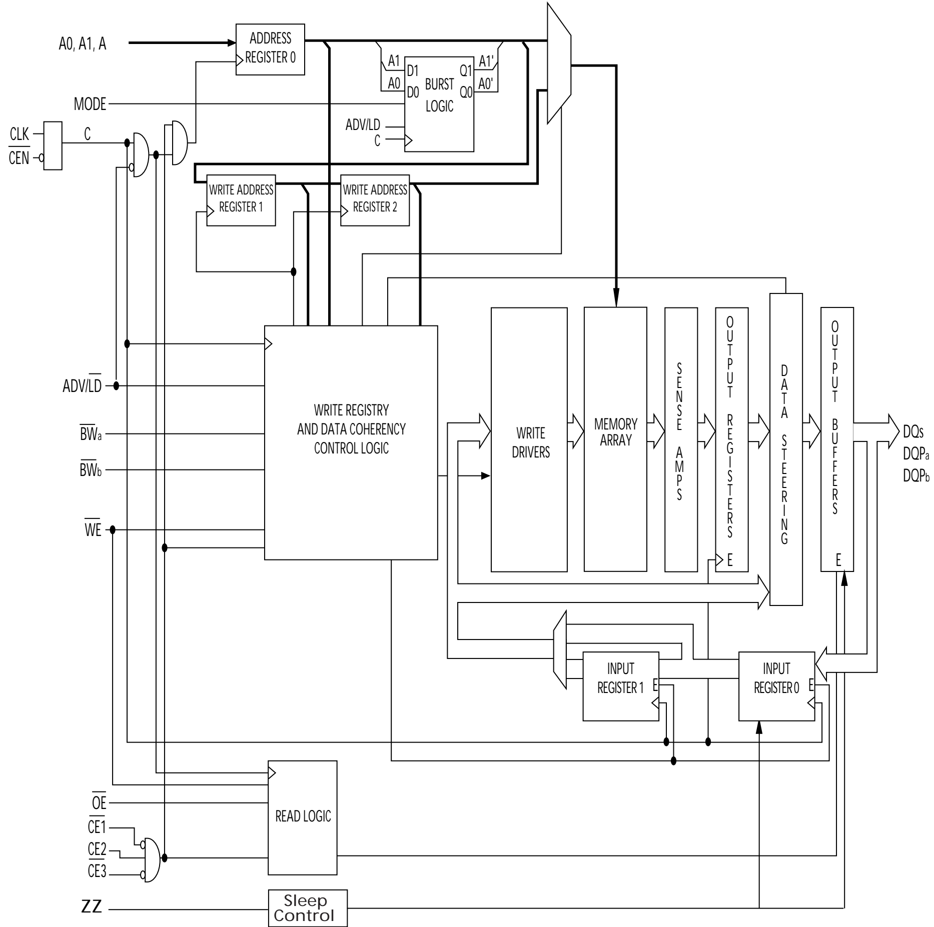
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{\text{CEN}}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Write operations are controlled by the byte write selects ($\overline{\text{BW}}_a$–$\overline{\text{BW}}_d$ for CY7C1460AV25 and $\overline{\text{BW}}_a$–$\overline{\text{BW}}_b$ for CY7C1462AV25) and a write enable ($\overline{\text{WE}}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{\text{CE}}_1$, $\text{CE}_2$, $\overline{\text{CE}}_3$) and an asynchronous output enable ($\overline{\text{OE}}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

## Logic Block Diagram – CY7C1460AV25



## Logic Block Diagram – CY7C1462AV25



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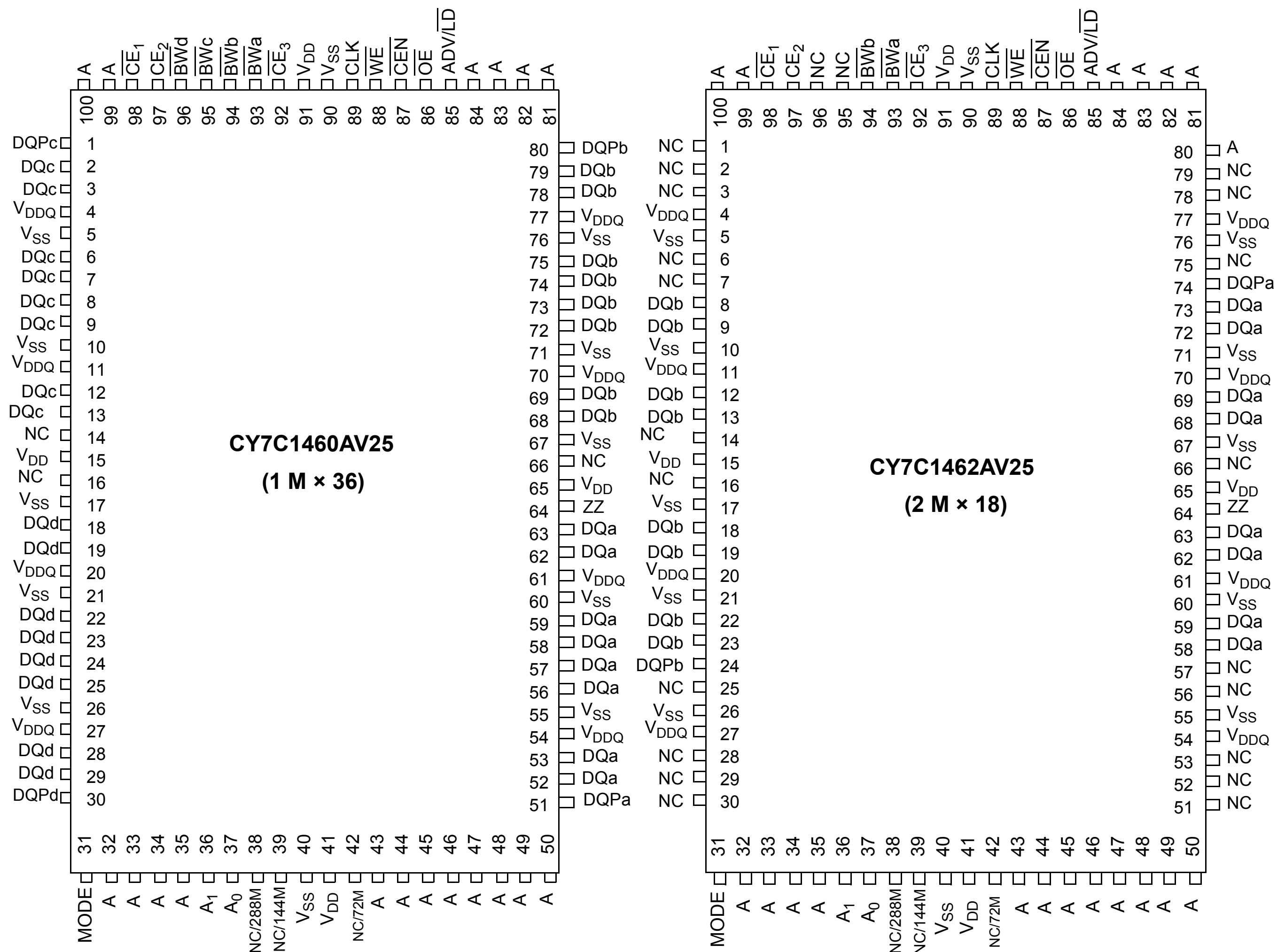
## Selection Guide

| Description | 250 MHz | 200 MHz | 167 MHz | Unit |
|---|---|---|---|---|
| Maximum access time | 2.6 | 3.2 | 3.4 | ns |
| Maximum operating current | 435 | 385 | 335 | mA |
| Maximum CMOS standby current | 120 | 120 | 120 | mA |

## Pin Configurations

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout**



## Pin Configurations *(continued)*

**Figure 2. 165-ball FBGA (15 × 17 × 1.4 mm) pinout**

**CY7C1460AV25 (1 M × 36)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC/576M | A | $\overline{CE_1}$ | $\overline{BW_c}$ | $\overline{BW_b}$ | $\overline{CE_3}$ | $\overline{CEN}$ | ADV/$\overline{LD}$ | A | A | NC |
| **B** | NC/1G | A | CE2 | $\overline{BW_d}$ | $\overline{BW_a}$ | CLK | $\overline{WE}$ | $\overline{OE}$ | A | A | NC |
| **C** | $DQP_c$ | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_b$ |
| **D** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **E** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **F** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **G** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **K** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **L** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **M** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **N** | $DQP_d$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **P** | NC/144M | NC/72M | A | A | TDI | A1 | TDO | A | A | A | NC/288M |
| **R** | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

**CY7C1462AV25 (2 M × 18)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC/576M | A | $\overline{CE_1}$ | $\overline{BW_b}$ | NC | $\overline{CE_3}$ | $\overline{CEN}$ | ADV/$\overline{LD}$ | A | A | A |
| **B** | NC/1G | A | CE2 | NC | $\overline{BW_a}$ | CLK | $\overline{WE}$ | $\overline{OE}$ | A | A | NC |
| **C** | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **D** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **E** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **F** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **G** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **K** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **L** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **M** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **N** | $DQP_b$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| **P** | NC/144M | NC/72M | A | A | TDI | A1 | TDO | A | A | A | NC/288M |
| **R** | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

## Pin Definitions

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-synchronous | **Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. |
| $\overline{BW}_a$, $\overline{BW}_b$, $\overline{BW}_c$, $\overline{BW}_d$ | Input-synchronous | **Byte write select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls $DQ_a$ and $DQP_a$, $\overline{BW}_b$ controls $DQ_b$ and $DQP_b$, $\overline{BW}_c$ controls $DQ_c$ and $DQP_c$, $\overline{BW}_d$ controls $DQ_d$ and $DQP_d$. |
| $\overline{WE}$ | Input-synchronous | **Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| ADV/$\overline{LD}$ | Input-synchronous | **Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address. |
| CLK | Input-clock | **Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW. |
| $\overline{CE}_1$ | Input-synchronous | **Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select/deselect the device. |
| $CE_2$ | Input-synchronous | **Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. |
| $\overline{CE}_3$ | Input-synchronous | **Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select/deselect the device. |
| $\overline{OE}$ | Input-asynchronous | **Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| $\overline{CEN}$ | Input-synchronous | **Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required. |
| $DQ_a$, $DQ_b$, $DQ_c$, $DQ_d$ | I/O-synchronous | **Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_X$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, $DQ_a$–$DQ_d$ are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. |
| $DQP_a$, $DQP_b$, $DQP_c$, $DQP_d$ | I/O-synchronous | **Bidirectional data parity I/O lines**. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, $DQP_a$ is controlled by $\overline{BW}_a$, $DQP_b$ is controlled by $\overline{BW}_b$, $DQP_c$ is controlled by $\overline{BW}_c$, and $DQP_d$ is controlled by $\overline{BW}_d$. |
| MODE | Input strap pin | **Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order. |
| TDO | JTAG serial output synchronous | **Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. |
| TDI | JTAG serial input synchronous | **Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. |
| TMS | Test mode select synchronous | **This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK. |
| TCK | JTAG-clock | **Clock input to the JTAG circuitry**. |

## Pin Definitions *(continued)*

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| $V_{DD}$ | Power supply | **Power supply inputs to the core of the device**. |
| $V_{DDQ}$ | I/O power supply | **Power supply for the I/O circuitry**. |
| $V_{SS}$ | Ground | **Ground for the device**. Should be connected to ground of the system. |
| NC | N/A | **No connects**. This pin is not connected to the die. |
| NC/72M | N/A | **Not connected to the die**. Can be tied to any voltage level. |
| NC/144M | N/A | **Not connected to the die**. Can be tied to any voltage level. |
| NC/288M | N/A | **Not connected to the die**. Can be tied to any voltage level. |
| NC/576M | N/A | **Not connected to the die**. Can be tied to any voltage level. |
| NC/1G | N/A | **Not connected to the die**. Can be tied to any voltage level. |
| ZZ | Input-asynchronous | **ZZ “sleep” Input**. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down. |

## Functional Overview

The CY7C1460AV25/CY7C1462AV25 are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ($t_{CO}$) is 2.6 ns (250-MHz device).

Accesses can be initiated by asserting all three chip enables ($CE_1$, $CE_2$, $CE_3$) active at the rising edge of the clock. If clock enable (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable (WE). $BW_{[x]}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable (WE). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($CE_1$, $CE_2$, $CE_3$) and an asynchronous output enable (OE) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD should be driven LOW once the device has been deselected in order to load a new address for the next operation.

### Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) $CE_1$, $CE_2$, and $CE_3$ are all asserted active, (3) the write enable input signal WE is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.6 ns (200-MHz device) provided OE is active LOW. After the first clock of the read access the output buffers are controlled by OE and the internal control logic. OE must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

### Burst Read Accesses

The CY7C1460AV25/CY7C1462AV25 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Accesses section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/LD will increment the internal burst counter regardless of the state of chip enables inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

### Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) $CE_1$, $CE_2$, and $CE_3$ are all asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address inputs is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the OE input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460AV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1462AV25). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460AV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1462AV25) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1460AV25 and $\overline{BW}_{a,b}$ for CY7C1462AV25) signals. The CY7C1460AV25/CY7C1462AV25 provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1460AV25/CY7C1462AV25 are common I/O devices, data should not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP

( $DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460AV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1462AV25) inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1460AV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1462AV25) are automatically three-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

### Burst Write Accesses

The CY7C1460AV25/CY7C1462AV25 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Accesses section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ( $\overline{BW}_{a,b,c,d}$ for CY7C1460AV25 and $\overline{BW}_{a,b}$ for CY7C1462AV25) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$, must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or $V_{DD}$)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

### ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | $ZZ \geq V_{DD} - 0.2$ V | – | 100 | mA |
| $t_{ZZS}$ | Device operation to ZZ | $ZZ \geq V_{DD} - 0.2$ V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | $ZZ \leq 0.2$ V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

## Truth Table

The truth table for CY7C1460AV25/CY7C1462AV25 follows. [1, 2, 3, 4, 5, 6, 7]

| Operation | Address Used | $\overline{CE}$ | ZZ | ADV/$\overline{LD}$ | $\overline{WE}$ | $\overline{BW}_x$ | $\overline{OE}$ | $\overline{CEN}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|
| Deselect cycle | None | H | L | L | X | X | X | L | L–H | Tri-state |
| Continue deselect cycle | None | X | L | H | X | X | X | L | L–H | Tri-state |
| Read cycle (begin burst) | External | L | L | L | H | X | L | L | L–H | Data out (Q) |
| Read cycle (continue burst) | Next | X | L | H | X | X | L | L | L–H | Data out (Q) |
| NOP/dummy read (begin burst) | External | L | L | L | H | X | H | L | L–H | Tri-state |
| Dummy read (continue burst) | Next | X | L | H | X | X | H | L | L–H | Tri-state |
| Write cycle (begin burst) | External | L | L | L | L | L | X | L | L–H | Data in (D) |
| Write cycle (continue burst) | Next | X | L | H | X | L | X | L | L–H | Data in (D) |
| NOP/WRITE ABORT (begin burst) | None | L | L | L | L | H | X | L | L–H | Tri-state |
| WRITE ABORT (continue burst) | Next | X | L | H | X | H | X | L | L–H | Tri-state |
| IGNORE CLOCK EDGE (stall) | Current | X | L | X | X | X | X | H | L–H | – |
| Sleep MODE | None | X | H | X | X | X | X | X | X | Tri-state |

**Notes**

1. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BWx}$ = L signifies at least one byte write select is active, $\overline{BWx}$ = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle $DQ_s$ and $DQP_X$ = Three-state when $\overline{OE}$ is inactive or when the device is deselected, and $DQ_s$=data when $\overline{OE}$ is active.

## Partial Write Cycle Description

The partial write cycle description table for CY7C1460AV25 follows. [8, 9, 10, 11]

| Function (CY7C1460AV25) | $\overline{WE}$ | $\overline{BW_d}$ | $\overline{BW_c}$ | $\overline{BW_b}$ | $\overline{BW_a}$ |
|---|---|---|---|---|---|
| Read | H | X | X | X | X |
| Write – no bytes written | L | H | H | H | H |
| Write byte a – ($DQ_a$ and $DQP_a$) | L | H | H | H | L |
| Write byte b – ($DQ_b$ and $DQP_b$) | L | H | H | L | H |
| Write bytes b, a | L | H | H | L | L |
| Write byte c – ($DQ_c$ and $DQP_c$) | L | H | L | H | H |
| Write bytes c, a | L | H | L | H | L |
| Write bytes c, b | L | H | LL | L | H |
| Write bytes c, b, a | L | H | L | L | L |
| Write byte d – ($DQ_d$ and $DQP_d$) | L | L | H | H | H |
| Write bytes d, a | L | L | H | H | L |
| Write bytes d, b | L | L | H | L | H |
| Write bytes d, b, a | L | L | H | L | L |
| Write bytes d, c | L | L | L | H | H |
| Write bytes d, c, a | L | L | L | H | L |
| Write bytes d, c, b | L | L | L | L | H |
| Write all bytes | L | L | L | L | L |

**Notes**
8. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BWx}$ = L signifies at least one byte write select is active, $\overline{BWx}$ = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by $\overline{WE}$ and $\overline{BW_X}$. See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

## Partial Write Cycle Description

The partial write cycle description table for CY7C1462AV25 follows. [12, 13, 14, 15]

| Function (CY7C1462AV25) | $\overline{WE}$ | $\overline{BW}_b$ | $\overline{BW}_a$ |
|---|---|---|---|
| Read | H | X | X |
| Write – no bytes written | L | H | H |
| Write byte a – ($DQ_a$ and $DQP_a$) | L | H | L |
| Write byte b – ($DQ_b$ and $DQP_b$) | L | L | H |
| Write both bytes | L | L | L |

**Notes**

12. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}x$ = L signifies at least one byte write select is active, $\overline{BW}x$ = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
13. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
14. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
15. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write will be done based on which byte write is active.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1460AV25/CY7C1462AV25 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 2.5 V/1.8 V I/O logic level.

The CY7C1460AV25/CY7C1462AV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

### Test Access Port (TAP)

*Test Clock (TCK)*

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

*Test Mode Select (TMS)*

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

*Test Data-In (TDI)*

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller Block Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

*Test Data-Out (TDO)*

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram on page 14). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

*Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 15. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

*Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

*Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The length of the Boundary Scan Register for the SRAM in different packages is listed in the Scan Register Sizes table.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order on page 19 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

*Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 18.

### TAP Instruction Set

*Overview*

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes on page 18. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and

TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

*IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

*SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is given during the “Update IR” state.

*SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1-mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture set-up plus hold times ($t_{CS}$ and $t_{CH}$). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

*BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

*EXTEST*

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

*EXTEST Output Bus Tri-State*

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

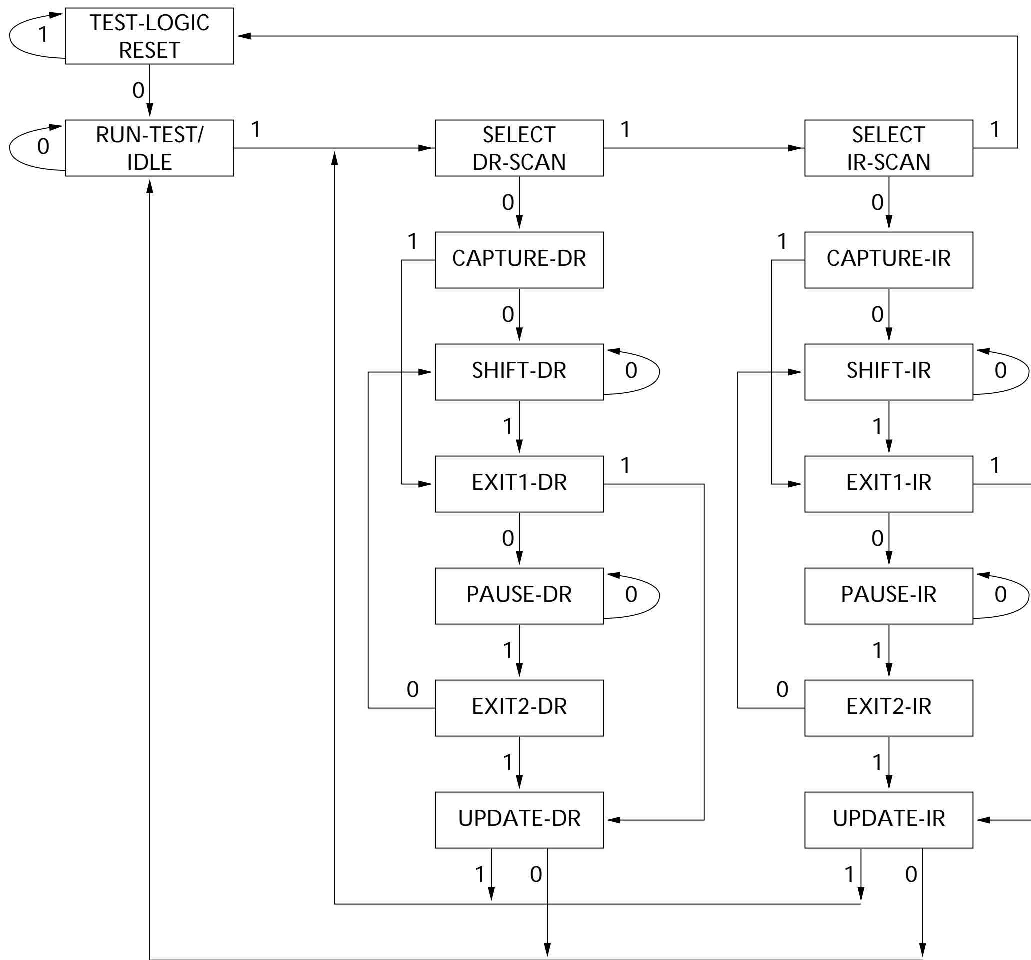
The boundary scan register has a special bit located at bit #89 (for 165-ball FBGA package). When this scan cell, called the “extest output bus tri-state,” is latched into the preload register during the “Update-DR” state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR,” the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

*Reserved*

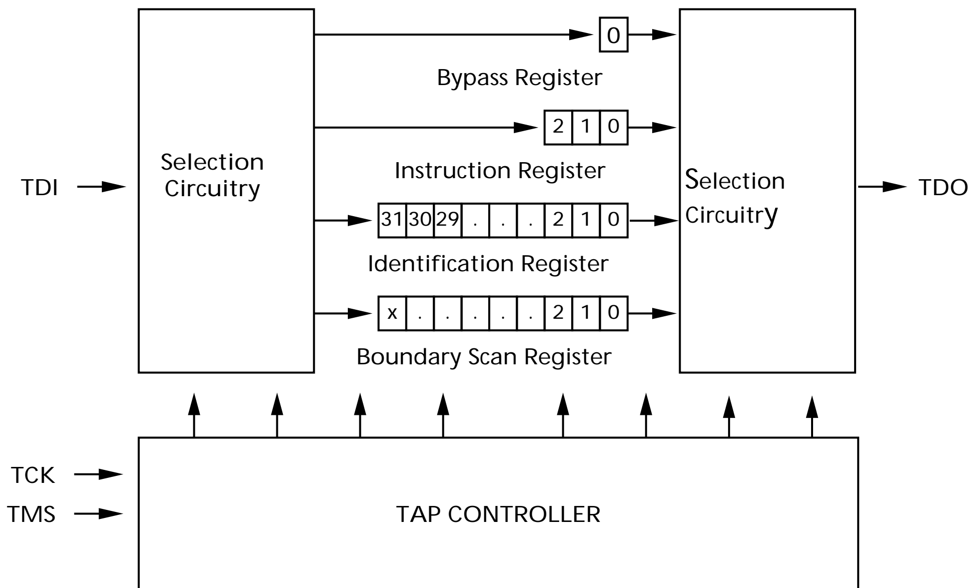
These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

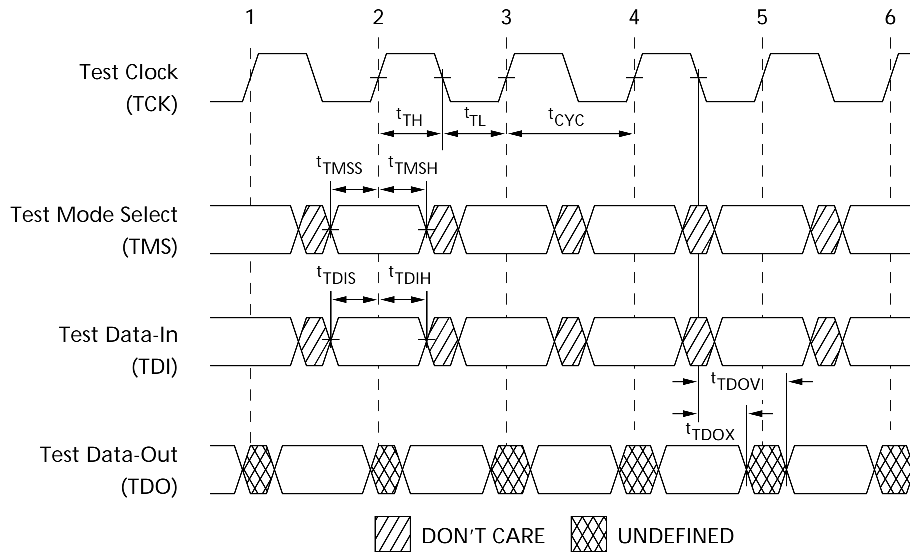



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

## TAP Controller Block Diagram




## TAP Timing



## TAP AC Switching Characteristics

Over the Operating Range

| Parameter [16, 17] | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Clock** | | | | |
| $t_{TCYC}$ | TCK clock cycle time | 50 | – | ns |
| $t_{TF}$ | TCK clock frequency | – | 20 | MHz |
| $t_{TH}$ | TCK clock HIGH time | 20 | – | ns |
| $t_{TL}$ | TCK clock LOW time | 20 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK clock LOW to TDO valid | – | 10 | ns |
| $t_{TDOX}$ | TCK clock LOW to TDO invalid | 0 | – | ns |
| **Set-up Times** | | | | |
| $t_{TMSS}$ | TMS set-up to TCK clock rise | 5 | – | ns |
| $t_{TDIS}$ | TDI set-up to TCK clock rise | 5 | – | ns |
| $t_{CS}$ | Capture set-up to TCK rise | 5 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS hold after TCK clock rise | 5 | – | ns |
| $t_{TDIH}$ | TDI hold after clock rise | 5 | – | ns |
| $t_{CH}$ | Capture hold after clock rise | 5 | – | ns |

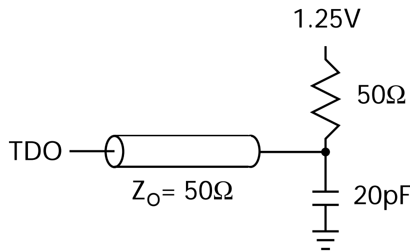
**Notes**

16. $t_{CS}$ and $t_{CH}$ refer to the set-up and hold time requirements of latching data from the boundary scan register.
17. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F$ = 1 ns.

## 2.5 V TAP AC Test Conditions

Input pulse levels ............................................. $V_{SS}$ to 2.5 V
Input rise and fall time ................................................... 1 ns
Input timing reference levels ........................ .............. 1.25 V
Output reference levels ............................................ 1.25 V
Test load termination supply voltage .......................... 1.25 V

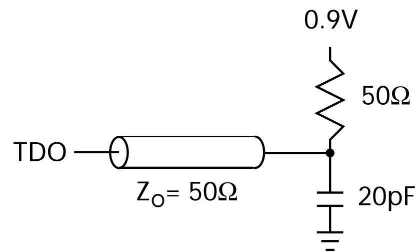
## 2.5 V TAP AC Output Load Equivalent




## 1.8 V TAP AC Test Conditions

Input pulse levels ................................ 0.2 V to $V_{DDQ}$ – 0.2 V
Input rise and fall time ................................................... 1 ns
Input timing reference levels ........................................ 0.9 V
Output reference levels ................................................ 0.9 V
Test load termination supply voltage ............................ 0.9 V

## 1.8 V TAP AC Output Load Equivalent




## TAP DC Electrical Characteristics and Operating Conditions

(0 °C < $T_A$ < +70 °C; $V_{DD}$ = 2.5 V ± 0.125 V unless otherwise noted)

| Parameter [18] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH}$ = –1.0 mA | $V_{DDQ}$ = 2.5 V | 1.7 | – | V |
| $V_{OH2}$ | Output HIGH voltage | $I_{OH}$ = –100 µA | $V_{DDQ}$ = 2.5 V | 2.1 | – | V |
| | | | $V_{DDQ}$ = 1.8 V | 1.6 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL}$ = 1.0 mA | $V_{DDQ}$ = 2.5 V | – | 0.4 | V |
| $V_{OL2}$ | Output LOW voltage | $I_{OL}$ = 100 µA | $V_{DDQ}$ = 2.5 V | – | 0.2 | V |
| | | | $V_{DDQ}$ = 1.8 V | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | | $V_{DDQ}$ = 2.5 V | 1.7 | $V_{DD}$ + 0.3 | V |
| | | | $V_{DDQ}$ = 1.8 V | 1.26 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | | $V_{DDQ}$ = 2.5 V | –0.3 | 0.7 | V |
| | | | $V_{DDQ}$ = 1.8 V | –0.3 | 0.36 | V |
| $I_X$ | Input load current | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |

**Note**
18. All voltages referenced to $V_{SS}$ (GND).

## Identification Register Definitions

| Instruction Field | CY7C1460AV25 (1 M × 36) | CY7C1462AV25 (2 M × 18) | Description |
|---|---|---|---|
| Revision number (31:29) | 000 | 000 | Describes the version number |
| Device depth (28:24) | 01011 | 01011 | Reserved for internal use |
| Architecture/memory type(23:18) | 001000 | 001000 | Defines memory type and architecture |
| Bus width/density(17:12) | 100111 | 010111 | Defines width and density |
| Cypress JEDEC ID code (11:1) | 00000110100 | 00000110100 | Allows unique identification of SRAM vendor |
| ID register presence indicator (0) | 1 | 1 | Indicates the presence of an ID register |

## Scan Register Sizes

| Register Name | Bit Size (× 36) | Bit Size (× 18) |
|---|---|---|
| Instruction | 3 | 3 |
| Bypass | 1 | 1 |
| ID | 32 | 32 |
| Boundary scan order (165-ball FBGA package) | 89 | 89 |

## Instruction Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

## Boundary Scan Order

165-ball FBGA [19]

**CY7C1460AV25 (1 M × 36), CY7C1462AV25 (2 M × 18)**

| Bit# | Ball ID | Bit# | Ball ID | Bit# | Ball ID | Bit# | Ball ID |
|---|---|---|---|---|---|---|---|
| 1 | N6 | 26 | E11 | 51 | A3 | 76 | N1 |
| 2 | N7 | 27 | D11 | 52 | A2 | 77 | N2 |
| 3 | N10 | 28 | G10 | 53 | B2 | 78 | P1 |
| 4 | P11 | 29 | F10 | 54 | C2 | 79 | R1 |
| 5 | P8 | 30 | E10 | 55 | B1 | 80 | R2 |
| 6 | R8 | 31 | D10 | 56 | A1 | 81 | P3 |
| 7 | R9 | 32 | C11 | 57 | C1 | 82 | R3 |
| 8 | P9 | 33 | A11 | 58 | D1 | 83 | P2 |
| 9 | P10 | 34 | B11 | 59 | E1 | 84 | R4 |
| 10 | R10 | 35 | A10 | 60 | F1 | 85 | P4 |
| 11 | R11 | 36 | B10 | 61 | G1 | 86 | N5 |
| 12 | H11 | 37 | A9 | 62 | D2 | 87 | P6 |
| 13 | N11 | 38 | B9 | 63 | E2 | 88 | R6 |
| 14 | M11 | 39 | C10 | 64 | F2 | 89 | Internal |
| 15 | L11 | 40 | A8 | 65 | G2 | | |
| 16 | K11 | 41 | B8 | 66 | H1 | | |
| 17 | J11 | 42 | A7 | 67 | H3 | | |
| 18 | M10 | 43 | B7 | 68 | J1 | | |
| 19 | L10 | 44 | B6 | 69 | K1 | | |
| 20 | K10 | 45 | A6 | 70 | L1 | | |
| 21 | J10 | 46 | B5 | 71 | M1 | | |
| 22 | H9 | 47 | A5 | 72 | J2 | | |
| 23 | H10 | 48 | A4 | 73 | K2 | | |
| 24 | G11 | 49 | B4 | 74 | L2 | | |
| 25 | F11 | 50 | B3 | 75 | M2 | | |

**Note**

19. Bit# 89 is preset HIGH.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ................................ –65 °C to +150 °C

Ambient temperature with power applied .......................................... –55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to GND .......–0.5 V to +3.6 V

Supply voltage on $V_{DDQ}$ relative to GND ...... –0.5 V to $+V_{DD}$

DC to outputs in tri-state ...................–0.5 V to $V_{DDQ}$ + 0.5 V

DC input voltage .................................–0.5 V to $V_{DD}$ + 0.5 V

Current into outputs (LOW) ........................................ 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .......................... > 2001V

Latch-up current ................................................... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 2.5 V – 5% / + 5% | 1.7 V to $V_{DD}$ |
| Industrial | –40 °C to +85 °C | | |

## Electrical Characteristics

Over the Operating Range

| Parameter [20, 21] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | | 2.375 | 2.625 | V |
| $V_{DDQ}$ | I/O supply voltage | for 2.5 V I/O | | 2.375 | $V_{DD}$ | V |
| | | for 1.8 V I/O | | 1.7 | 1.9 | V |
| $V_{OH}$ | Output HIGH voltage | for 2.5 V I/O, $I_{OH}$ = –1.0 mA | | 2.0 | – | V |
| | | for 1.8 V I/O, $I_{OH}$ = –100 µA | | 1.6 | – | V |
| $V_{OL}$ | Output LOW voltage | for 2.5 V I/O, $I_{OL}$ = 1.0 mA | | – | 0.4 | V |
| | | for 1.8 V I/O, $I_{OL}$ = 100 µA | | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage [20] | for 2.5 V I/O | | 1.7 | $V_{DD}$ + 0.3 V | V |
| | | for 1.8 V I/O | | 1.26 | $V_{DD}$ + 0.3 V | V |
| $V_{IL}$ | Input LOW voltage [20] | for 2.5 V I/O | | –0.3 | 0.7 | V |
| | | for 1.8 V I/O | | –0.3 | 0.36 | V |
| $I_X$ | Input leakage current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input current of MODE | Input = $V_{SS}$ | | –30 | | µA |
| | | Input = $V_{DD}$ | | – | 5 | µA |
| | Input current of ZZ | Input = $V_{SS}$ | | –5 | – | µA |
| | | Input = $V_{DD}$ | | – | 30 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_I$ ≤ $V_{DDQ,}$ output disabled | | –5 | 5 | µA |
| $I_{DD}$ | $V_{DD}$ operating supply | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 4-ns cycle, 250 MHz | – | 435 | mA |
| | | | 5-ns cycle, 200 MHz | – | 385 | mA |
| | | | 6-ns cycle, 167 MHz | – | 335 | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | Max $V_{DD}$, device deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ = $1/t_{CYC}$ | All speed grades | – | 185 | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | Max $V_{DD}$, device deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3 V, f = 0 | All speed grades | – | 120 | mA |

**Notes**
20. Overshoot: $V_{IH(AC)} < V_{DD}$ +1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
21. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter [20, 21] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SB3}$ | Automatic CE power-down current – CMOS inputs | Max $V_{DD}$, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$ | All speed grades | – | 160 | mA |
| $I_{SB4}$ | Automatic CE power-down current – TTL inputs | Max $V_{DD}$, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0 | All speed grades | – | 135 | mA |

## Capacitance

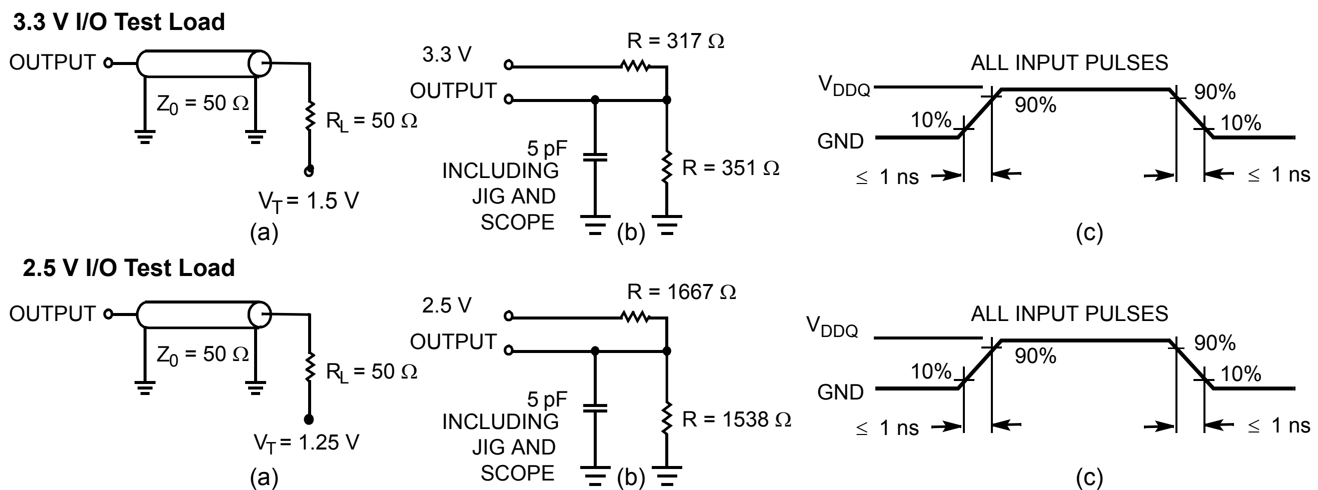
| Parameter [22] | Description | Test Conditions | 100-pin TQFP Max | 165-ball FBGA Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 2.5 V $V_{DDQ}$ = 2.5 V | 6.5 | 7 | pF |
| $C_{CLK}$ | Clock input capacitance | | 3 | 7 | pF |
| $C_{I/O}$ | Input/Output capacitance | | 5.5 | 6 | pF |

## Thermal Resistance

| Parameter [22] | Description | Test Conditions | 100-pin TQFP Package | 165-ball FBGA Package | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 25.21 | 20.8 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 2.58 | 3.2 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**




**Note**
22. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

| Parameter [23, 24] | Description | -250 | | -200 | | -167 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{Power}$[25] | $V_{CC}$(typical) to the first access read or write | 1 | – | 1 | – | 1 | – | ms |
| **Clock** | | | | | | | | |
| $t_{CYC}$ | Clock cycle time | 4.0 | – | 5.0 | – | 6.0 | – | ns |
| $F_{MAX}$ | Maximum operating frequency | – | 250 | – | 200 | – | 167 | MHz |
| $t_{CH}$ | Clock HIGH | 1.5 | – | 2.0 | – | 2.4 | – | ns |
| $t_{CL}$ | Clock LOW | 1.5 | – | 2.0 | – | 2.4 | – | ns |
| **Output Times** | | | | | | | | |
| $t_{CO}$ | Data output valid after CLK rise | – | 2.6 | – | 3.2 | – | 3.4 | ns |
| $t_{EOV}$ | $\overline{OE}$ LOW to output valid | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| $t_{DOH}$ | Data output hold after CLK rise | 1.0 | – | 1.5 | – | 1.5 | – | ns |
| $t_{CHZ}$ | Clock to high Z [26, 27, 28] | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| $t_{CLZ}$ | Clock to low Z [26, 27, 28] | 1.0 | – | 1.3 | – | 1.5 | – | ns |
| $t_{EOHZ}$ | $\overline{OE}$ HIGH to output high Z [26, 27, 28] | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| $t_{EOLZ}$ | $\overline{OE}$ LOW to output low Z [26, 27, 28] | 0 | – | 0 | – | 0 | – | ns |
| **Set-up Times** | | | | | | | | |
| $t_{AS}$ | Address set-up before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| $t_{DS}$ | Data input set-up before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| $t_{CENS}$ | $\overline{CEN}$ set-up before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| $t_{WES}$ | $\overline{WE}$, $\overline{BW}_x$ set-up before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| $t_{ALS}$ | ADV/$\overline{LD}$ set-up before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| $t_{CES}$ | Chip select set-up | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| **Hold Times** | | | | | | | | |
| $t_{AH}$ | Address hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| $t_{DH}$ | Data input hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| $t_{CENH}$ | $\overline{CEN}$ hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| $t_{WEH}$ | $\overline{WE}$, $\overline{BW}_x$ hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| $t_{ALH}$ | ADV/$\overline{LD}$ hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| $t_{CEH}$ | Chip select hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |

**Notes**

23. Timing reference is 1.25 V when $V_{DDQ}$ = 2.5 V and 0.9 V when $V_{DDQ}$ = 1.8 V.
24. Test conditions shown in (a) of Figure 3 on page 21 unless otherwise noted.
25. This part has a voltage regulator internally; $t_{power}$ is the time power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
26. $t_{CHZ}$, $t_{CLZ}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with AC test conditions shown in (b) of Figure 3 on page 21. Transition is measured ±200 mV from steady-state voltage.
27. At any given voltage and temperature, $t_{EOHZ}$ is less than $t_{EOLZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
28. This parameter is sampled and not 100% tested.

## Switching Waveforms

**Figure 4. Read/Write/Timing** [29, 30, 31]

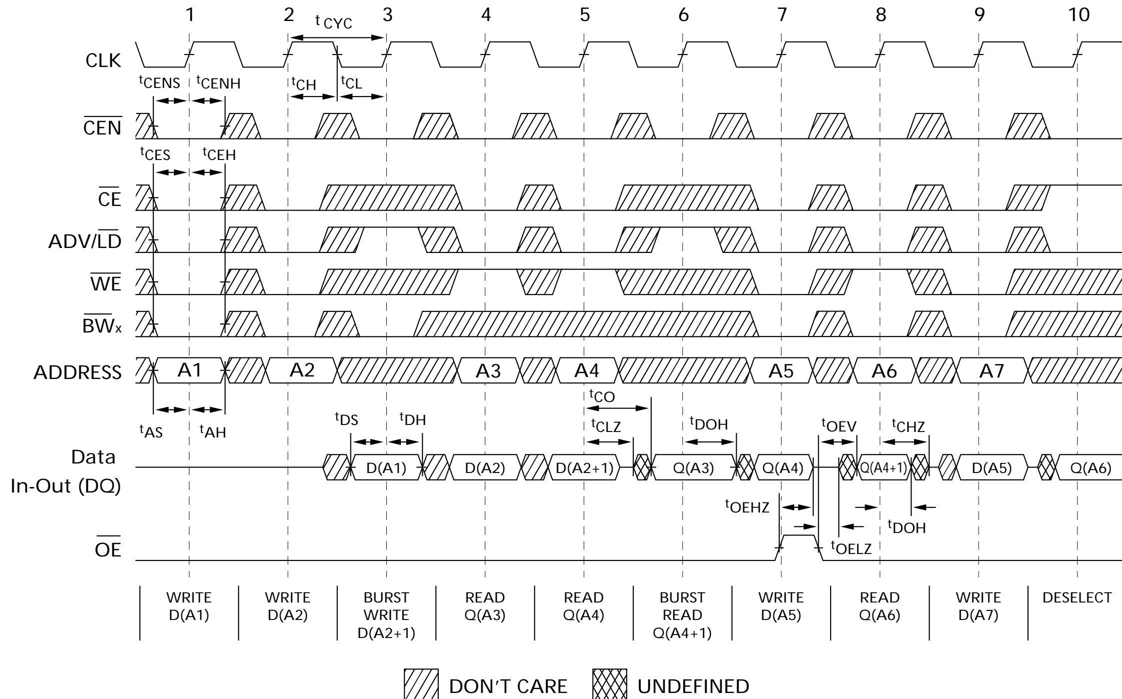
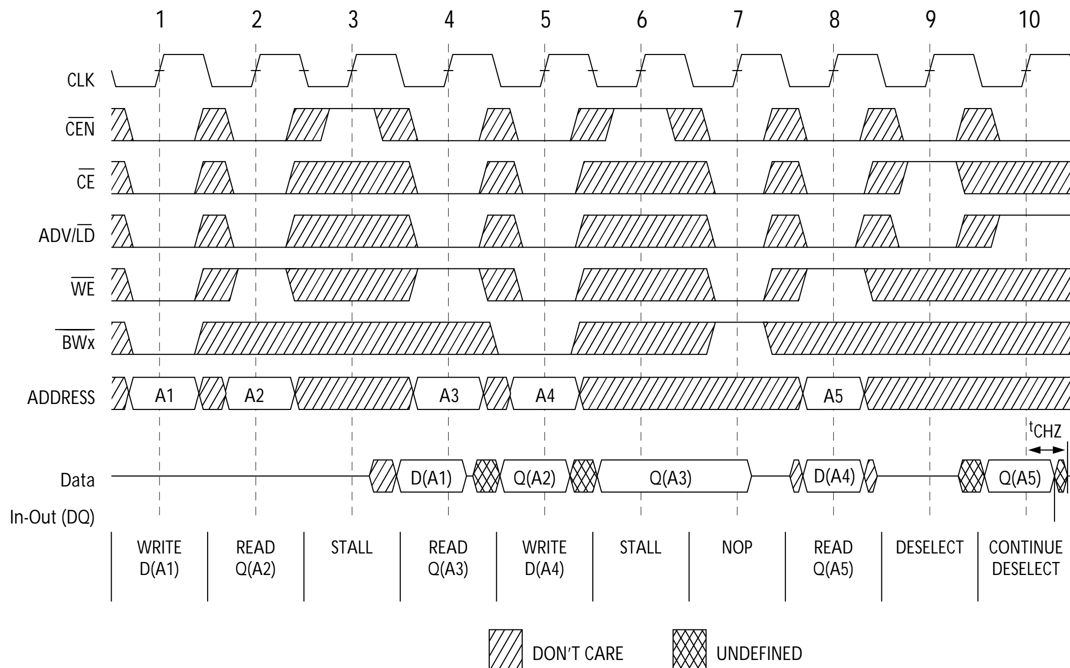



**Figure 5. NOP, STALL and DESELECT Cycles** [29, 30, 32]

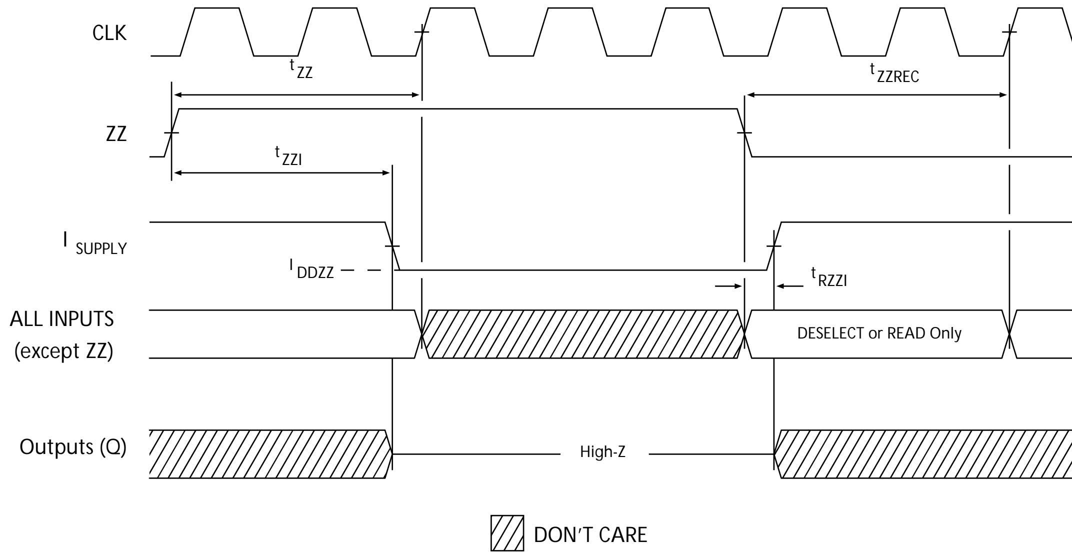



**Notes**

29. For this waveform ZZ is tied low.
30. When CE is LOW, $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When CE is HIGH, $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
31. Order of the burst sequence is determined by the status of the MODE (0=Linear, 1=Interleaved). Burst operations are optional.
32. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.

## Switching Waveforms *(continued)*

**Figure 6. ZZ Mode Timing** [33, 34]




**Notes**

33. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
34. I/Os are in high Z when exiting ZZ sleep mode.

## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available.For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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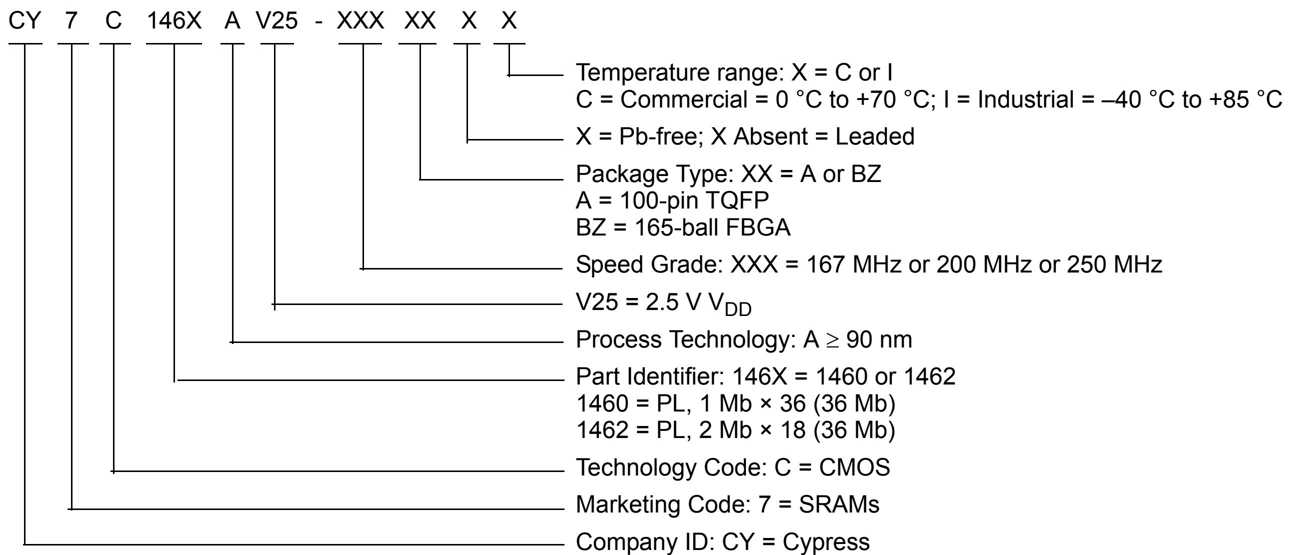
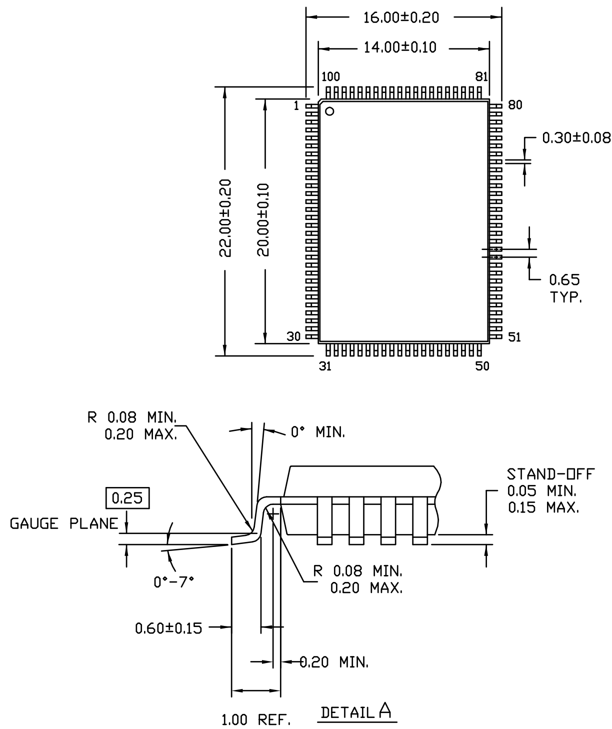
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 167 | CY7C1460AV25-167AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1460AV25-167BZC | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) | |
| | CY7C1462AV25-167BZI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) | Industrial |
| | CY7C1460AV25-167BZXI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) Pb-free | |
| 200 | CY7C1460AV25-200BZXI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) Pb-free | Industrial |
| | CY7C1460AV25-200BZI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) | |
| | CY7C1460AV25-200BZXC | 51-85165 | 165-ball FBGA (15 × 17 × 1.4 mm) Pb-free | Commercial |
| | CY7C1462AV25-200AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | |
| 250 | CY7C1460AV25-250AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |

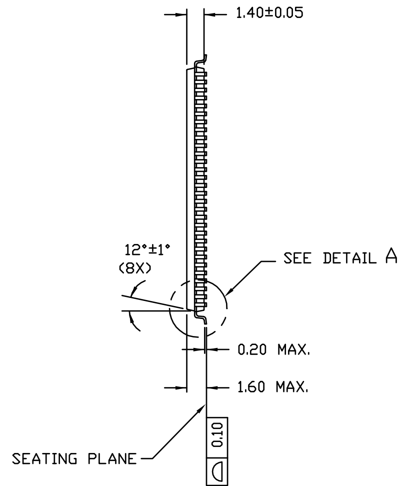
### Ordering Code Definitions



## Package Diagrams

**Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050**




NOTE:

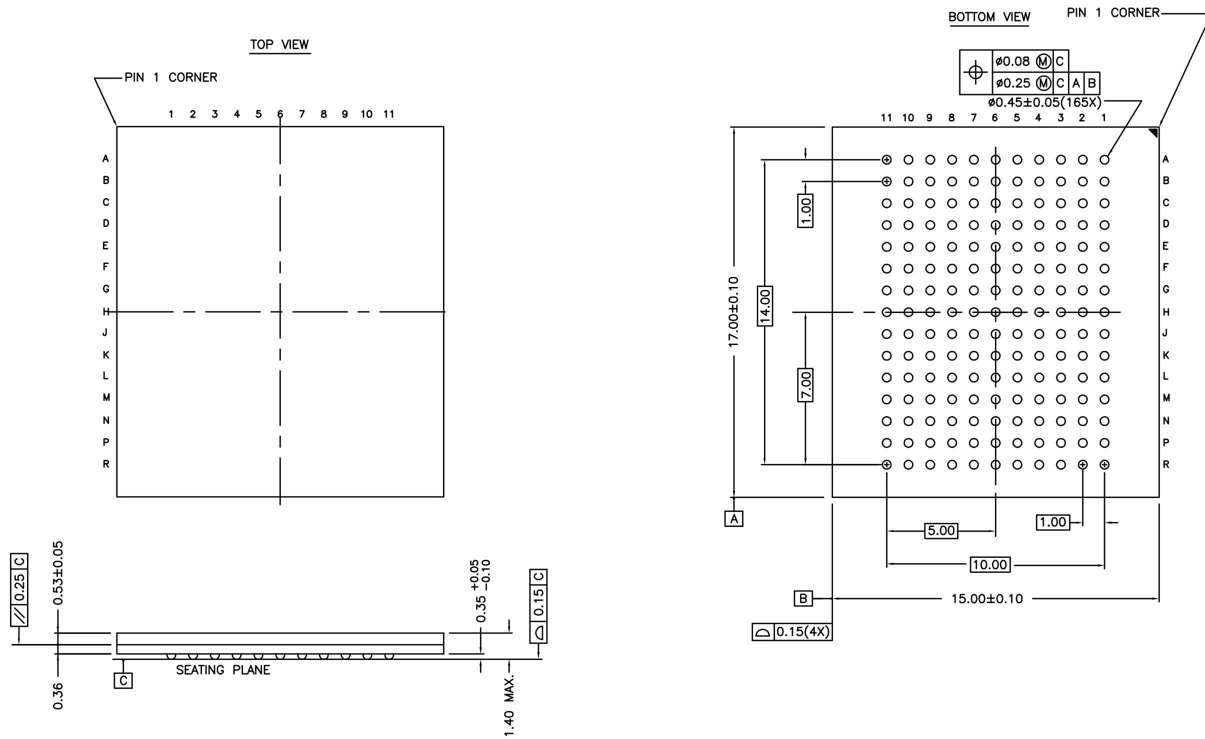
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

## Package Diagrams *(continued)*

**Figure 8. 165-ball FBGA (15 × 17 × 1.4 mm) (0.45 Ball Diameter) Package Outline, 51-85165**

NOTES:
SOLDER PAD TYPE: SOLDER MASK DEFINED (SMD)
PACKAGE WEIGHT: 0.60g
JEDEC REFERENCE: MO-216 / ISSUE E
PACKAGE CODES: BB0AA / BW0AG




51-85165 *D

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | chip enable |
| $\overline{CEN}$ | clock enable |
| CMOS | complementary metal-oxide-semiconductor |
| EIA | electronic industries alliance |
| FBGA | fine-pitch ball grid array |
| I/O | input/output |
| JEDEC | joint electron devices engineering council |
| JTAG | joint test action group |
| LSB | least significant bit |
| MSB | most significant bit |
| NoBL | No Bus Latency |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| TAP | test access port |
| TCK | test clock |
| TMS | test mode select |
| TDI | test data-in |
| TDO | test data-out |
| TQFP | thin quad flat pack |
| TTL | transistor-transistor logic |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1460AV25/CY7C1462AV25, 36-Mbit (1 M × 36/2 M × 18) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05354 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 254911 | See ECN | SYT | New data sheet<br>Part number changed from previous revision (New and old part number differ by the letter “A”) |
| *A | 303533 | See ECN | SYT | Updated Pin Configurations (Changed H9 pin from $V_{SSQ}$ to $V_{SS}$ for 209-ball FBGA).<br>Updated Electrical Characteristics (Changed the test condition for $V_{OL}$ parameter from $V_{DD}$ = Min. to $V_{DD}$ = Max., changed maximum value of $I_{DD}$ parameter from 450 mA, 400 mA and 350 mA to 435 mA, 385 mA and 335 mA for 250 MHz, 200 MHz and 167 MHz respectively, changed maximum value of $I_{SB1}$ parameter from 190 mA, 180 mA and 170 mA to 185 mA for 250 MHz, 200 MHz and 167 MHz respectively, changed maximum value of $I_{SB2}$ parameter from 80 mA to 100 mA for all frequencies, changed maximum value of $I_{SB3}$ parameter from 180 mA, 170 mA and 160 mA to 160 mA for 250 MHz, 200 MHz and 167 MHz respectively, changed maximum value of $I_{SB4}$ parameter from 100 mA to 110 mA for all frequencies).<br>Updated Thermal Resistance (Replaced values of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from TBD to respective Thermal Values for all Packages).<br>Updated Capacitance (Changed values of $C_{IN}$, $C_{CLK}$ and $C_{I/O}$ parameters to 6.5 pF, 3 pF and 5.5 pF from 5 pF, 5 pF and 7 pF for 100-pin TQFP Package).<br>Updated Switching Characteristics (Changed maximum value of $t_{CO}$ parameter from 3.0 ns to 3.2 ns for 200 MHz Speed Bin, changed maximum value of $t_{DOH}$ parameter from 1.3 ns to 1.5 ns for 200 MHz Speed Bin).<br>Updated Ordering Information (Added Pb-free information for 100-pin TQFP, 165-ball FBGA and 209-ball FBGA packages). |
| *B | 331778 | See ECN | SYT | Updated Pin Configurations (Modified Address Expansion balls in the pinouts for 165-ball FBGA and 209-ball FBGA Package as per JEDEC standards).<br>Updated Pin Definitions.<br>Updated Operating Range (Added Industrial Temperature Range).<br>Updated Electrical Characteristics (Updated test conditions for $V_{OL}$ and $V_{OH}$ parameters, changed maximum value of $I_{SB2}$ parameter from 100 mA to 120 mA, changed maximum value of $I_{SB4}$ parameter from 110 mA to 135 mA respectively).<br>Updated Capacitance (Changed values of $C_{IN}$, $C_{CLK}$ and $C_{I/O}$ parameters to 7 pF, 7 pF and 6 pF from 5 pF, 5 pF and 7 pF for 165-ball FBGA Package).<br>Updated Ordering Information (By shading and unshading MPNs as per availability). |
| *C | 417547 | See ECN | RXU | Changed status from Preliminary to Final.<br>Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”.<br>Updated Electrical Characteristics (Updated Note 21 (Changed test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$), changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE”, changed minimum value of $I_X$ parameter (corresponding to Input current of MODE (Input = $V_{SS}$)) from –5 µA to –30 µA, changed maximum value of $I_X$ parameter (corresponding to Input current of MODE (Input = $V_{DD}$)) from 30 µA to 5 µA respectively, changed minimum value of $I_X$ parameter (corresponding to Input current of ZZ (Input = $V_{SS}$)) from –30 µA to –5 µA, changed maximum value of $I_X$ parameter (corresponding to Input current of ZZ (Input = $V_{DD}$)) from 5 µA to 30 µA respectively).<br>Updated Ordering Information (Replaced Package Name column with Package Diagram in the Ordering Information table).<br>Updated Package Diagrams. |

## Document History Page *(continued)*

| Document Title: CY7C1460AV25/CY7C1462AV25, 36-Mbit (1 M × 36/2 M × 18) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05354 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| *D | 473650 | See ECN | VKN | Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND).<br>Updated TAP AC Switching Characteristics (Changed minimm value of $t_{TH}$ and $t_{TL}$ parameters from 25 ns to 20 ns, changed maximum value of $t_{TDOV}$ parameter from 5 ns to 10 ns).<br>Updated Ordering Information (Updated part numbers). |
| *E | 2898564 | 03/24/10 | NJY | Updated Ordering Information (Removed inactive parts).<br>Updated Package Diagrams. |
| *F | 3023843 | 09/28/2010 | NJY | Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure.<br>Minor edits and updated in new template. |
| *G | 3067448 | 10/21/2010 | NJY | Updated Ordering Information (Updated part numbers). |
| *H | 3342808 | 08/11/2011 | OSN | Updated Package Diagrams.<br>Updated in new template. |
| *I | 3591743 | 05/10/2012 | NJY / PRIT | Updated Features (Removed CY7C1464AV25 related information, removed 209-ball FBGA package related information).<br>Updated Functional Description (Removed CY7C1464AV25 related information).<br>Removed Logic Block Diagram – CY7C1464AV25.<br>Updated Pin Configurations (Removed CY7C1464AV25 related information, removed 209-ball FBGA package related information).<br>Updated Pin Definitions.<br>Updated Functional Overview (Removed CY7C1464AV25 related information).<br>Updated Truth Table (Removed CY7C1464AV25 related information).<br>Removed Partial Write Cycle Description (Corresponding to CY7C1464AV25).<br>Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1464AV25 related information, removed 209-ball FBGA package related information).<br>Updated Identification Register Definitions (Removed CY7C1464AV25 related information).<br>Updated Scan Register Sizes (Removed Bit Size (× 72) column, removed 209-ball FBGA package related information).<br>Removed Boundary Scan Order (Corresponding to 209-ball FBGA package).<br>Updated Capacitance (Removed 209-ball FBGA package related information).<br>Updated Thermal Resistance (Removed 209-ball FBGA package related information).<br>Updated Package Diagrams (spec 51-85165 (changed revision from *C to *D), removed 209-ball FBGA package related information (spec 51-85167)). |
| *J | 3753130 | 09/24/2012 | PRIT | No technical updates. Completing sunset review. |

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