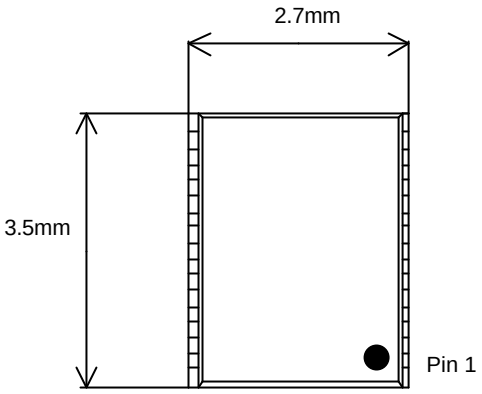
SONY â SP5T GSM TRIPLE-BAND / GPRS ANTENNA SWITCH

CXG1122EN

DESCRIPTION



VSON-16P-01

Pin Pitch 0.4mm

The CXG1122EN is one of a range of **low insertion loss**, high power MMIC antenna switches for GSM / GPRS Tripleband, Dualband (CXG1121TN) and applications. The low insertion loss on transmit means **increased talk time** as the Tx power amplifier can be operated at a lower output level. **On chip logic** reduces component count and **simplifies PCB layout** by allowing direct connection of the switch to digital baseband control lines with **CMOS logic levels**.

This switch is an **SP5T**, one antenna can be routed to either of the 2 Tx or 3 Rx ports. It requires 3 CMOS control lines (CTL1, CTL2 and Tx ON).

The **Sony GaAs JFET** process is used for low insertion loss.

An evaluation PCB is available.

Features

- Insertion Loss (Tx) 0.5dB typical at 34dBm (GSM 900)
- 3 CMOS compatible Control Lines
- Low second harmonic, -40dBm typical, at 34dBm (GSM 900)
- Small package Size: VSON-16 pin (2.7mm x 3.5mm x 0.9mm)

APPLICATIONS

Triple-band Handsets using combinations of

- GSM900 / DCS1800 / PCS1900
- GPRS
- DECT

STRUCTURE

GaAs J-FET MMIC

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

Truth Table

On Path	CTL1	CTL2	Tx ON
ANT – Tx1 GSM 900	H	Don't Care	H
ANT – Tx2 DCS 1800 & PCS 1900	L	Don't Care	H
ANT – Rx1 GSM 900/DCS1800/PCS 1900	H	L	L
ANT – Rx2 GSM 900/DCS1800/PCS 1900	L	L	L
ANT – Rx3 GSM 900/DCS1800/PCS 1900	L	H	L

Other frequency assignments upon request. See last page for contact details.

Electrical Characteristics

(Tamb= +25ºC)

	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	Tx1,Tx2-Ant	*1		0·5	0.7	dB
		Tx1,Tx2 -Ant	*2		1.0	1.2	dB
		Rx1 -Ant	*3		0.65	0.85	dB
		Rx2 -Ant	*4		1.2	1.4	dB
		Rx3 -Ant	*5		1.2	1.4	dB
Isolation	ISO.	Ant-Tx1,Tx2	*3	18	20		dB
			*4, *5	14	16		dB
		Tx-Rx1,Rx2,Rx3	*1	23	25		dB
		Tx-Rx1,Rx2,Rx3	*2	18	20		dB
VSWR	VSWR				1.2		
Harmonics***	2fo	Tx1,Tx2-Ant	*1, *2		-40	-36	dBm
(see note below)	3fo				-34	-30	dBm
P_{1dB} Compression Input Power	P_{1dB}	Tx1,Tx2-Ant	*1, *2		36		dBm
Control Current	Ictl		Vctl = 3.0 V		80	120	µ A
Supply Current for Tx and Rx modes	I_{Tx}/ I_{Rx}		Vdd = 3.3V		0.3	1	mA

Electrical Characteristics are measured with all RF ports terminated in 50 Ohms.

***** Harmonics measured with Tx inputs harmonically matched. We recommend the use of harmonic matching to ensure optimum performance.**

* 1 Power incident on GSM Tx, Pin =34dBm, 880 to 915 MHz,Vdd=3.3V, GSM Tx enabled

* 2 Power incident on DCS/PCS Tx, Pin =32dBm, 1710 to 1910 MHz, Vdd=3.3V, DCS/PCS Tx enabled

* 3 Power incident on Ant, Pin =10dBm, 925 to 960 MHz, Vdd=3.3V, GSM Rx enabled

* 4 Power incident on Ant, Pin = 10dBm, 1805 to 1880 MHz, Vdd=3.3V, DCS Rx enabled

* 5 Power incident on Ant, Pin =10dBm, 1930 to 1990 MHz,Vdd=3.3V, PCS Rx enabled

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

Supply voltage value (Vdd):

Mode	Minimum	Typical	Maximum
GSM/DCS Tx	3.0V	3.3V	3.5V
GSM/DCS/PCS Rx	2.7V	3.0V	3.5V

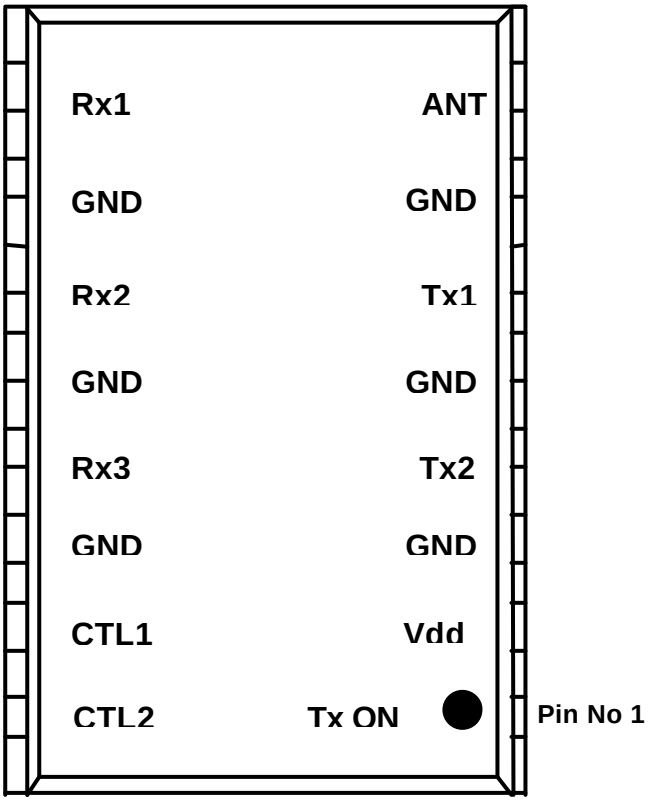
CMOS logic value:

	Minimum	Typical	Maximum
High	2.4V	2.8V	3.2V
Low	0V		0.4V

Absolute Maximum Ratings (Ta = 25°C)

- Bias Voltage Vdd 7V
- Control Voltage Vctl 5V
- Operating Temperature -20°C to +80°C

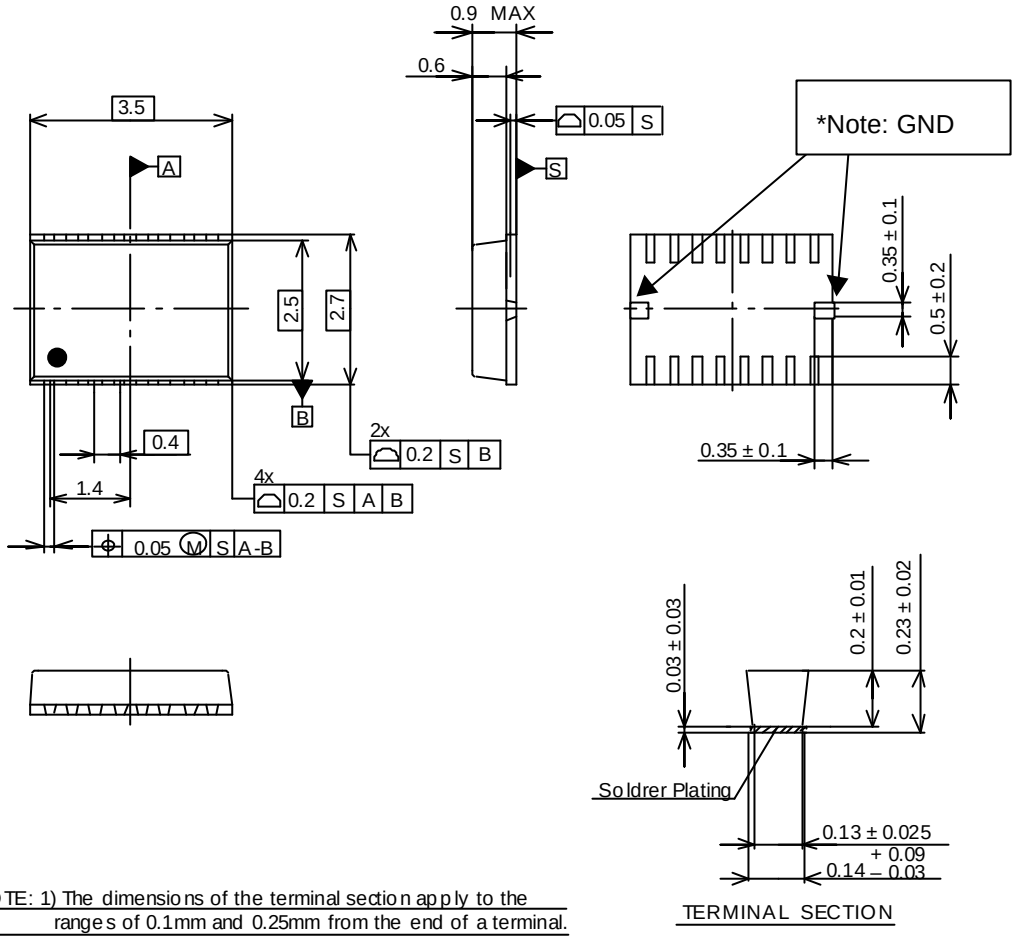
Pin Out



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

Package Outline Drawing

16PIN VSON(PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

TERMINAL SECTION

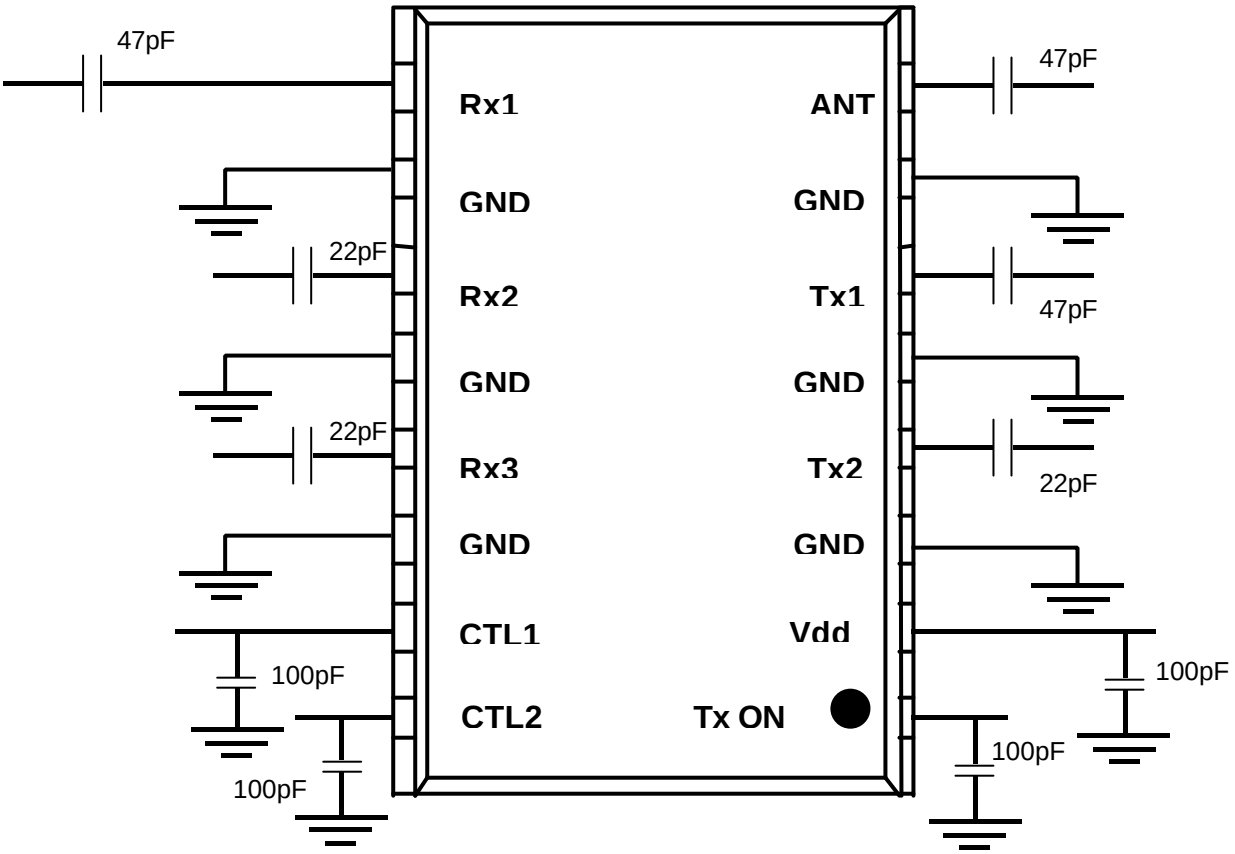
SONY CODE	VSON-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

DC Blocking Capacitors and Decoupling Capacitors



Note: Capacitors are required on all RF ports for DC blocking (22pF – 47pF). Decoupling capacitors are required on Vdd and on control lines.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

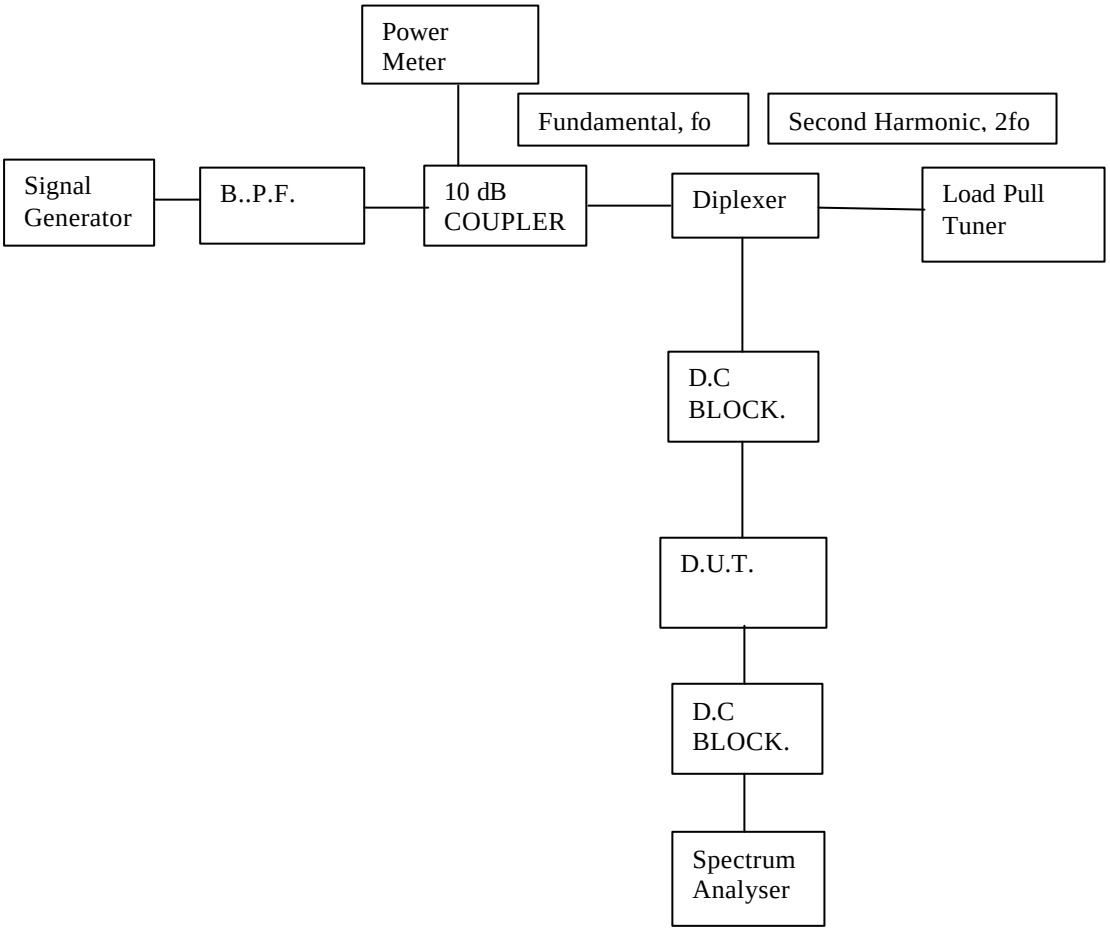
Application Note 1

Impedance Matching for Harmonic Minimisation

This note outlines the method used to find the source impedance to present to a transmit port at the second harmonic frequency (2fo) to reduce the second harmonic level at the antenna.

This should be carried out for a set of devices that represent the process variants. This way a compromise can be found that suits all variants.

The necessary equipment is shown immediately below.



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

The device should be mounted on a PCB with 50Ω tracks running from all RF pins to SMA connectors on the PCB edge (DUT). All ports should be externally DC blocked and unused ports should be terminated in 50Ω. All measurements should be performed at the incident powers for which the harmonic levels are specified in this document.

The 2nd Harmonic level at the Antenna Port is measured using the Spectrum Analyser and the Vertical and Horizontal position of the Load Pull Stub adjusted such that this level is minimised.

The device should then be removed from the board and an SMA connector mounted such that the source impedance seen by the transmit port at 2fo can be measured using a VNA.

Measurements should be de-embedded to the end of the SMA centre pin.

A network should then be designed to match the impedance of the low pass filter (LPF), which usually comes in front of the device, to the 2fo source impedance that gives sufficiently reduced 2fo levels for all devices measured.

The network should be designed to maintain a good match and insertion loss at the fundamental frequency.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits

SONY SEMICONDUCTOR AND DEVICES EUROPE SALES OFFICES

Europe

European Design Center:

The Cresent, Jays Close, Basingstoke,

Hampshire, RG22 4DE, United Kingdom

Tel: +44-1256-388883 Fax: +44-1256-388705

Email : thomas.eichhorst@sde.eu.sony.com

US, Canada

SONY Electronics Inc.

16450 West Bernardo Drive / MZ5100

San Diego, California 92127-1804

Tel: +1-858-942-5193 Fax: +1-858-942-9197

Email : nobuyasu.matsuoka@am.sony.com

Others

Semiconductor & Network Company

Gate City Osaki East Tower Osaki East Tec.

1-11-1 Osaki Shinagawa-ku, Tokyo, 141-0032 Japan

Tel: +81-3-5435-3522 Fax: +81-3-5435-3586

Email: seiji.yagawa@jp.sony.com

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits