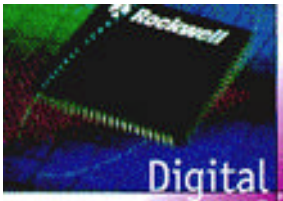

Digital infotainment

August 27, 1998

Bt878/879

Literature Affected: D879DSA
Product Affected: Bt878/9, Rev. D (25878-12ES1, 25879-12ES1, 25878-12 and 25879-12)

errata sheet

DELIVERING INFORMATION AND ENTERTAINMENT TO THE PC AND TV

The following errata apply to the Bt878/879 Revision D part numbers 25878-12ES1, 25879-12ES1, 25878-12 and 25879-12, as related to the Bt878/9 datasheet, D879DSA, dated March 1998. In addition, some updated information is now available. All previous revisions of this datasheet also contain these errors. This errata supercedes all previous erratas for the literature and parts listed above. Please contact your local Field Applications Engineer to ensure you are working from the latest errata available for the Bt878 or Bt879.

1. On page 2 the ordering information incorrectly states the following:

Model Number	it should state	Model Number
Bt878KPF		Bt878KHF
Bt879KPF		Bt879KHF

2. On page 79 of the Bt878/Bt879 datasheet, it erroneously states the following:

   "In addition to the 24 I/O bits, the GPIO port includes an interrupt pin, and a write enable pin. The GPINTR signal sets the bit in the interrupt register and causes an interrupt condition to occur."

It should state the following:

"The GPIO Port supports a GPIO interrupt. This signal is shared with the GPIO[8]. If this pin is to be used as a data input or output in any GPIO mode, the GPIO interrupt **must** be masked in the Interrupt Mask Register. Failure to do so could result in the part self-interrupting. If this pin is to be used as an interrupt input in the GPIO normal mode, the corresponding GPIO Output Enable Control Register bit must be set as an input (logical 0)."

There is no GPIO write enable pin on the Bt878/Bt879.

3. The Video Timing Register Table on pg. 122 incorrectly states the HSFMT. It should state the following:

   HSFMT [7:6] 00 = 64

   01 = 48

   10 = 32

   11 = 16

4. The Color Format Register Table on pg. 125 incorrectly lists YUV12 on the YCrCb 4:1:1 line. The YUV12 color format should be listed on the 4:2:2 planar line.

5. The Memory Mapped Location 0x0B0—VTOTAL_LO table description on page 124 is incorrect.

The VTOTAL _LO description is the following:

> The least significant byte of the 10 bit VTOTAL register, which sets the expected number of horizontal video lines to
>
> VTOTAL_LO = (# of horizontal video lines / frame)–1

6. The Memory Mapped Location 0x0B4—VTOTAL_HI table description on page 125 is incorrect.

The VTOTAL _HI description is the following:

> The most significant 2 bits of the 10 bit VTOTAL register, which sets the expected number of horizontal lines to
>
> VTOTAL_HI = (# of horizontal video lines / frame)–1

7. The DC characteristics defined in Table 22 on page 151 is incorrectly stated in the datasheet. The datasheet currently states the following:

   "GPIO Output Low Voltage (IOL= 8.0mA)"

   It should state the following:

   "GPIO Output Low Voltage (IOL= 6.0mA)"

8. The JTAG Timing Parameter, Table 26 on Page 153 has been updated. Each timing parameter should state the following:

TMS, TDI Setup Time	Typ=2
TMS, TDI Hold Time	Typ=2
TCK Asserted to TDO Valid	Typ=15
TCK Asserted to TDO Driven	Typ=14
TCK Negated to TDO Three-stated	Typ=85

9. The Power Supply Current Parameters, Table 25 on page 153 are the following:

   VAA=VDD=5.0V, Fs_2 = 28.64 MHz, T=25°C Typ=210

   VAA=VDD=5.25V, Fs_2= 35.47 MHz, T=70°C Max=320

   VAA=VDD=5.25V, Fs_2= 35.47 MHz, T= 0°C Max=330

10. The Supply Current, Power Down Parameter, Table 25 on page 153 should be Typ=90

11. On page 103, 141 and 147 the datasheet incorrectly states the PCI Configuration Header Location and Subsystem Vendor ID address as 0x20.

It should state the following:

PCI Configuration Header Location and Subsystem Vendor ID as 0x2C.

If you have any questions concerning this errata, please contact your local Rockwell Field Applications Engineer.