AUTODIRECTIONAL BUS TRANSCEIVER 8X41

DESIGN FEATURES

- **Intelligent bidirectional bus repeater with self-generating or external control**
- **Eight independent channels**
- **Open-collector outputs (meets DEC UNIBUS* specifications)**
- **TTL compatible**
- **High speed (30-nanoseconds max)**
- **Expandable to any number of bits**
- **High input impedance for every operating value of V_{CC}**
- **Low input current (less than 100-microamperes); high output current (up to 70-milliamperes)**
- **0.6 in. 24-pin DIP**
- **+5V supply**

USE AND APPLICATION

- **Minicomputers**
- **Microcomputers MOS/Bipolar**
- **Communications**
- **Signal buffer**
- **Bus fan-out extensions**
- **Distributed processing**
- **Bidirectional bus connector/isolator**

PRODUCT DESCRIPTION

The Signetics 8X41 Autodirectional Bus Transceiver is a general purpose asynchronous device ideal for system bus expansion applications. The 8X41 consists of eight data channels, each with one pair of terminals (A_i and B_i); each data channel can be operated independently.

The device requires no external controls since all intelligence is internally generated; thus, operation of the device is completely autonomous. The first logic low signal that occurs on one channel terminal (A_i or B_i) will be repeated on the corresponding terminal (B_i or A_i) of the same channel.

The 8X41 is designed for use in open-collector bus systems where high speed and low-current inputs/high-current outputs are required. In system configurations, the discrete capabilities of the bus transceiver can be expanded by parallel connection to service any number of bits. To provide reliable operation and integrity of data transfers, all channels are disabled by an on-chip power monitor whenever V_{CC} falls below approximately 4V.

FUNCTIONAL OPERATION

The 8X41 (Figure 1) consists of eight functionally independent yet logically identical channels. Each channel consists of two bus terminals (A_i and B_i); each terminal is internally connected to an open-collector driver and a high-impedance receiver. The monitoring state of each channel is defined when both terminals (A_i and B_i) are "high"; in this state, the internal logic of the 8X41 continually examines the A and B bus signals to determine signal direction—A_i to B_i or B_i to A_i. A low signal occurring at either of the two terminals causes the open-collector driver on the opposite terminal to follow suit; hence, the signal is repeated by the 8X41. For each channel, latches L1 and L2 determine signal direction. As shown in the truth table for these latches, there is no transmission of data when both signals are low, however, this condition should never occur during normal system operation.

The internal automatic direction control can be overridden by either or both of the common disable inputs—$\overline{DBA}$ and $\overline{DAB}$. When $\overline{DBA}$ is driven low ($\overline{DAB}$ = high), the B_i to A_i path is interrupted and the device becomes a unidirectional repeater in the A_i to B_i direction only. With these conditions reversed ($\overline{DAB}$ = low and $\overline{DBA}$ = high), the A_i to B_i path is interrupted and the chip functions as a unidirectional repeater in the B_i to A_i direction. When both control signals are low, data passage is inhibited in both directions. Refer to the I/O truth table for all possible input/output conditions.

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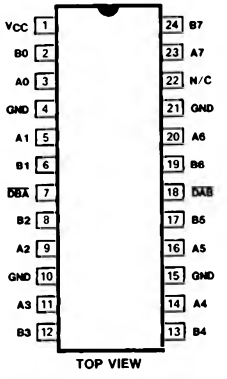
8X41 PACKAGE/PIN DESIGNATIONS

N PACKAGE



TOP VIEW

ORDER NUMBER

N8X41N

PIN NO.	IDENTIFIER	FUNCTION
1	V_{CC}	+5V power
3, 5, 9, 11, 14, 16, 20, and 23	A_0-A_7	A-bus input/output
2, 6, 8, 12, 13, 17, 19, and 24	B_0-B_7	B-bus input/output
4, 10, 15, and 21	GND	Circuit ground
7 & 18	$\overline{DBA}$ & $\overline{DAB}$	Input/output control
22	N/C	No connection

AUTODIRECTIONAL BUS TRANSCEIVER 8X41

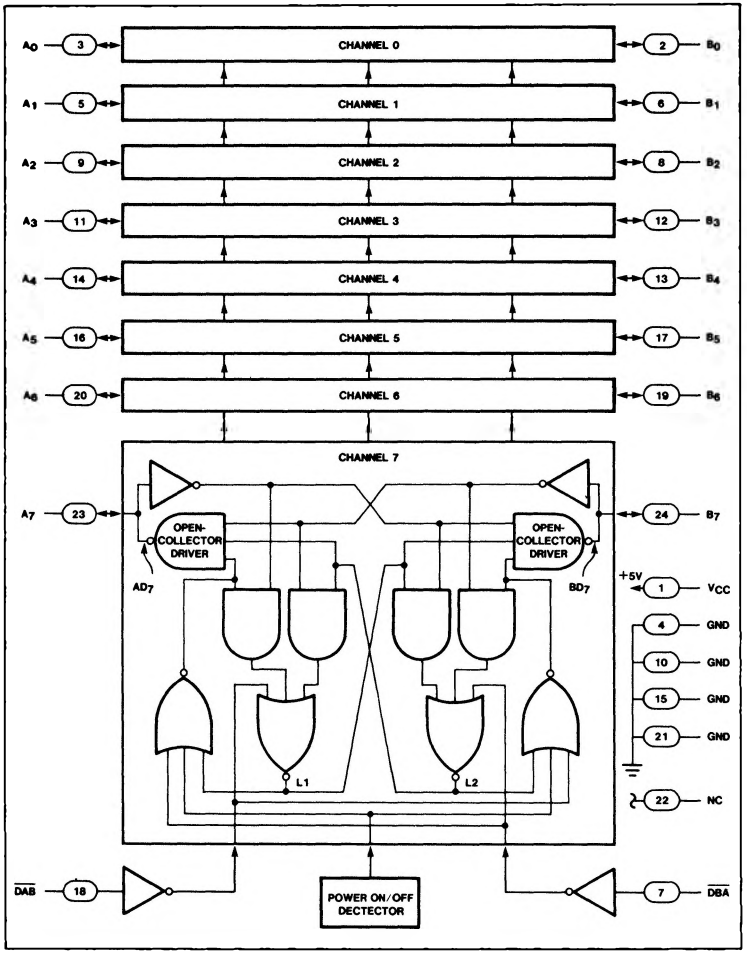


Figure 1. Logic Diagram of 8X41

$\overline{DBA}$	$\overline{DAB}$	FUNCTION
0	0	Data transmission inhibited
0	1	$A_i \rightarrow B_i$
1	0	$A_i \leftarrow B_i$
1	1	$A_i \rightarrow B_i$ $A_i \leftarrow B_i$

i = Channel 0, 1, 2, 3, 4, 5, 6, or 7
$A_i \rightarrow B_i$ = Data transmission from A_i to B_i
$A_i \leftarrow B_i$ = Data transmission from B_i to A_i

TRUTH TABLE FOR INTERNAL LATCHES

LATCHES		DIRECTION OF DATA
L1	L2	
1	1	Monitoring state
1	0	A_i to B_i
0	1	B_i to A_i
0	0	No transmission

INPUT/OUTPUT TRUTH TABLE

EXTERNAL CONTROLS		INPUT SIGNALS		OUTPUT DRIVER SIGNALS	
$\overline{DAB}$	$\overline{DBA}$	A_i	B_i	AD_i	BD_i
H	H	L	L	H	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	H	H
H	L	L	L	H	L
H	L	L	H	H	L
H	L	H	L	H	H
H	L	H	H	H	H
L	H	L	L	L	H
L	H	L	H	H	H
L	H	H	L	L	H
L	H	H	H	H	H
L	L	X	X	H	H

Notes
A_i = External signal
AD_i = Output A driver
B_i = External signal
BD_i = Output B driver
X = Don't care

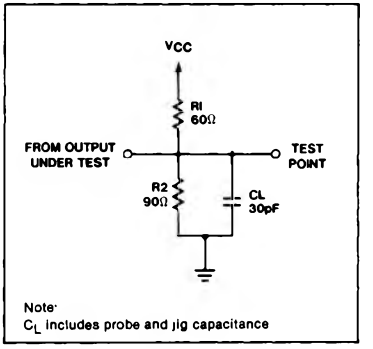
AUTODIRECTIONAL BUS TRANSCEIVER 8X41

DC CHARACTERISTICS V_{CC} = 5V (±5%); T_A = 0°C to 70°C

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{OL}	Bus output low voltage (driver ON)	I_{OL} = 70 mA; V_{CC} = Min			0.5	V
*V_B	Bus input threshold voltage (driver OFF)		1.3		1.7	V
V_{IH} ($\overline{DBA}$, $\overline{DAB}$ only)	High level input voltage		2.0			V
V_{IL} ($\overline{DBA}$, $\overline{DAB}$ only)	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = Min; I_{IL} = −18mA			−1.5	V
V_{PD}	Power ON/OFF detector threshold voltage		3.7		4.35	V
I_{IH} ($\overline{DBA}$, $\overline{DAB}$ only)	High level input current	V_{CC} = Max; V_{IN} = 2.7V			20	μA
I_{IL} ($\overline{DBA}$, $\overline{DAB}$ only)	Low level input current	V_{CC} = Max; V_{IN} = 0.4V			−0.4	mA
I_I	Bus input current (driver OFF)	V_{CC} = Max; V_B = 2.5V*			100	μA
		V_{CC} = Max; V_B = 0V*			−20	μA
I_{OFF}	Bus leakage current (power OFF)	V_{CC} = 0V; V_B = 2.5V*			100	μA
I_{CC}	Supply current	V_{CC} = Max; A_0-A_7 = Low or B_0-B_7 = Low and $\overline{DBA}$ = $\overline{DAB}$ = High		145	180	mA

*V_B = V_{BUS}

LOAD CIRCUIT FOR OUTPUTS



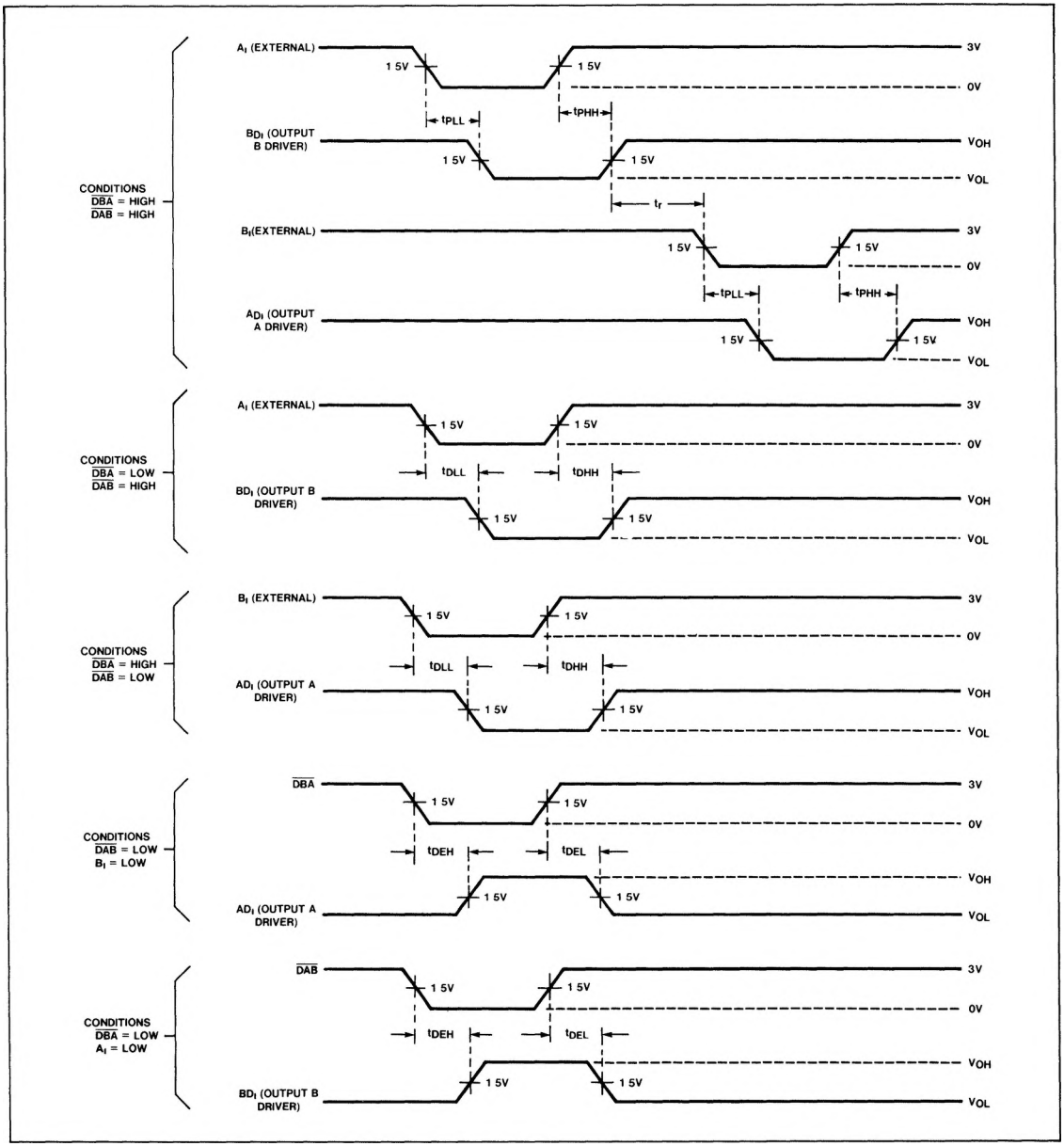
Note:
C_L includes probe and jig capacitance

AC CHARACTERISTICS V_{CC} = 5V (±5%); T_A = 0°C to 70°C

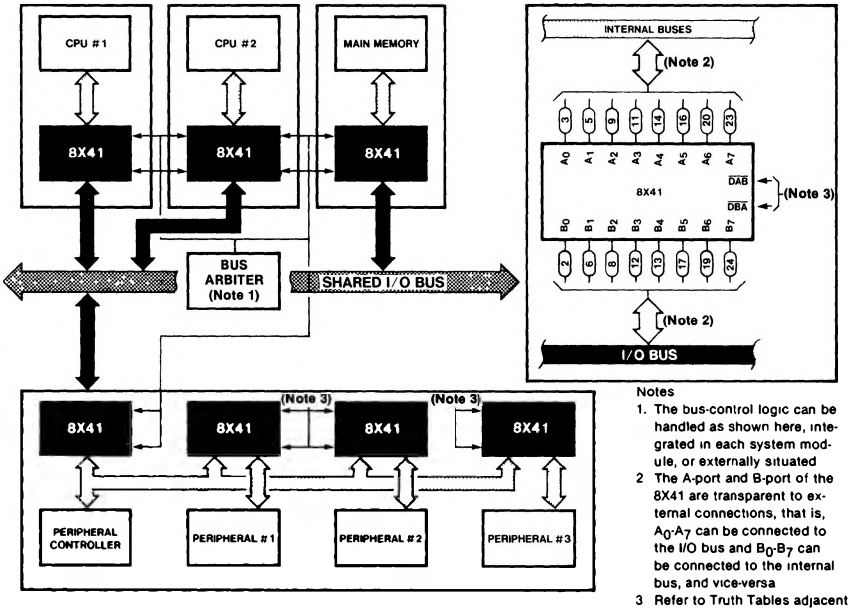
PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS			UNITS
					Min	Typ	Max	
t_{PLL}	Propagation delay	Low A_i Low B_i	Low BD_i Low AD_i	$\overline{DBA}$ = $\overline{DAB}$ = High			30	ns
t_{PHH}	Propagation delay	High A_i High B_i	High BD_i High AD_i	$\overline{DBA}$ = $\overline{DAB}$ = High			30	ns
t_{DHH}	Propagation delay	High A_i	High BD_i	$\overline{DBA}$ = Low; $\overline{DAB}$ = High			25	ns
		High B_i	High AD_i	$\overline{DAB}$ = Low; $\overline{DBA}$ = High			25	ns
t_{DLL}	Propagation delay	Low A_i	Low BD_i	$\overline{DBA}$ = Low; $\overline{DAB}$ = High			25	ns
		Low B_i	Low AD_i	$\overline{DAB}$ = Low; $\overline{DBA}$ = High			25	ns
t_{DEH}	Propagation delay	Low $\overline{DBA}$	High AD_i	$\overline{DAB}$ = Low; B_i = Low			30	ns
t_{DEL}	Propagation delay	High $\overline{DBA}$	Low AD_i	$\overline{DAB}$ = Low; B_i = Low			30	ns
t_{DEH}	Propagation delay	Low $\overline{DAB}$	High BD_i	$\overline{DBA}$ = Low; A_i = Low			30	ns
t_{DEL}	Propagation delay	High $\overline{DAB}$	Low BD_i	$\overline{DBA}$ = Low; A_i = Low			30	ns
t_r	Recovery time (see timing diagram)	—	—	$\overline{DBA}$ = $\overline{DAB}$ = High		20		ns

Notes A_i = External signal AD_i = Output A driver B_i = External signal BD_i = Output B driver

8X41 TIMING DIAGRAM



USING THE 8X41 IN A BUS-SHARED CONFIGURATION



Notes

1. The bus-control logic can be handled as shown here, integrated in each system module, or externally situated
2. The A-port and B-port of the 8X41 are transparent to external connections, that is, A_0-A_7 can be connected to the I/O bus and B_0-B_7 can be connected to the internal bus, and vice-versa
3. Refer to Truth Tables adjacent to Figure 1 for data control capabilities

INTERFACING 8X41 TO IEEE 488 BUS