ADDRESSABLE/BIDIRECTIONAL I/O PORT WITH PARITY 8X374

FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user bus priority for data entry)**
- **Parity generate/check logic with:**
  Odd/Even parity select
  Strobed error flag output
- **Synchronous data input**
- **Programmable MicroController port address**
- **Three-state TTL outputs (for all except parity error flag)**
- **High drive capabilities**
- **Power-up to predetermined state**
- **Directly compatible with 8X305 MicroController**
- **Single +5V supply**
- **0.6 inch, 28-pin DIP**

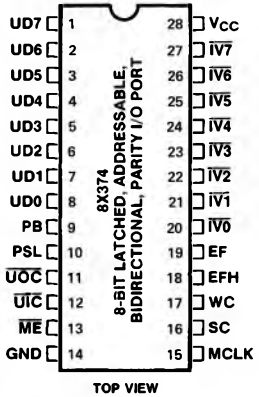
PRODUCT DESCRIPTION

The Signetics 8X374 is an addressable 8-bit I/O Port that features on-chip parity generate/check logic. The 8X374 port is designed for applications that require an 8-bit bidirectional interface element with parity-generate and parity-check capabilities. Typically, the 8X374 is used with the 8X305 MicroController and its associated Interface Vector (IV) bus.

As shown in the logic diagram of Figure 1, the 8X374 consists of eight identical latches, bits 0 through 7. These latches are accessed through either of two 8-bit busses, one connecting to the MicroController (IV bus) and the other to the user system (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time. In such situations, the user bus always has priority. The data latches are transparent, in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output. The data latch in Figure 1 is common to both busses, that is, data traveling from the IV bus to the UD bus, or vice-versa, is latched and applied to the parity generate/check logic. The parity-bit latch is interfaced to the UD bus and latches the parity bit. The user can implement the parity features of the chip by simply selecting odd or even parity via the Parity SeLect (PSL) input pin. When data is output to the UD bus, a parity bit is generated and appended to each byte of data; for incoming data, parity is checked and the result is transmitted to an error-flag latch. The status of the latch (0 = no parity error/1 = parity error) is reflected by the Error Flag (EF) output pin. Operation of the error-flag latch is controlled by the Error Flag Hold (EFH) signal. With EFH low, the operation is transparent; when high the contents of the latch are frozen to avoid false errors while data latches are changing.

8X374 PACKAGE AND PIN DESIGNATIONS

N,F PACKAGE



TOP VIEW

ORDER NUMBERS

N8X374N, N8X374F
S8X374F/883B, S8X374F/883C

Pin No.	Identifier	Function
1-8	UD7-UD0	Three-state bidirectional User Data (UD) bus; UD0 corresponds to $\overline{IV0}$.
9	PB	User port Parity Bit I/O pin.
10	PSL	Parity SeLect input control; even parity = 1 and odd parity = 0.
11	$\overline{UOC}$	User Output Control — active low input to enable data output from UD0-UD7.
12	$\overline{UIC}$	User Input Control — active low input to enable data input from UD0-UD7.
13	$\overline{ME}$	Master Enable — active low input to enable the IV bus for data input, data output, or IV address selection/deselection; UD-bus operations are unaffected.
14	GND	Ground
15	MCLK	Master Clock — active high input from MicroController used to strobe data into the data latches; MCLK also synchronizes IV address selection.
16	SC	Select Command — active high input from MicroController to enable IV address input from the IV bus for device selection.
17	WC	Write Command — active high input from MicroController to enable the writing of data into the data latches from the IV bus, provided $\overline{UIC}$ is not low.
18	EFH	Error Flag Hold signal to control error-flag latch. When low, latch operation is transparent; when high, contents of latch are frozen.
19	EF	Error Flag output; no parity error = 0 parity error = 1.
20-27	$\overline{IV0}$-$\overline{IV7}$	Interface Vector (Input/Output Bus), three-state, bidirectional, MicroController data bus; $\overline{IV0}$ corresponds to UD0.
28	VCC	+5V power supply.

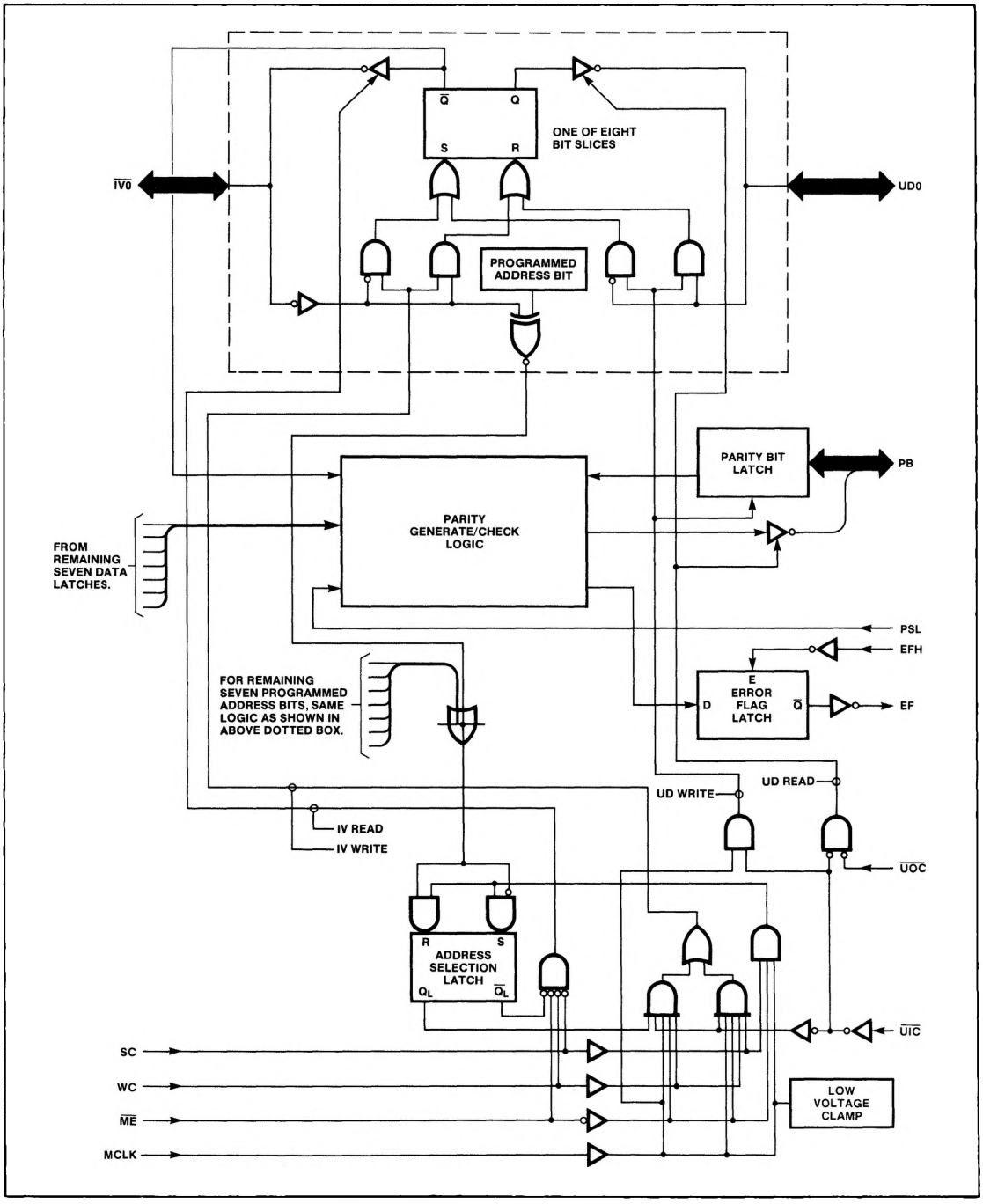


Figure 1. Logic Diagram for 8X374 I/O Port

The 8X374 is available with either preprogrammed addresses (0_{10} to 255_{10}) or unprogrammed; the device can be field-programmed over the same address range as the preprogrammed port. Input/Output operations to the Micro-Controller bus can begin once the 8X374 enabling address has been selected and appropriate control signals from the IV bus are generated. Port selection is implemented by putting the 8X374 address (0_{10} to 255_{10}) on the IV bus. Once selected, the I/O port remains selected until a different port address is put on the bus.

With appropriate control inputs, data is accessible on the UD bus at all times. A Master Enable (ME) input, which is typically connected to the Left Bank (LB) or Right Bank (RB) output of the MicroController, provides the capability of organizing the IV bus into two separate and independent banks of I/O devices.

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus and parity-bit interface are controlled by the UIC and UOC inputs. Data from the UD bus is written synchronously with MCLK, that is with UIC low, information is written into the data latches only when MCLK is high. Output drivers on the UD bus are enabled when UOC is low and UIC is high.

Table 1. INPUT/OUTPUT CONTROL OF UD BUS

			Function of UD Bus	
UIC	UOC	MCLK	8-Bit Data Bus	Parity Bit
H	L	X	Output data	Output parity
L	X	H	Input data	Input parity
L	X	L	Inactive	Inactive
H	H	X	Inactive	Inactive

X = Don't Care

IV Bus Control

Input/Output control of the IV bus is shown in Table 2; this bus is controlled by SC, WC, ME, MCLK and the current state of the internal address selection latch. As shown in Table 2, UIC is required to indicate priority of the UD bus for data input operations. The selection latch in the I/O port stores the result of the most recent IV address selection. The latch is set when the internally preprogrammed address of the port matches the address on the IV bus during an address-selection operation (SC = MCLK = High; ME = WC = Low). The latch is cleared when the two 8-bit address patterns are in disagreement. The IV bus can transfer data only when the selection latch is set. As shown in the APPLICATION DIAGRAM, the 8X305 Left Bank (LB) and Right Bank (RB) outputs can control the ME inputs for two banks of I/O devices, thus, acting as a ninth address bit.

Table 2. INPUT/OUTPUT CONTROL OF IV BUS

ME	SC	WC	MCLK	UIC	Selection Latch	Function of IV Bus
L	L	L	X	X	Set	Output Data
L	L	H	H	H	Set	Input Data
L	H	L	H	X	X	Input Address*
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

X = Don't Care *Selection latch is updated.

Data is written into the data latches of a selected device from the IV bus when WC, MCLK and UIC are all high and ME is low. To prevent data-input conflicts, inputs from the IV bus are inhibited when UIC is low, under all other conditions, the IV and UD busses operate independently. Output drivers on the IV bus of a selected device are enabled when ME, WC, and SC are all low and the address selection latch is set.

Parity Generate/Check Logic

The Parity Bit (PB) pin provides both parity-generate and parity-check capabilities according to user data bus controls. With UIC low (active), a parity check is performed on the input data stream; with UOC low (active) and UIC high, the 8X374 generates the parity-bit for the output data stream. The user can select odd or even parity via the Parity SeLect (PSL) input control, 1 = even parity and 0 = odd parity. As data and parity are input to the data latches and the parity-bit latch from the UD bus and PB line (Figure 1), parity errors (if any) are continuously detected by the parity-check logic. Parity error status enters the error flag latch (if enabled) and appears at the EF output pin. The error latch can be strobed by the Error Flag Hold (EFH) control to latch in valid error status; otherwise, the error flag is transparent to the user. (Note: If the sytem uses less than eight data bits, keeping zeros in unused data latches preserves proper parity operation.)

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: A logic "1" in MicroController software corresponds to a high level on the UD bus even though the IV bus

is inverted.) The 8X374 wakes up with the address selection latch in the unselected state, all data bits latched at the "logic 1" level (UD bus outputs high if enabled), and the EF output high.

ADDRESS PROGRAMMING AND ADDRESS PROTECT

Programming Procedures

The 8X374 can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level ($\leq$ 0.8 V) inputs on all IV bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level ($\geq$ 2.0 V) input on the corresponding IV pin (a logical "0" to the MicroController), the counterpart UD-bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state, UIC = UOC = ME = V_{CC} and SC = WC = MCLK = 0 V; leave the UD and IV bus pins open.

Table 3. PROGRAMMING SPECIFICATIONS

Parameters	Limits Min.	Typ.	Max.	Units
V_{CCP} — Programming supply voltage:				
Address	8.75	9.0	9.25	V
Protect		0		V
Maximum Time V_{CC} > 5.25 V			1.0	sec
Programming voltage:				
Address	8.75	9.0	9.25	V
Protect	8 75		9.25	V
Programming current:				
Address			5	mA
Protect			50	mA
t_r — Programming pulse rise time:				
Address	10		100	μs
Protect	10		100	μs
t_W — Programming pulse width	0.5		1.0	ms

Step 2: Increase V_{CC} to V_{CCP}.

Step 3: After V_{CC} has stabilized, apply a single programming pulse (Figure 2) to the user-bus bit that corresponds to the desired high-level IV address bit. The I/O port is programmed from the user bus (UD0-UD7) for addressing from the MicroController bus (IV0-IV7).

Step 4: Return V_{CC} to 0 volts. (Note: If the programming of all address bits is completed in less than one second, V_{CC} can remain at V_{CCP} for the required interval of time.)

Step 5: Step 1 through Step 3 are applicable to the programming of each address bit that requires a high-level IV match.

Step 6: To verify that the address is properly programmed, return V_{CC} to +5 V and set IV0-IV7 to the desired address pattern (inverted). Set ME = WC = Low and SC = MCLK = High to select the programmed I/O port. With ME = SC = Low and WC = MCLK = High, write an 8-bit pattern to the port. If there are no programming errors, the transmitted data pattern will appear inverted at UD0-UD7 of selected port.

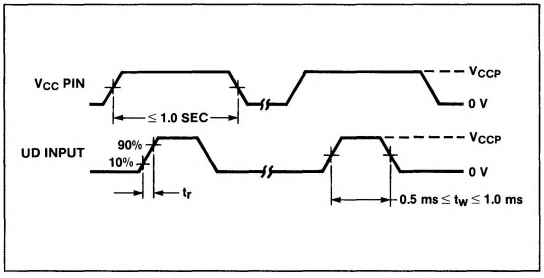


Figure 2. Address Programming Pulse

ADDRESS PROTECT

After programming the I/O Port, optional steps can be taken to isolate the fuse circuits and to make these circuits permanently immune to further change.

Step 1: Set V_{CC} and all control inputs to 0 volts, V_{CC} = UIC = UOC = ME = SC = WC = MCLK = 0V, IV0-IV7 = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user-bus bit (UD0-UD7). Refer to Table 3 for min/max specifications pertaining to voltage and current.

Step 3: Verify that the address circuits for each bit are isolated by applying V_{CCP}, in turn, to each user-bus pin (UD0-UD7) and measuring less than 200 microamperes of input current. (Note: Setup conditions are the same as those in Step 1.)

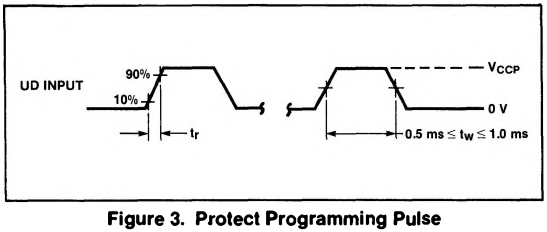


Figure 3. Protect Programming Pulse

ABSOLUTE MAXIMUM RATINGS

	Parameter	Rating	Unit
V_{CC}	Power supply voltage[3]	+7	V DC
V_{IN}	Input voltage[3]	+5.5	V DC
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

COMMERCIAL: V_{CC} = 5 V (±5%); $T_A \geq 0°C$
$T_A \leq 70°C$
MILITARY: V_{CC} = 5 V (±10%); $T_A \geq -55°C$
$T_C \leq 125°C$

Parameter		Test Conditions	Limits (Commercial)			Limits (Military)			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{CL}	Input Clamp Voltage	V_{CC} = Min; I_I = -10 mA			-1.5			-1.5	V
I_{IH}	High Level Input Current[1]	V_{CC} = Max; V_{IH} = 2.7 V		5.0	100		5.0	250	µA
I_{IL}	Low Level Input Current[1]	V_{CC} = Max; V_{IL} = 0.5 V		-350	-550		-350	-550	µA
V_{OL}	Low Level Output Voltage $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Min; I_{OL} = 16 mA			0.55			0.55	V
	User Bus (UD0-UD7) and PB	V_{CC} = Min; I_{OL} = 24 mA			0.55			0.55	V
	EF	V_{CC} = Min; I_{OL} = 8 mA			0.55			0.55	V
V_{OH}	High Level Output Voltage EF	V_{CC} = Min; I_{OH} = -1 mA	2.4			2.4			V
	Others	V_{CC} = Min; I_{OH} = -3.2 mA	2.4			2.4			V
I_{OS}	Short Circuit Output Current[2] $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Max	-20			-20			mA
	UD Bus (UD0-UD7)	V_{CC} = Max	-10			-10			mA
I_{CC}	Supply Current	V_{CC} = Max; $\overline{ME}$ = $\overline{UOC}$ = V_{CC}		90	150		90	160	mA

Notes:
1. The input current includes the high-Z leakage current of the output drivers ($\overline{IV0}$-$\overline{IV7}$, UD0-UD7) on the data lines.
2. Only one output may be shorted at a time for testing purposes.
3. These limits do not apply during address programming.

AC ELECTRICAL CHARACTERISTICS

COMMERCIAL: V_{CC} = 5 V (±5%); $T_A \geq 0°C$, $T_A \leq 70°C$
MILITARY: V_{CC} = 5 V (±10%); $T_A \geq -55°C$, $T_C \leq 125°C$
LOADING: See TEST LOADING CIRCUITS

Parameter		References From	References To	Test Conditions[1]	Limits (Commercial) Min	Typ	Max	Limits (Military) Min	Typ	Max	Unit
Pulse Widths:											
t_{W1}	Clock High	↑MCLK	↓MCLK		35			35			ns
t_{W2}	User Input Control	↑$\overline{UIC}$	↓$\overline{UIC}$	MCLK = High	35			35			ns
Propagation Delays:											
t_{PD1}	UD Propagation Delay	UD	$\overline{IV}$	MCLK = High SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			40			40	ns
t_{PD2}	UD Clock Delay	↑MCLK	$\overline{IV}$	UD = Stable; SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			50			50	ns
t_{PD3}	UD Input Delay	↑$\overline{UIC}$	$\overline{IV}$	UD = Stable; MCLK = High; SC = WC = $\overline{ME}$ = Low			50			50	ns
t_{PD4}	$\overline{IV}$ Data Propagation Delay	$\overline{IV}$	UD	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME}$ = $\overline{UOC}$ = SC = Low			45			45	ns
t_{PD5}	$\overline{IV}$ Data Clock Delay	↑MCLK	UD	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable, $\overline{ME}$ = $\overline{UOC}$ = SC = Low			55			55	ns
t_{PD6}	Error Flag Propagation Delay	UD, PB	EF	MCLK = High; $\overline{UIC}$ = EFH = Low			55			55	ns
t_{PD7}	Parity Generate Propagation Delay	$\overline{IV}$	PB	MCLK = WC = $\overline{UIC}$ = High; $\overline{UOC}$ = $\overline{ME}$ = Low			55			55	ns
t_{PD8}	Error Flag Strobe Delay[3]	↑EFH	EF				20			20	ns
Output Enable Timing:											
t_{OE1}	UD Output Enable	↑$\overline{UOC}$	UD, PB	$\overline{UIC}$ = High			30			30	ns
t_{OE2}	UD Input Recovery	↑$\overline{UIC}$	UD, PB	$\overline{UOC}$ = Low			30			30	ns
t_{OE3}	$\overline{IV}$ Data Master Enable	↑$\overline{ME}$	$\overline{IV}$	WC = SC = Low			22			25	ns
t_{OE4}	$\overline{IV}$ Data Write Recovery	↑WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns
t_{OE5}	$\overline{IV}$ Data Select Recovery	↑SC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Parameter	References		Test Conditions[1]	Limits (Commercial)			Limits (Military)			Unit
	From	To		Min	Typ	Max	Min	Typ	Max	
Output Disable Timing:										
t_{OD1} UD Output Disable	↓$\overline{UOC}$	UD, PB	$\overline{UIC}$ = High			25			25	ns
t_{OD2} UD Input Override	↓$\overline{UIC}$	UD, PB	$\overline{UOC}$ = Low			30			30	ns
t_{OD3} $\overline{IV}$ Data Master Disable	↓$\overline{ME}$	$\overline{IV}$	WC = SC = Low			20			20	ns
t_{OD4} $\overline{IV}$ Data Write Override	↓WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			20			20	ns
t_{OD5} $\overline{IV}$ Data Select Override	↓SC	$\overline{IV}$	WC = $\overline{ME}$ = Low			20			20	ns
Setup Times:										
t_{S1} UD Clock Setup Time	UD, PB	↑MCLK	$\overline{UIC}$ = Low	15			15			ns
t_{S2} UD Control Setup Time	UD, PB	↓$\overline{UIC}$	MCLK = High	15			15			ns
t_{S3} User Input Control Setup Time	↓$\overline{UIC}$	↑MCLK		25			25			ns
t_{S4} $\overline{IV}$ Data Setup Time	$\overline{IV}$	↑MCLK	WC = High or SC = High; $\overline{ME}$ = Low; $\overline{UIC}$ = High	35			35			ns
t_{S5}[2] $\overline{IV}$ Master Enable Setup Time	↓$\overline{ME}$	↑MCLK	WC = High or SC = High, $\overline{UIC}$ = High	30			30			ns
t_{S6} $\overline{IV}$ Write Control Setup Time	↓WC	↑MCLK	SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High	30			30			ns
t_{S7} $\overline{IV}$ Select Control Setup Time	↓SC	↑MCLK	WC = $\overline{ME}$ = Low	30			30			ns
Hold Times:										
t_{H1} UD Clock Hold Time	↑MCLK	UD, PB	$\overline{UIC}$ = Low	15			15			ns
t_{H2} UD Control Hold Time	↓$\overline{UIC}$	UD, PB	MCLK = High	15			15			ns
t_{H3} User Input Control Hold Time	↑MCLK	↓$\overline{UIC}$		0			0			ns
t_{H4} $\overline{IV}$ Data Hold Time	↑MCLK	$\overline{IV}$	WC = High or SC = High, $\overline{ME}$ = Low, $\overline{UIC}$ = High	5			5			ns
t_{H5}[2] $\overline{IV}$ Master Enable Hold Time	↑MCLK	↑$\overline{ME}$	WC = High or SC = High; $\overline{UIC}$ = High	0			0			ns
t_{H6} $\overline{IV}$ Write Control Hold Time	↑MCLK	↑WC	SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High	0			0			ns
t_{H7} $\overline{IV}$ Select Control Hold Time	↑MCLK	↑SC	WC = $\overline{ME}$ = Low	0			0			ns

Notes:

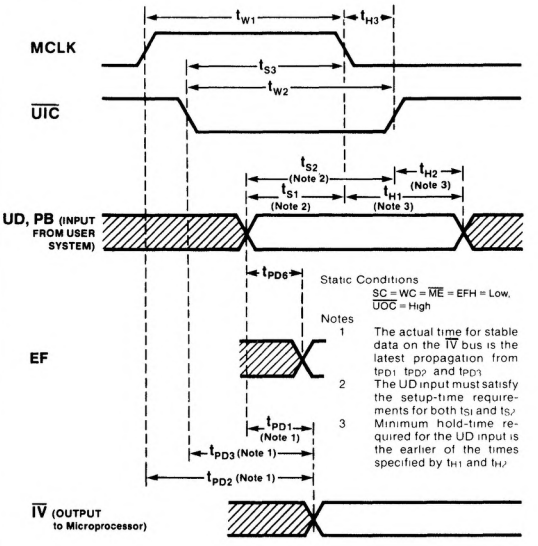
1 All measurements to the $\overline{IV}$ bus assumes the address selection latch is set

2 If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.

3 Parameters are measured by holding $\overline{UIC}$ = High and MCLK = Low and changing the state of the PSL input before each EFH pulse.

TIMING DIAGRAMS

USER DATA INPUT TIMING



Static Conditions
$\overline{SC}$ = WC = $\overline{ME}$ = EFH = Low,
$\overline{UOC}$ = High

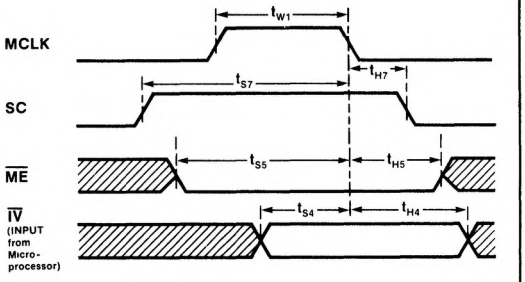
Notes
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from t_{PD1}, t_{PD2} and t_{PD3}.
2. The UD input must satisfy the setup-time requirements for both t_{S1} and t_{S2}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1} and t_{H2}.

Legend:

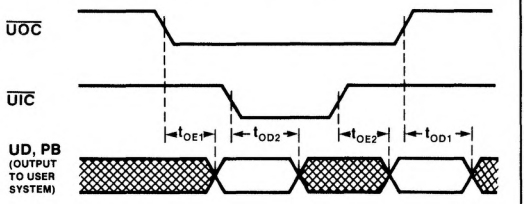
= HIGH-Z STATE

= CHANGING DATA

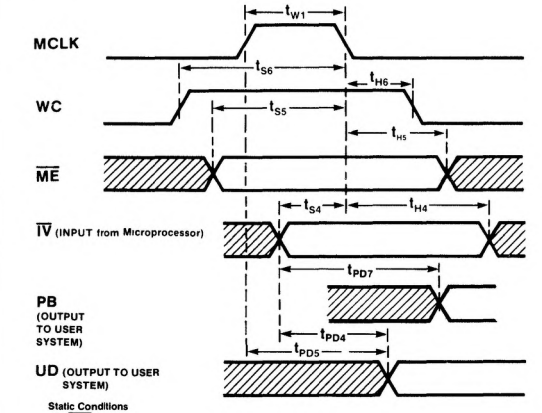
MICROCONTROLLER SELECT CYCLE TIMING



USER DATA OUTPUT ENABLE TIMING

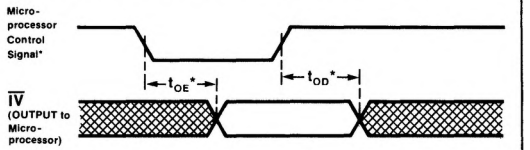


MICROCONTROLLER WRITE CYCLE TIMING



Static Conditions
$\overline{UOC}$ = Low
$\overline{UIC}$ = High

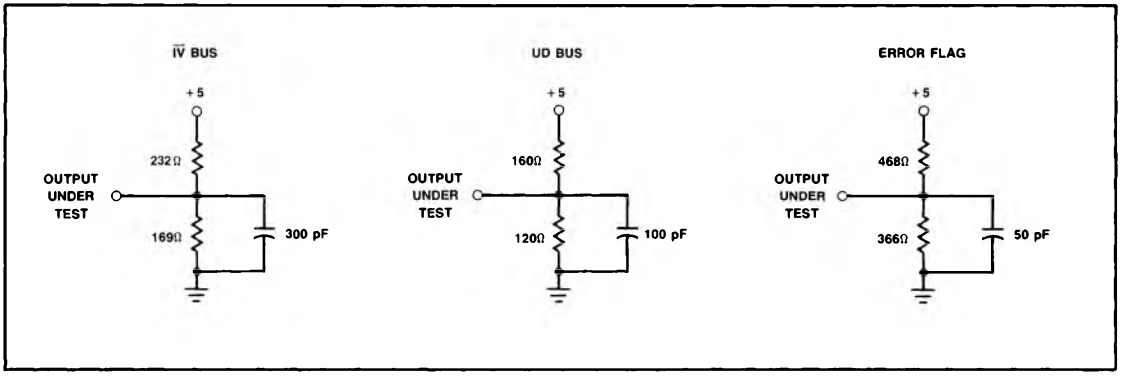
MICROCONTROLLER OUTPUT ENABLE TIMING



*PARAMETER KEY

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
$\overline{ME}$	t_{OE3} t_{OD3}	SC = WC = LOW
WC	t_{OE5} t_{OD5}	SC = $\overline{ME}$ = LOW
SC	t_{OE6} t_{OD6}	WC = $\overline{ME}$ = LOW

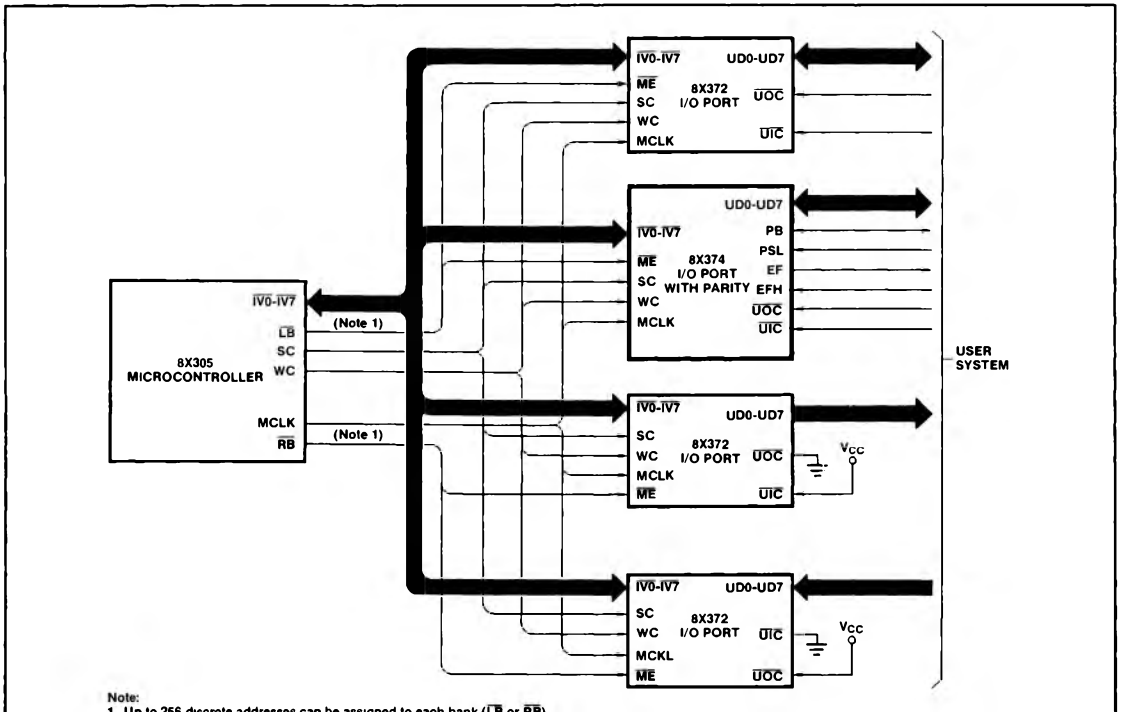
TEST LOADING CIRCUITS



APPLICATIONS

As shown in the following diagram, the 8X374 can be used with other I/O ports to provide a complete range of input/output functions By proper control of the UIC and UOC lines, the user can perform bidirectional data transfers, exercise system control, read system status and, by using the 8X374, implement a bidirectional parity-controlled data stream To use the parity capabilities, the user need only select even or odd parity (PSL = 1 or 0) and connect the PB pin to the system parity bit The EFH and EF pins can be wired according to system requirements

APPLICATIONS DIAGRAM



Note:
1. Up to 256 discrete addresses can be assigned to each bank ($\overline{LB}$ or $\overline{RB}$).