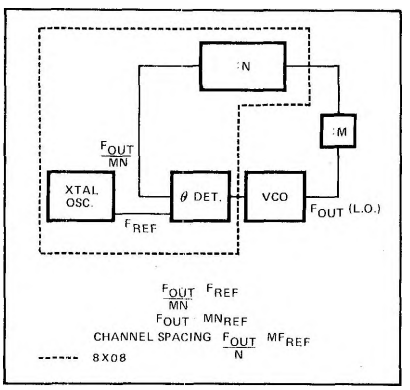
DESCRIPTION

This LSI integrated circuit performs the digital control functions required for generating AM/FM radio frequency local oscillator signals using digital phase locked loop techniques. By the use of low power Schottky and ECL technologies on the same substrate it is possible to operate at 80MHz input frequencies with an average system power of 1.6mW per gate typical.

FEATURES

- **80MHz input frequency**
- **ECL prescaler**
- **LS process**
- **Single 5V supply**
- **Power dissipation—600mW (max)**
- **External components—**
  - **1 crystal**
  - **2 capacitors**

PHASE LOCKED LOOP BLOCK DIAGRAM



PHASE LOCKED LOOP PRINCIPLES

Digital phase locked loops are comprised of 4 basic building blocks: A fixed reference frequency generator (crystal oscillator and divider), a phase comparator, a voltage controlled oscillator (VCO) and a programable counter (÷N).

In cases where very high frequencies must be generated, a fixed prescaler (÷M) is employed to divide the local oscillator frequency down to a frequency compatible with the programmable counter. Fout from the VCO is divided down by the prescaler and programmable counters and compared to the reference frequency by the phase detector. If $\frac{Fout}{MN}$ is not equal to Fref in phase and frequency, the phase detector generates a signal which causes the VCO frequency to increase or decrease until Fref = $\frac{Fout}{MN}$. When this occurs, the local oscillator is essentially as stable as the crystal reference oscillator.

The local oscillator frequency (Fout) is changed by programming a different number into the programmable counter. The distance between discrete frequencies or the channel spacing is determined by the reference frequency.

For the AM/FM circuit, up to 200 channels are possible with selectable channel spacing of 10kHz for AM operation and 2000 channels at 100kHz for FM operation.

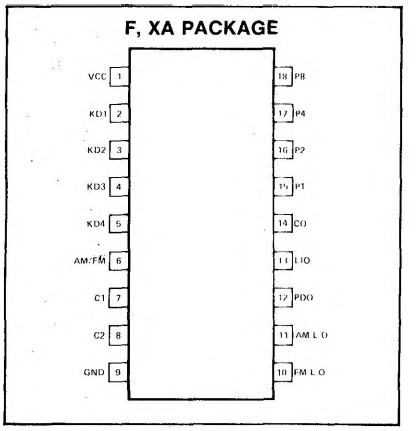
AM/FM Frequency Synthesizer Circuit Description

The frequency synthesizer circuit logic diagram is shown below. Following is a description of each of the major blocks.

Programmable Counter

The programmable counter consists of 3 stages of decade counter plus a divide by 1 or 0 counter to divide by numbers up to 1999. BCD programming data is presented to the dividers in parallel form, one digit at a time. Parallel data is strobed into internal latches via strobe signals; one strobe for each digit. A ÷ 5 80MHz ECL prescaler precedes the programmable counter for FM operation. This prescaler plus an external 160MHz ÷ 2 flip-flop provide a ÷ 10 160MHz prescaler (÷M) function to scale the programmable counter input frequency down to 16MHz maximum. A logic control circuit bypasses the ÷M prescaler and the first decade counter for AM operation. By this technique, the channel spacing is programmable to 10kHz for AM operation and 100kHz for FM operation.

PIN CONFIGURATION



VCO

An externally provided integrator and voltage controlled oscillator must be provided to perform the complete frequency synthesizer function. The integrator converts the pulses that come from the phase detector into a dc signal that controls the output frequency of the voltage controlled oscillator. It is in the integrator part of the circuit that the critical loop constants are determined. The voltage controlled oscillator is normally a LC tuned oscillator with varactor diode tuning that is controlled by the dc signals from the integrator. In this case, two are required, one for the AM band and one for the FM band. The FM oscillator output must be +5V ECL compatible while the AM oscillator must be TTL compatible.

RECOMMENDED OPERATING CONDITIONS

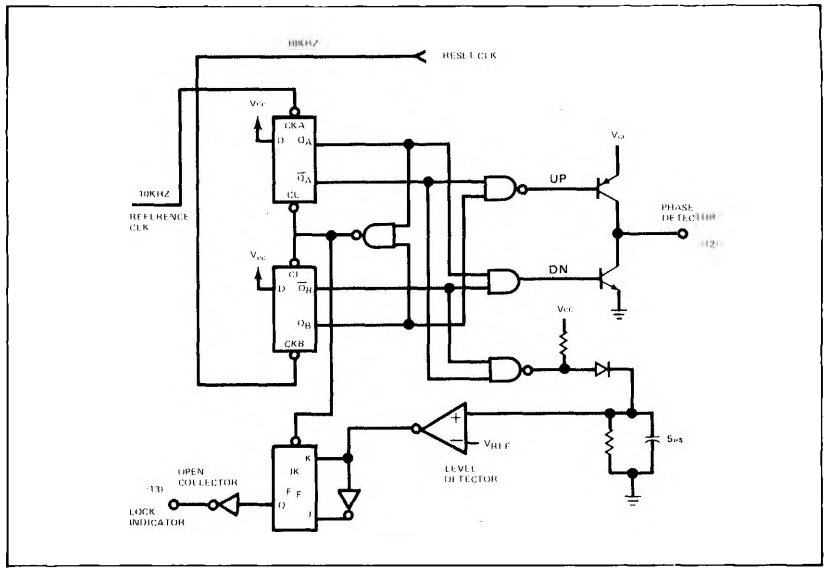
PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_A	Operating free air temperature	-40		+85	°C
V_{CC}	Supply voltage	4.75	5.0	5.25	V
	Max input voltage data, strobe			16	V
	Max AM local oscillator input operating frequency (Pin 11)		20		MHz
	Max FM local oscillator input operating frequency (Pin 10)		100	80	MHz
	Maximum reference frequency oscillator operating frequency		6		MHz

Phase Detector Circuit

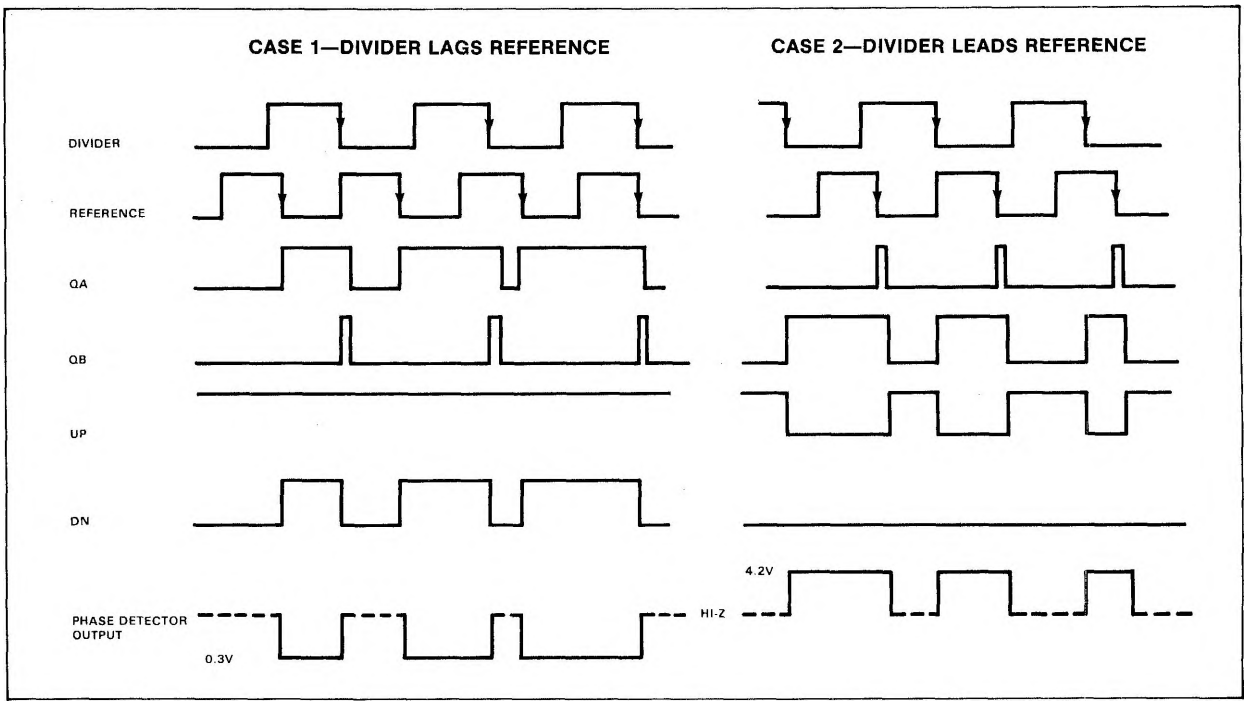
The phase detector is a digital edge-detecting device that provides an output three-state signal that is in a high impedance state when the 2 input signals are equal in phase and/or frequency. The output of the phase detector is a series of pulses that swing from the high impedance state to .3V typical or from the high impedance state to 4.2V typical. If the positive edge of the divider input leads the reference, the pulses will go to 4.2V. If it lags they will go to .3V.

The width of the output pulses is a function of the time between the positive edges (phase) of the 2 signals. An example of the operation of the device is shown where the reference signal is twice the frequency of the divider signal and has a phase lead of 270°. The output pulses are converted to a dc signal by integrating amplifiers causing the output frequency of the voltage controlled oscillator to increase or decrease (increase in this case) until the divider output and the reference output are equal in phase and frequency.

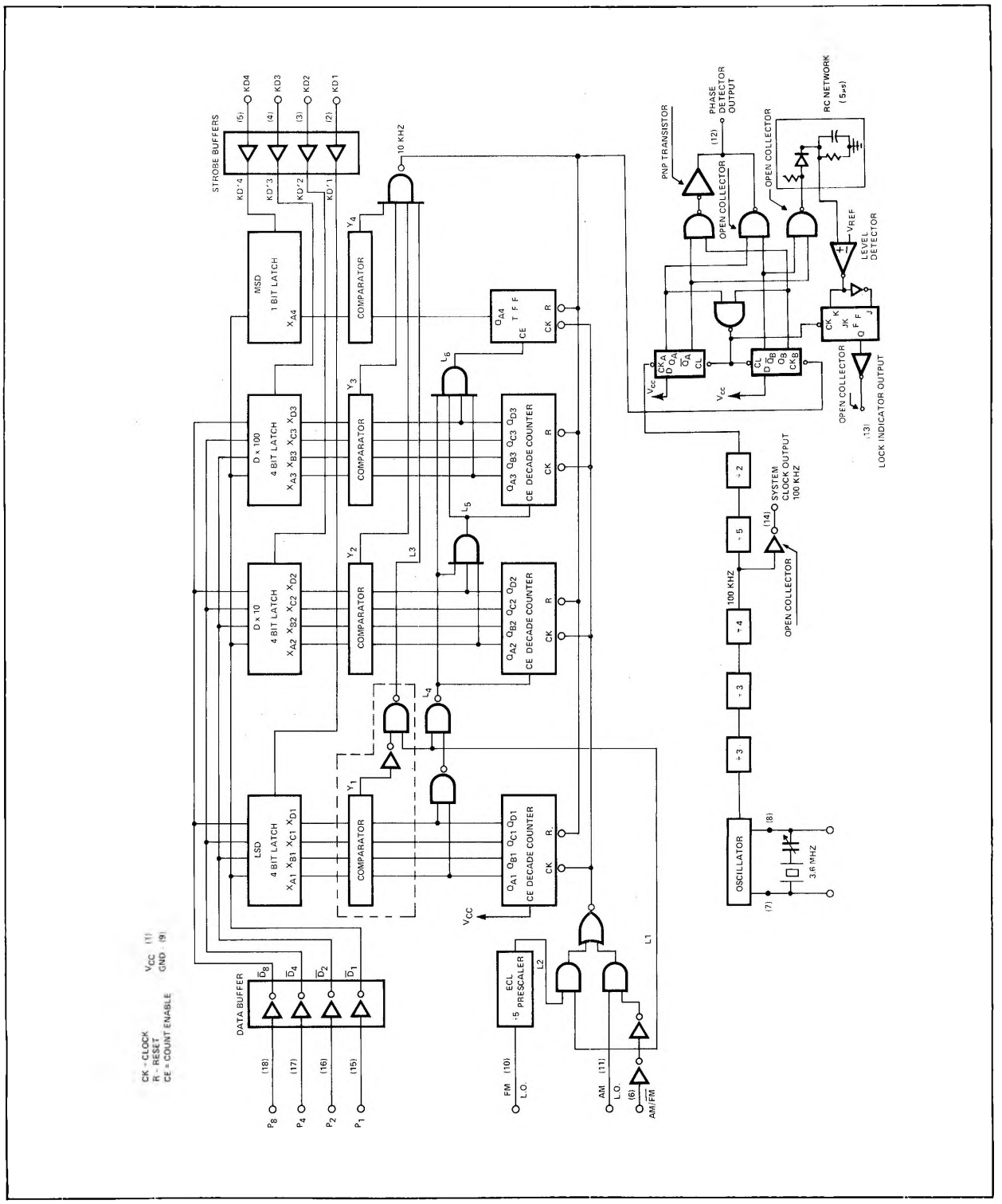
PHASE DETECTOR CIRCUIT



DIVIDER REFERENCE



LOGIC DIAGRAM



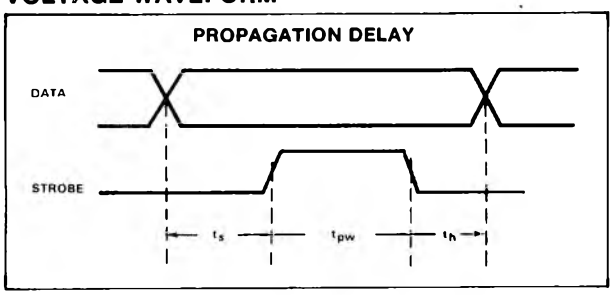
DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{IH}	High level input voltage					
	P, K_D, AM/$\overline{FM}$ inputs		5.25			V
	AM L.O. input		2			V
	FM L.O. input		4.1		5.25	V
V_{IL}	Low level input voltage					
	P, K_D, AM/$\overline{FM}$ inputs				3.75	V
	AM L.O. input				0.8	V
	FM L.O. input				3.3	V
I_{IH}	High level input current					
	P, K_D, AM/$\overline{FM}$ inputs	V_{CC} = max, V_I = 16V			200	μA
		V_{CC} = max, V_I = 5.25V			40	μA
	AM L.O. input					
	(with 5kΩ pullup to V_{CC})	V_{CC} = max, V_I = 5.25V			200	μA
	FM L.O. input	V_{CC} = max, V_I = 5.25V			400	μA
I_{IL}	Low level inputs current					
	P, K_D, AM/$\overline{FM}$ inputs	V_{CC} = max, V_I = 3.75V			-40	μA
	AM L.O. input					
	(with 5kΩ pullup to V_{CC})	V_{CC} = max, V_I = 0.4V	-.7		-1.6	mA
	FM L.O. input	V_{CC} = max, V_I = 0.4V			-40	μA
V_{OL}	Low level output voltage					
	System clock output	V_{CC} = min, I_{OL} = 16mA			0.8	V
	Lock indicator output	V_{CC} = min, I_{OL} = 16mA			0.8	V
	Phase detector output	V_{CC} = min, I_{OL} = 40μA			0.5	V
V_{OH}	High level output voltage					
	Phase detector output	V_{CC} = min, I_{OH} = -40μA	V_{CC} -0.5V			
I_{OL}	High level output current					
	System clock output	V_{CC} = min, V_{OH} = 16V			250	μA
	Lock indicator output	V_{CC} = min, V_{OH} = 16V			250	μA
I_{CC}	Supply current	V_{CC} = max			150	mA

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Strobe pulse width			200	100		ns
	Setup and hold time						ns
t_s	Logic high	Strobe	Data	150			
	Logic low			50			
t_h	Logic high	Strobe	Data	40			
	Logic low			0			

VOLTAGE WAVEFORM



Crystal Oscillator Circuit

In this circuit, the cross-coupled transistor pair form a bistable circuit. The crystal provides positive feedback between the emitters of T_{15} and T_{16} which causes the circuit to oscillate at the crystal frequency.

Recommended Crystal Characteristics

Type	Fundamental Mode Series Resonant
Series resistance	< 100 Ω

CRYSTAL OSCILLATOR CIRCUIT