# 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

## FEATURES

- **Independent port operation (user-port priority for data entry)**
- **User data input available as synchronous (8T32) or as asynchronous (8T36)**
- **User data bus available with three-state (8T32, 8T36)**
- **At power-up, user-port outputs are high and microprocessor-port outputs are high-z; status latch (from address compare) is also cleared at power-up**
- **Three-state TTL outputs for high-drive capabilities**
- **Directly compatible with 8X300 microcontroller**
- **Single +5V supply**

## PRODUCT IDENTITY

**8T32— Three-state, field-programmable (addresses 0-255), synchronous user port.**

**8T36—Three-state, field-programmable (addresses 0-255), asynchronous user port**

## PRODUCT DESCRIPTION

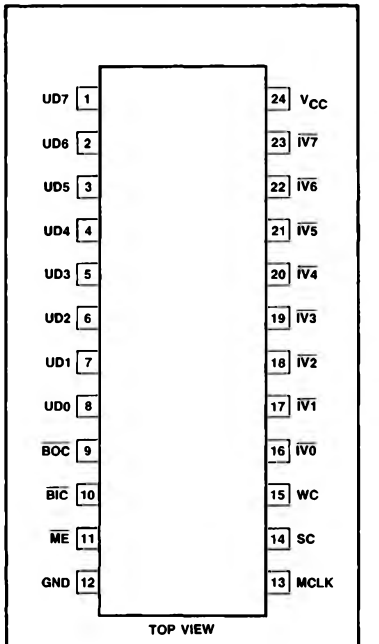
**8T32/8T36.** Each of these I/O Bytes is an addressable and bi-directional register designed for use as an interface element in any system with TTL-compatible buses. (*Note.* Since these I/O Bytes are frequently used with the 8X300 Microcontroller and its associated Interface Vector bus, the 8T32-8T36 family of parts are commonly called IV Bytes.) Each I/O Byte contains eight identical data latches (Bits 0 through 7); the latches are accessed from either of two 8-bit ports—one port connecting to the microprocessor (8X300) and the other port connecting to the user device.

Separate controls are provided for each port and the two ports operate independently, except when both attempt to input data at the same time; in this case, the user port bus has priority.

The address of each I/O Byte is field-programmable and the microprocessor port is accessed when a valid address is received; the user port is accessible at all times. A selected Byte is automatically deselected when the address of another I/O Byte is sensed on the address/data bus. A Master Enable (ME) input is available for use as a ninth address bit, allowing direct access to 512 I/O Bytes without address decoding.

A unique feature of these parts is their ability to start up in a predetermined state. If the clock is maintained at a level of less than 0.8 volts until the power supply reaches 3.5 volts, all bits of the user port will wakeup at a "logic 1" level and those of the microprocessor port will wakeup in the high-impedance state.

## PIN CONFIGURATION




TOP VIEW

**ORDER NUMBERS**

CONTACT LOCAL SALES REPRESENATIVE

A stock of 8T32s and 8T36s with addresses "1" through "10" are maintained in inventory; with a longer lead time, a small quantity of address "11" through "50" are also available.

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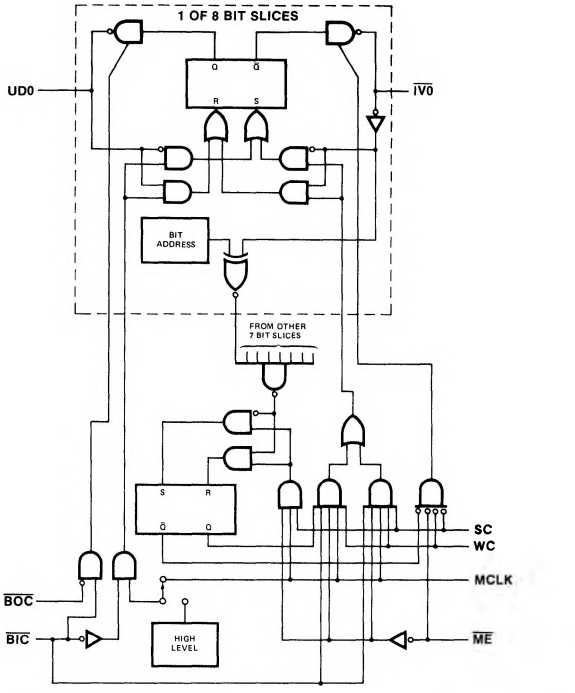
## TYPICAL BLOCK DIAGRAM




*Switch indicates synchronous/asynchronous user write option Switch shown for synchronous version

# 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

## PIN DESCRIPTION

| PIN | SYMBOL | NAME AND FUNCTION | TYPE |
|---|---|---|---|
| 1-8 | UD0-UD7 | User Data I/O Lines Bidirectional data lines to communicate with user's equipment Either tri-state or open collector outputs are available | Active high |
| 16-23 | $\overline{IV0}$-$\overline{IV7}$ | Microprocessor Bus Bidirectional data lines to communicate with controlling digital system (microprocessor) | Active low three-state |
| 10 | $\overline{BIC}$ | Input Control User input to control writing into the I/O Port from the user data lines | Active low |
| 9 | $\overline{BOC}$ | Output Control User input to control reading from the I/O Port onto the user data lines | Active low |
| 11 | $\overline{ME}$ | Master Enable System input to enable or disable all other system inputs and outputs It has no effect on user inputs and outputs | Active low |
| 15 | WC | Write Command. When WC is high and SC is low, I/O Port, if selected, stores contents of $\overline{IV0}$-$\overline{IV7}$ as data. | Active high |
| 14 | SC | Select Command. When SC is high and WC is low, data on $\overline{IV0}$-$\overline{IV7}$ is interpreted as an address I/O Port selects itself if its address is identical to $\mu$P bus data; it de-selects itself otherwise | Active high |
| 13 | MCLK | Master Clock Input to strobe data into the latches See function tables for details | Active high |
| 24 | VCC | 5V power connection | |
| 12 | GND | Ground | |

**Table 1. USER PORT CONTROL FUNCTION**

| $\overline{BIC}$ | $\overline{BOC}$ | MCLK | USER DATA BUS FUNCTION | |
|---|---|---|---|---|
| | | | 8T32 | 8T36 |
| H | L | X | Output Data | Output Data |
| L | X | H | Input Data | Input Data |
| L | X | L | Inactive | Input Data |
| H | H | X | Inactive | Inactive |

H = High Level L = Low Level X = Don't care

**Table 2. MICROPROCESSOR PORT CONTROL FUNCTION**

| $\overline{ME}$ | SC | WC | MCLK | $\overline{BIC}$ | STATUS LATCH | I/O PORT FUNCTION |
|---|---|---|---|---|---|---|
| L | L | L | X | X | SET | Output Data |
| L | L | H | H | H | SET | Input Data |
| L | H | L | H | X | X | Input Address |
| L | H | H | H | L | X | Input Address |
| L | H | H | H | H | X | Input Data and Address |
| L | X | H | L | X | X | Inactive |
| L | H | X | L | X | X | Inactive |
| L | L | H | H | L | X | Inactive |
| L | L | X | X | X | Not Set | Inactive |
| H | X | X | X | X | X | Inactive |

## USER DATA BUS

The activity of the user data bus is controlled by the $\overline{BIC}$ and $\overline{BOC}$ inputs as shown in Table 1.

For the 8T32, user data input is a synchronous function with MCLK. A low level on the $\overline{BIC}$ input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. For the 8T36, user data input is an asynchronous function. A low level on the $\overline{BIC}$ input allows data on the user data bus to be latched regardless of the level of the MCLK input Note that when the 8T36, is used with the 8X300 Microcontroller, care must be taken to insure that the Microprocessor bus is stable when it is being read by the 8X300 Microcontroller.

To avoid conflicts at the Data Latches, input from the Microprocessor Port is inhibited when $\overline{BIC}$ is at a low level. Under all other conditions the two ports operate independently

## MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the $\overline{ME}$, SC, WC, and $\overline{BIC}$ inputs, as well as the state of an internal status latch. $\overline{BIC}$ is included to show user port priority over the microprocessor port for data input.

Each I/O Port's status latch stores the result of the most recent I/O Port select; it is set when the I/O Port's internal address matches the Microprocessor Bus. It is cleared when an address that differs from the internal address is presented on the Microprocessor Bus.

In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the Microprocessor Bus is accepted as data, whether or not the I/O Port was selected. The data is also interpreted as an address. The I/O Port sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

## BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

## AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 5\%$

| PARAMETER | INPUT | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{PD}$ User data delay (Note 1) | UD X | $C_L$ = 50pF | | 25 | 38 | ns |
| | MCLK• | | | 45 | 61 | |
| | $\overline{BIC}$† | | | 40 | 55 | |
| $t_{OE}$ User output enable | $\overline{BOC}$ | $C_L$ = 50pF | 18 | 26 | 47 | ns |
| $t_{OD}$ User output disable | $\overline{BIC}$ | $C_L$ = 50pF | 18 | 28 | 35 | ns |
| | $\overline{BOC}$ | | 16 | 23 | 33 | |
| $t_{PD}$ $\mu$P data delay (Note 1) | $\overline{IV}$ X | $C_L$ = 50pF | | 38 | 53 | ns |
| | MCLK | | | 48 | 61 | |
| $t_{OE}$ $\mu$P output enable | $\overline{ME}$ | $C_L$ = 50pF | 14 | 19 | 25 | ns |
| | SC | | | | | |
| | WC | | | | | |
| $t_{OD}$ $\mu$P output disable | $\overline{ME}$ | $C_L$ = 50pF | 13 | 17 | 32 | ns |
| | SC | | | | | |
| | WC | | | | | |
| $t_W$ Minimum pulse width | MCLK | | 40 | | | ns |
| | $\overline{BIC}$† | | 35 | | | |
| $t_{SETUP}$ Minimum setup time | UD X□ | (Note 2) | 15 | | | ns |
| | $\overline{BIC}$• | | 25 | | | |
| | $\overline{IV}$ X | | 55 | | | |
| | $\overline{ME}$ | | 30 | | | |
| | SC | | 30 | | | |
| | WC | | 30 | | | |
| $t_{HOLD}$ Minimum hold time | UD X□ | (Note 2) | 25 | | | ns |
| | $\overline{BIC}$• | | 10 | | | |
| | $\overline{IV}$ X | | 10 | | | |
| | $\overline{ME}$ | | 5 | | | |
| | SC | | 5 | | | |
| | WC | | 5 | | | |

• Applies for 8T32.
† Applies for 8T36.
□ Times are referenced to MCLK for 8T32, and are referenced to BIC for 8T36.

NOTES:

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. $\overline{BIC}$ setup and hold times are for a user write operation. SC setup and hold times are for I/O Port select operation. $\overline{ME}$ setup and hold times are for both IV write and select operations.

# 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

## DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | 2.0 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | -1.0 | | 8 | V |
| $V_{CL}$ | Input clamp voltage | $I_I = -5mA$ | | | -1.0 | V |
| $I_{IH}$ | High-level input current[1] | $V_{CC} = 5.25V$<br>$V_{IH} = 5.25V$ | | <10 | 100 | μA |
| $I_{IL}$ | Low level input current[1] | $V_{CC} = 5.25V$<br>$V_{IL} = .5V$ | | -350 | -550 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC} = 4.75V$<br>$I_{OL} = 16mA$ | | | .55 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC} = 4.75V$<br>$I_{OH} = -3.2mA$ | 2.4 | | | V |
| $I_{OS}$ | Short-circuit output current[2]<br>UD bus<br>IV bus | <br>$V_{CC} = 4.75V$<br>$V_{CC} = 4.75V$ | <br>10<br>20 | | | <br>mA<br>mA |
| $I_{CC}$ | Supply current | $V_{CC} = 5.25V$ | | 100 | 150 | mA |

NOTES

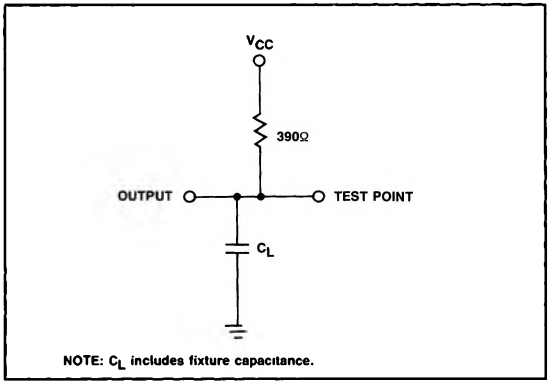
1 The input current includes the Three-state/Open Collector leakage current of the output driver on the data lines
2 Only one output may be shorted at a time
3 These limits do not apply during address programming

**Absolute Maximum Ratings:**

Supply voltage[3] ..... 7V

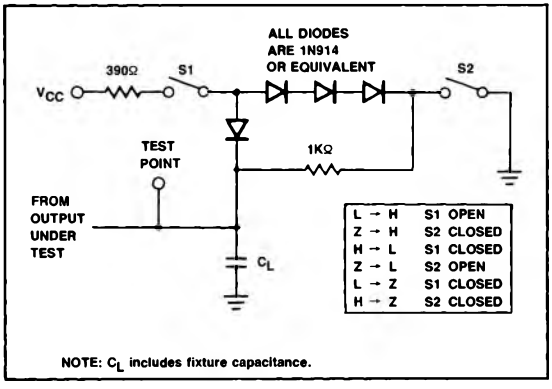
Input voltage[3] ..... 5.5V

## TEST LOAD CIRCUIT (OPEN COLLECTOR OUTPUTS)



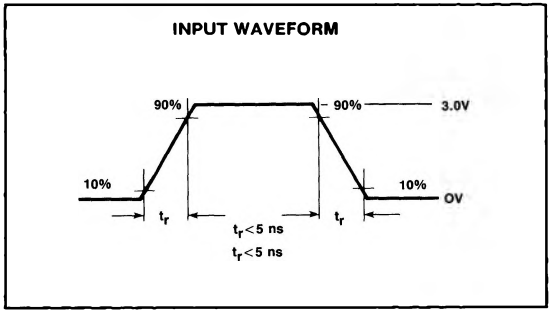

NOTE: $C_L$ includes fixture capacitance.

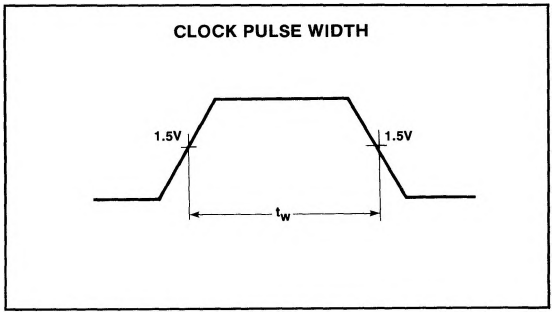
## TEST LOAD CIRCUIT (THREE-STATE OUTPUTS)




NOTE: $C_L$ includes fixture capacitance.

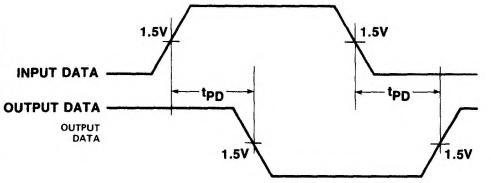
## VOLTAGE WAVEFORMS



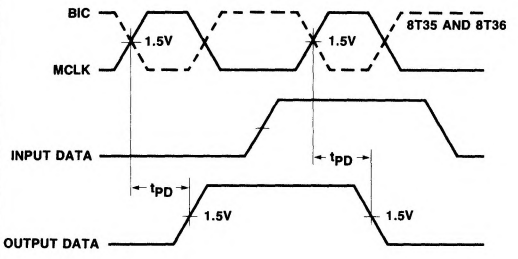



## VOLTAGE WAVEFORMS (Cont'd)

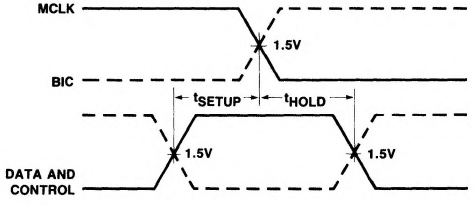
**DATA DELAY TIMES**
Input Data Reference



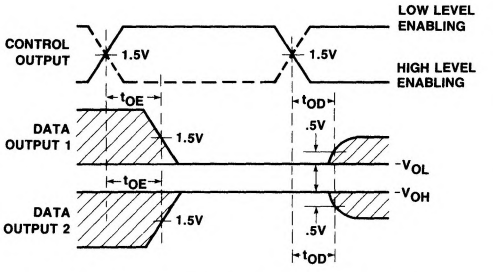

**DATA DELAY TIMES**
Clock Referenced




**SETUP AND HOLD TIMES**




**OUTPUT ENABLE AND DISABLE TIMES**
(Three-State Outputs)




Waveform #1 is for an output with internal conditions such that the output is Low when the three-state driver is enabled. Waveform #2 is for the opposite condition.

# 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

## ADDRESS PROGRAMMING

The I/O Port is manufactured such that an address of all high levels (>2V) on the Microprocessor Bus inputs matches the Port's internal address. To program a bit so a low-level input (<0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state ($\overline{BIC}$ = $\overline{BOC}$ = $\overline{ME}$ = $V_{CC}$, SC = WC = MCLK = GND). Leave all Microprocessor Bus I/O pins open.
2. Raise $V_{CC}$ to 7.75V ± .25V.
3. After $V_{CC}$ has stabilized, apply a single programming pulse to the user data bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited 75mA. Apply the pulse as shown in Figure 1.
4. Return $V_{CC}$ to 0V. (Note 1).
5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Port's status latch ($\overline{IV0}$-$\overline{IV7}$ = desired address, $\overline{ME}$ = WC = L, SC = MCLK = H). If the proper address has been programmed, data presented at the μP bus will appear inverted on the user bus outputs. (Use normal $V_{CC}$ and input voltage for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

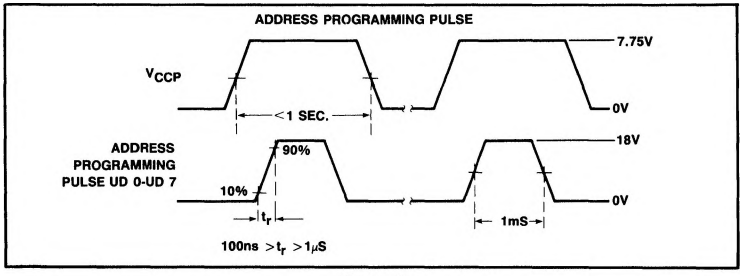



Figure 1

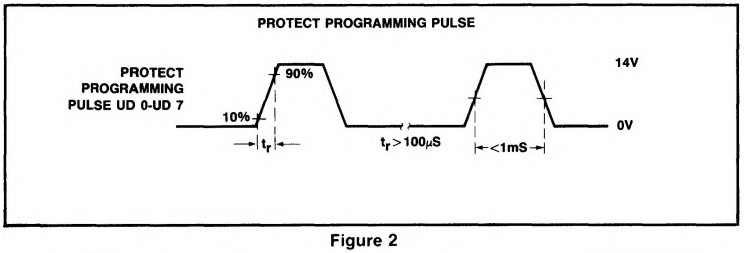



Figure 2

1. Set $V_{CC}$ and all control inputs to 0V. ($V_{CC}$ = $\overline{BIC}$ = $\overline{BOC}$ = $\overline{ME}$ = SC = WC = MCLK = 0V). Leave all Microprocessor Bus I/O pins open.
2. Apply a protect programming pulse to every user data bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Figure 2.
3. Verify that the address circuitry is isolated by applying 7V to each user data bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

## PROGRAMMING SPECIFICATIONS[1]

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CCP}$ | Programming supply voltage | | | | | |
| | Address | | 7.5 | | 8.0 | V |
| | Protect | | | 0 | | V |
| $I_{CCP}$ | Programming supply current | $V_{CCP}$ = 8.0V | | | 250 | mA |
| | Max time $V_{CCP}$>5.25V | | | | 1.0 | s |
| | Programming voltage | | | | | |
| | Address | | 17.5 | | 18.5 | V |
| | Protect | | 13.5 | | 14.0 | V |
| | Programming current | | | | | |
| | Address | | | | 75 | mA |
| | Protect | | | | 150 | mA |
| | Programming pulse rise time | | | | | |
| | Address | | .1 | | 1 | μs |
| | Protect | | 100 | | | μs |
| | Programming pulse width | | .5 | | 1 | ms |

NOTE

1. If all programming can be done in less than 1 second, $V_{CC}$ may remain at 7.75V for the entire programming cycle.

# 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

## APPLICATIONS

Figure 3 shows some of the various ways to use the I/O Port in a system. By controlling the $\overline{BIC}$ and $\overline{BOC}$ lines, the device may be used for the input and output of data, control, and status signals. I/O Port 1 functions bidirectionally for data transfer and I/O Port 2 provides a similar function for discrete status and control lines. I/O Ports 3 and 4 serve as dedicated output and input ports, respectively.

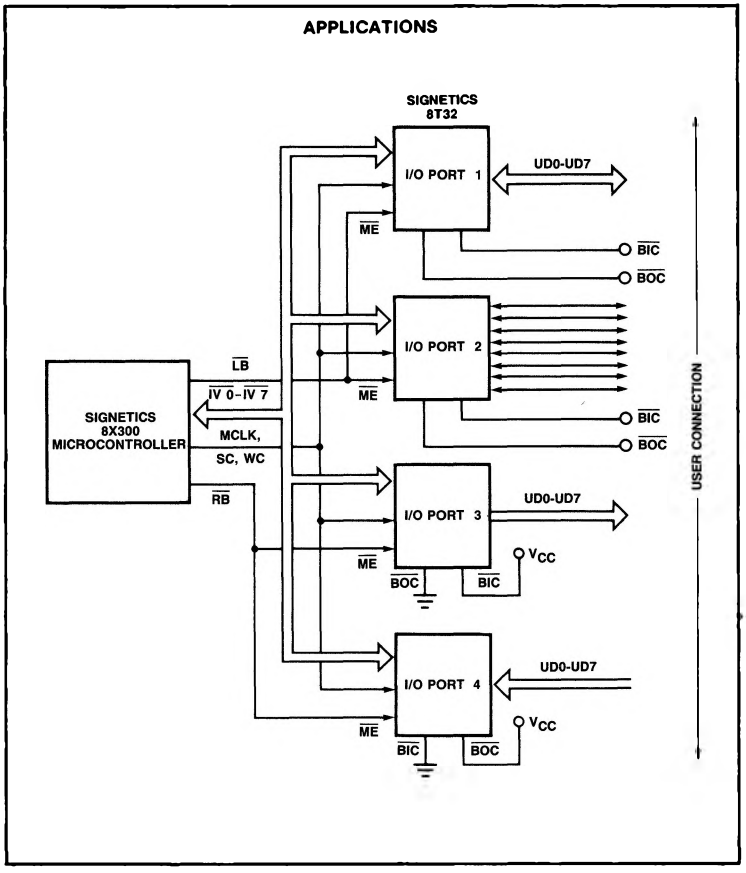



Figure 3