

0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System/360 I/O Interface Specification (File No. S360-19). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

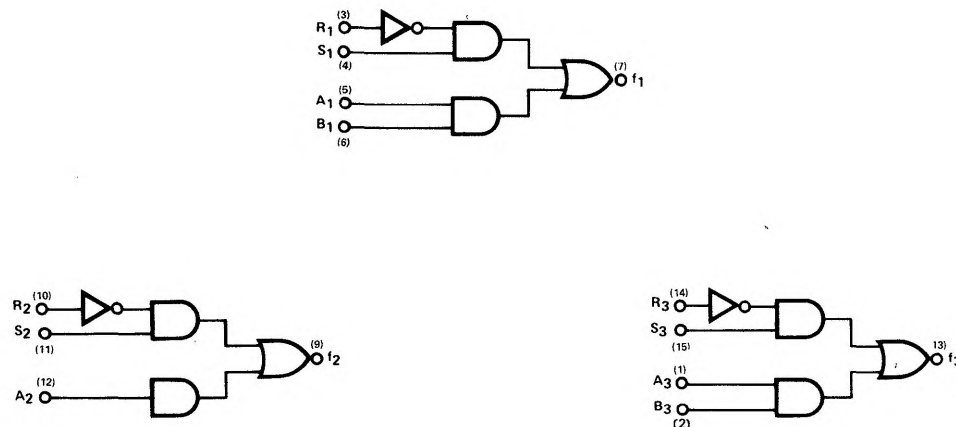
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $T_{ON} = T_{OFF} = 20\text{ns}$ (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

- Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

LOGIC DIAGRAM WITH PIN LAYOUT



V_{CC} = (16)
 GND = (8)
 () = Denotes Pin Numbers

DIGITAL 8000 SERIES TTL/MSI – 8T24

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ TO $+75^\circ C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
“1” Output Voltage	2.6	3.4		V	1.70V	4.5V	0V	0V	-800 μ A	7
	2.6	3.4		V	0V	0.7V	0V	0V	-800 μ A	7
“0” Output Voltage		0.2	0.4	V	0.70V	1.7V	0V	0V	16mA	8
		0.2	0.4	V	0V	0V	1.7V	1.7V	16mA	8
“0” Input Current										
S _n	-0.1		-1.6	mA	0V	0.4V				
A _n	-0.1		-1.6	mA	0V		0.4V			
B _n	-0.1		-1.6	mA				0.4V		
“1” Input Current										
R _n			0.17	mA	3.11V					9
R _n			5.0	mA	7.0V					
R _n			5.0	mA	6.0V					
S _n			40	μ A	3.11V	4.5V				
A _n			40	μ A			4.5V	0V		
B _n			40	μ A			0V	4.5V		

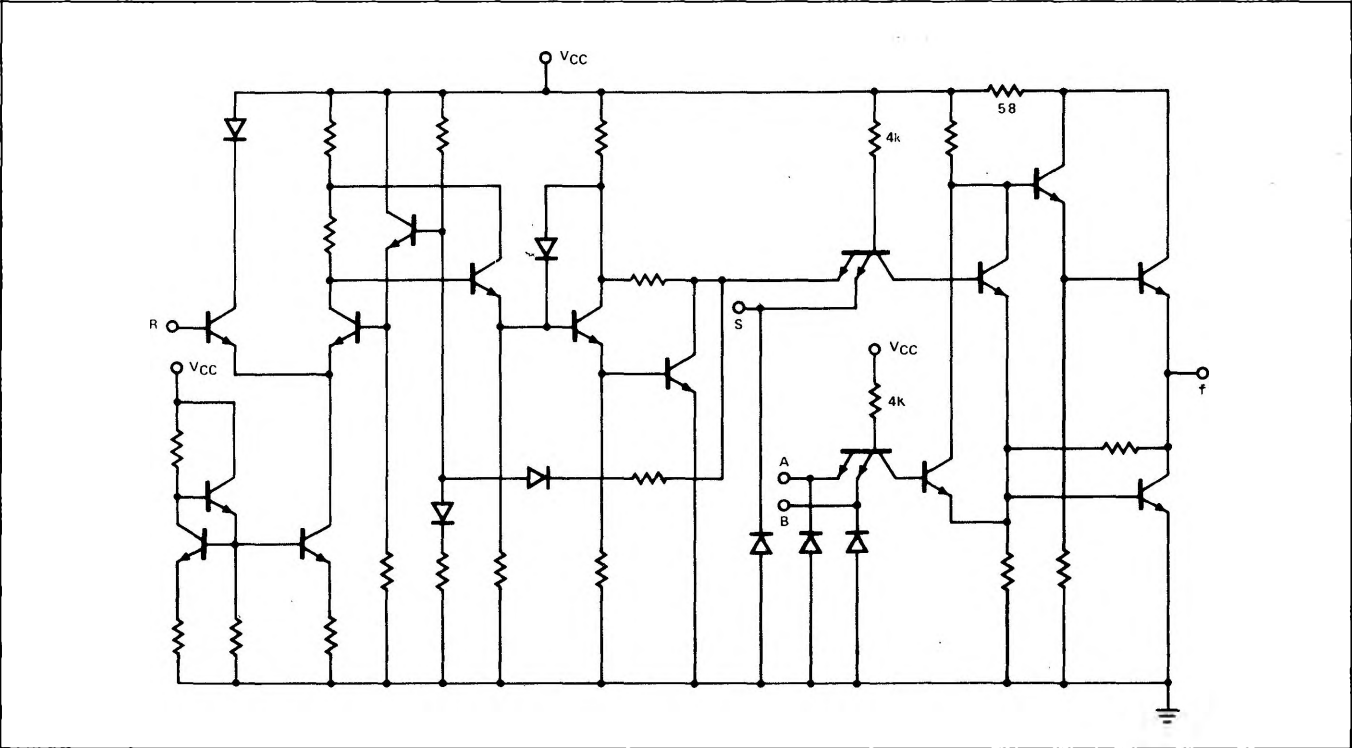
ELECTRICAL CHARACTERISTICS (AT $V_{CC} = 5.0V$ AND $T_A = 25^\circ C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-on Propagation Delay		20	30	nS						13
Turn-off Propagation Delay		20	30	nS						13
Hysteresis	0.2	0.4		V		4.5V	0V	0V		11, 12
Power/Current Consumption		315 60	380 72	mW mA						14
Input Latch Voltage:										
S	5.5			V	3.11V	10mA	0V	0V		10
A	5.5			V	0V	0V	10mA	0V		10
B	5.5			V	0V	0V	0V	10mA		10
Output Short Circuit Current	-50		-100	mA	3.11V	0V	0V	0V		
Input Clamp Voltage										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

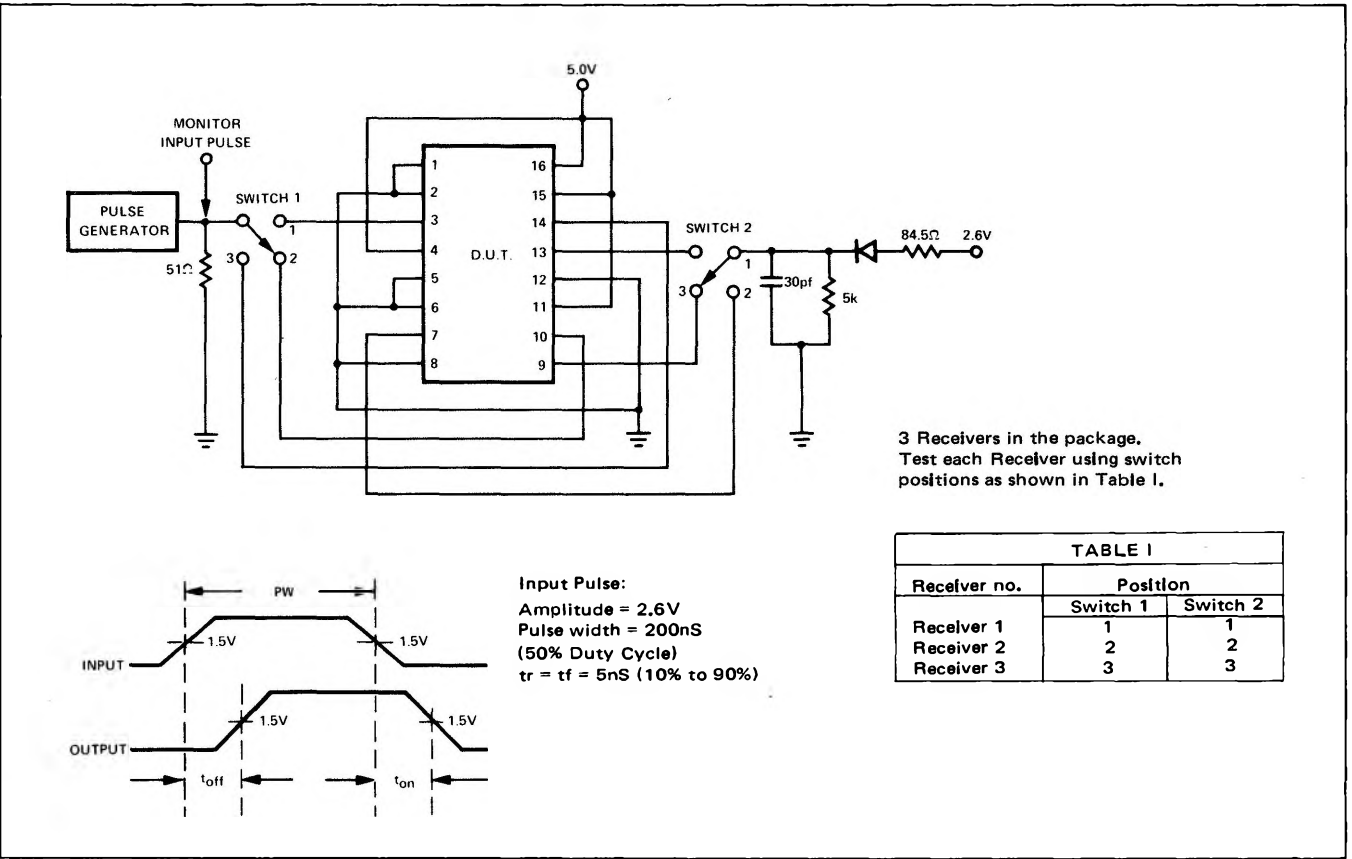
NOTES:

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current is defined as into the terminal referenced.
- Positive logic definition: “UP” Level = “1”, “DOWN” Level = “0”.
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Manufacturer reserves the right to make design and process changes and improvements.
- Output source current is applied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- $V_{CC} = 0.00V$
- This test guarantees operation free of Input latch up over the specified operating supply voltage range.
- Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from “0” to “1” state and the level at which the output begins to go from “1” to “0”.
- See Hysteresis test circuit.
- Refer to AC test circuits.
- $V_{CC} = 5.25V$.

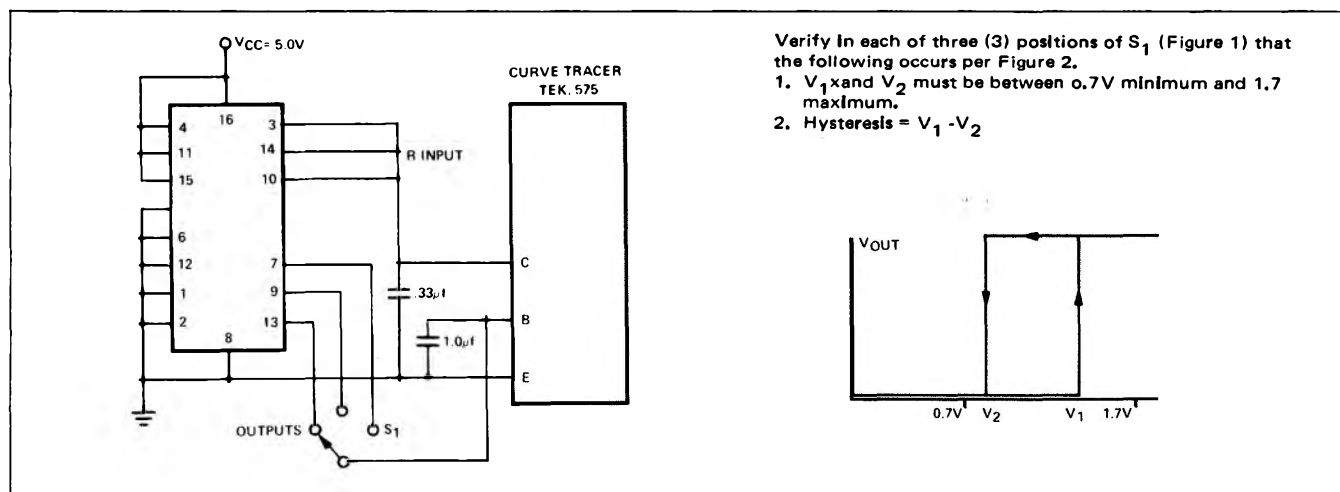
CIRCUIT SCHEMATIC



AC TEST CIRCUIT AND WAVEFORMS



HYSTERESIS TEST CIRCUIT



TYPICAL APPLICATION

