TRIPLE LINE RECEIVER | 8T14

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure (≈30kΩ) presents a minimal load to the driver circuit and allows the transmission line to be terminated in its characteristic impedance to minimize line reflections.

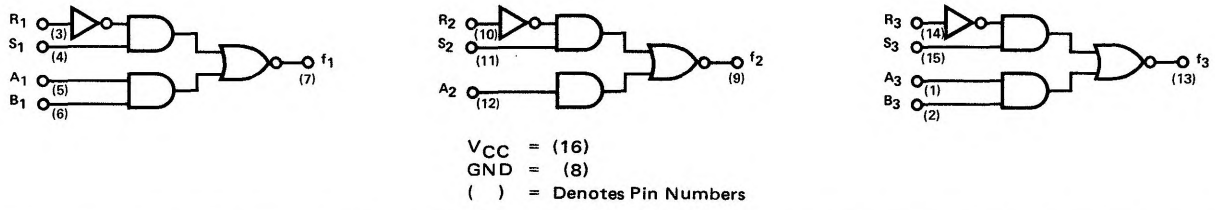
The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

FEATURES

- **BUILT-IN INPUT THRESHOLD HYSTERESIS***
- **HIGH SPEED: $t_{on} = t_{off}$ = 20ns (Typical)**
- **EACH CHANNEL CAN BE STROBED INDEPENDENTLY**
- **FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS**
- **INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY**
- **OPERATION FROM A SINGLE +5 VOLT LOGIC SUPPLY**

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.5 volts typically and 0.3 volts minimum over the operating temperature range.

LOGIC DIAGRAMS



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

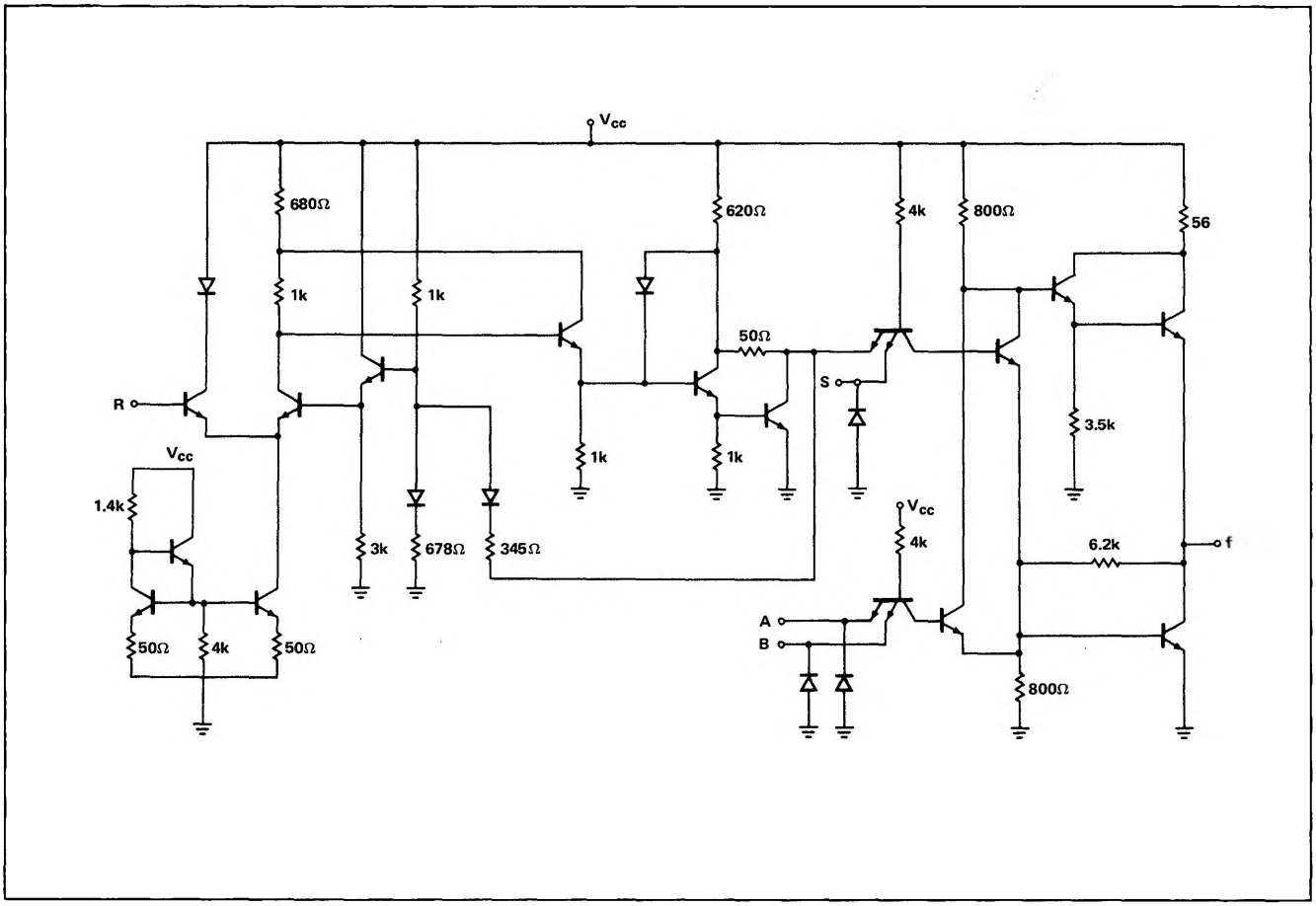
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	4.5V	0V	0V	-800μA	7, 13
	2.6	3.5		V	0V	0.8V	0V	0V	-800μA	7, 13
"0" Output Voltage			0.4	V	0.8V	2.0V	0V	0V	16mA	8, 12
			0.4	V	0V	0V	2.0V	2.0V	16mA	8, 12
"0" Input Current:										
S_n	-0.1		-1.6	mA	0V	0.4V				
A_n	-0.1		-1.6	mA	0V		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.8V					
S_n			40	μA	3.8V	4.5V				
A_n			40	μA			4.5V	0V		
B_n			40	μA			0V	4.5V		
Hysteresis	0.30	0.50		V		4.5V	0V	0V		10, 11

T_A = 25° C and V_{CC} = 5.0V

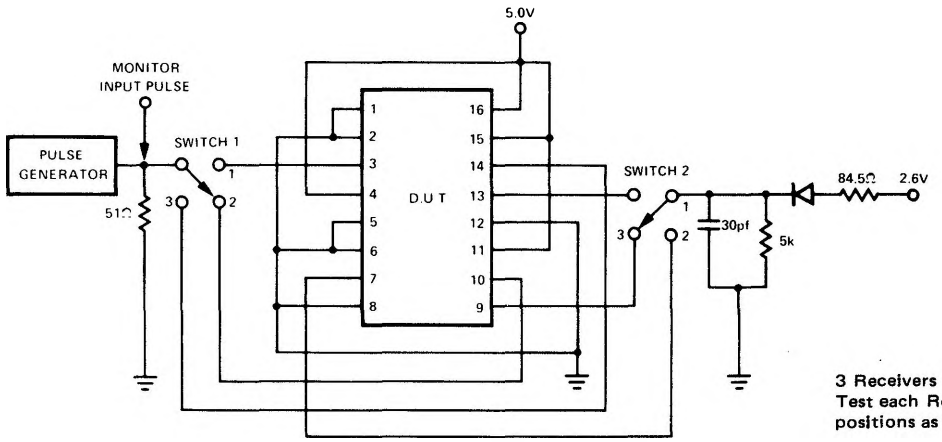
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-On Propagation Delay		20	30	ns						
Turn-Off Propagation Delay		20	30	ns						
Power/Current Consumption		315/60	380/72	mW/mA						
Input Voltage Rating										
S	5.5			V	3.8V	10mA	0V	0V		
A	5.5			V	0V	0V	10mA	0V		
B	5.5			V	0V	0V	0V	10mA		
Output Short Circuit Current	-50		-100	mA	3.8V	0V	0V	0V	0V	
Input Clamp Voltage:										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
10. Hysteresis is defined as voltage difference between R input level at which output begins to go from "0" to "1" state and level at which output begins to go from "1" to "0".
11. V_{CC} = 5.0V.
12. Previous condition is a "1" output state.
13. Previous condition is a "0" output state.
14. V_{CC} = 5.25 volts.

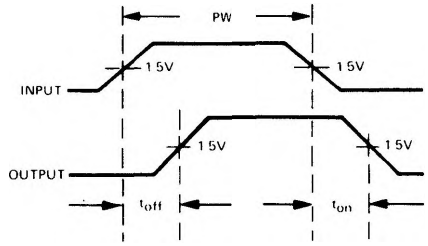
SCHEMATIC DIAGRAM



AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package.
Test each Receiver using switch positions as shown in Table I.

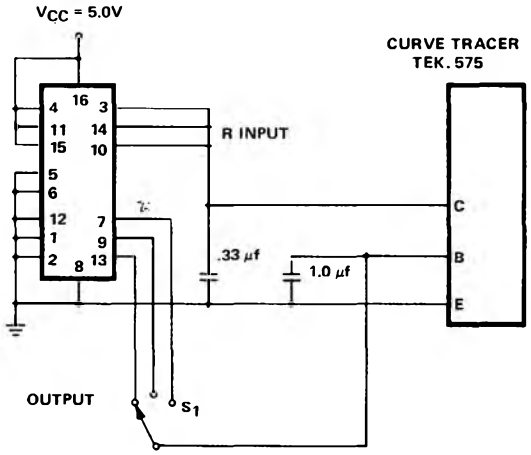


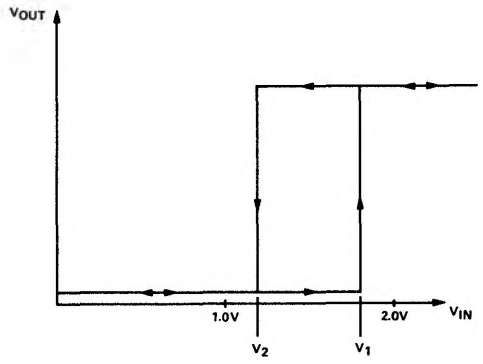
Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

TABLE I

Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT





Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.8V minimum and 2.0V max.
2. Hysteresis = $V_1 - V_2 \geq 0.3V$.

FIGURE 1

FIGURE 2

TYPICAL APPLICATIONS

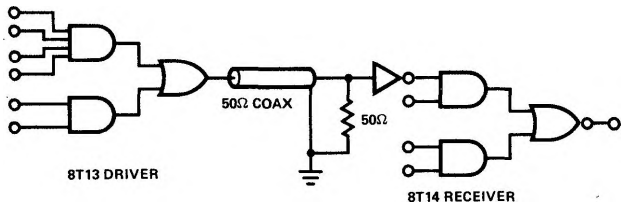
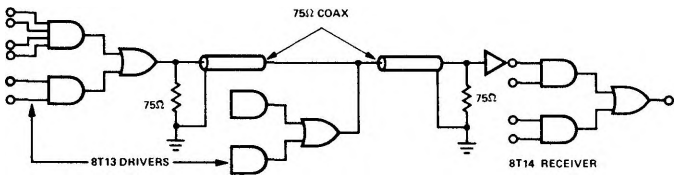


FIGURE 1



If more than one driver/receiver is to be used for each transmission line, the line should be terminated at both ends as shown in Fig. 2.

FIGURE 2

SCHMITT TRIGGER APPLICATION