8-INPUT DIGITAL MULTIPLEXER | 82S30

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S30 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\bar{f}$ output is unconditionally high.
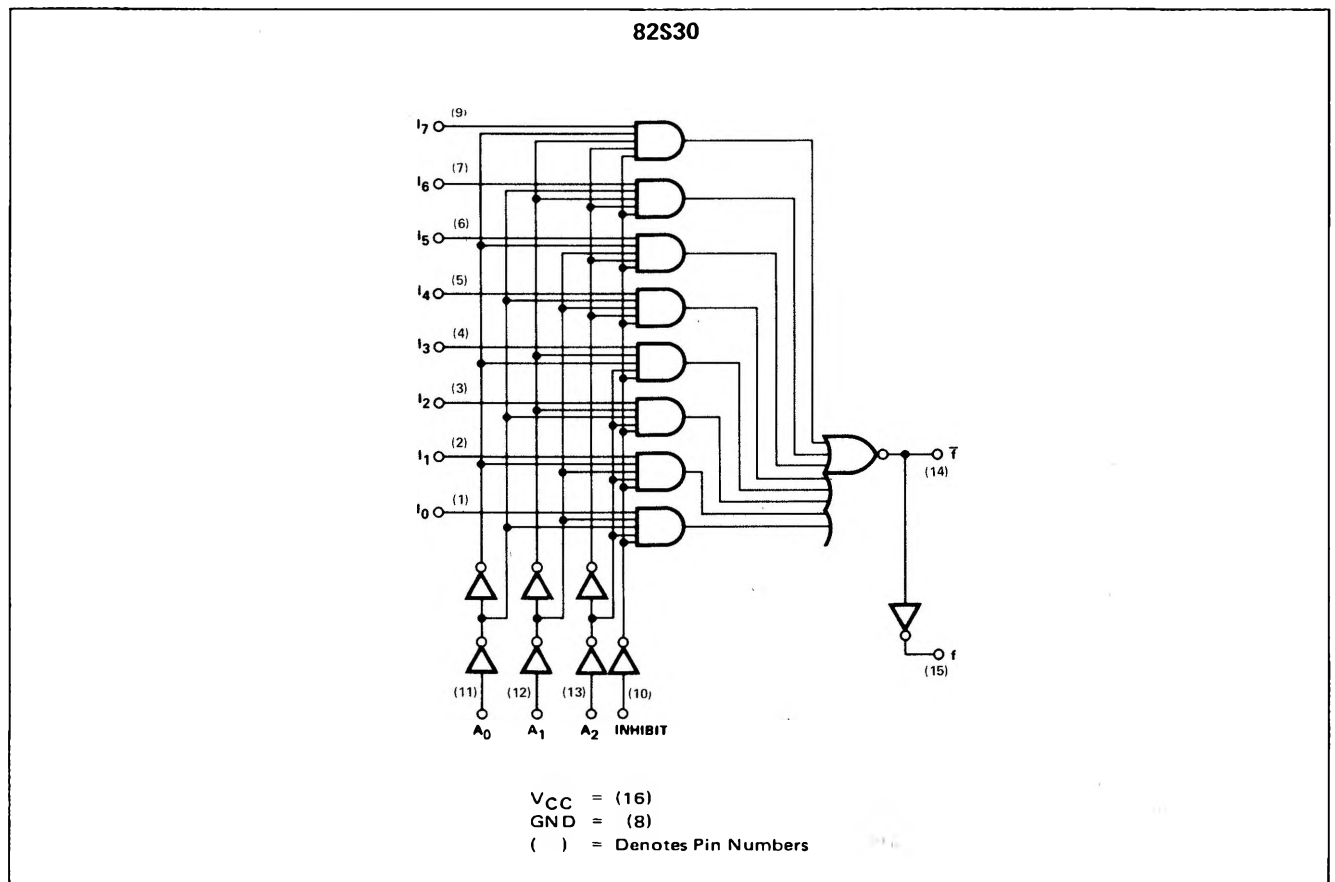
FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- DIRECT OUTPUT INHIBIT
- 82S30 CAN REPLACE 9312 FOR HIGHER SPEED

TRUTH TABLE

ADDRESS			DATA INPUT									OUTPUT	
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	$\bar{f}$	82S30 f
0	0	0	x	x	x	x	x	x	x	1	0	1	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1

x = don't care

LOGIC DIAGRAM

82S30

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | | | NOTES |
	MIN	TYP	MAX	UNITS	A_1	A_2	A_3	INH	DATA INPUT I_n	OUTPUTS	
"1" Output Voltage, Output f	2.7			V	*	*	*	0.8V	2.0V	−1.0mA	6,11
Output $\bar{f}$	2.7			V	*	*	*	2.0V	*	−1.0mA	6,11
"0" Output Voltage			0.5	V	0.8V	0.8V	0.8V	0.8V	0.8V	20mA	7,14
"1" Input Current											
Inputs An, I_n			10	μA	4.5V	4.5V	4.5V		4.5V		
Input INH			10	μA				4.5V			
"0" Input Current											
A_n, I_n, INH			−400	μA	0.5V	0.5V	0.5V		0.5V		

$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | | OUTPUTS | | NOTES |
	MIN	TYP	MAX	UNITS	A	A	A	INH	DATA INPUT I_n	f	$\bar{f}$	
Propagation Delay			20	ns								
A_n to f												
A_n to $\bar{f}$			17	ns								8
I_n to $\bar{f}$			12	ns								8
INH to $\bar{f}$			16	ns								8
Power Consumption/Supply Current			62	mA	4.5V	4.5V	4.5V	4.5V	0V			11
Output Short Circuit Current												
Output f	−40		−100	mA	0V	0V	0V	0V	4.5V	0V		
Output $\bar{f}$	−40		−100	mA	0V	0V	0V	0V	0V		0V	
Input Clamp Voltage	−1.2			V	−18 mA	−18 mA	−18 mA	−18 mA				12

*See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.

6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds at 0.8V for logical "0" and 2.0V for logical "1".
11. All I_n data inputs are at 0V, $V_{CC} = 5.25V$.
12. Connect an external 1K resistor from V_{CC} to the output terminal for this test.

AC TEST FIGURE AND WAVEFORMS

INPUT PULSE:
PRR = 1 MHz
$t_R = t_f = 2.5$ ns
PW = 50 ns
ALL DIODES ARE 1N3064
CL INCLUDES PROBE AND JIG CAPACITANCE

| TEST TABLE | | | | | | | | | | | | | | | |
| TEST NO. | INPUTS | | | | | | | | | | | | | OUTPUTS | |
	A_0	A_1	A_2	INH	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	E	F
1	PG	0	0	0	0	1	0	0	0	0	0	0	T	T
2	0	PG	0	0	0	0	1	0	0	0	0	0	T	
3	0	0	PG	0	0	0	0	0	1	0	0	0	T	
4	0	1	1	PG	0	0	0	0	0	1	0	0	T	
5	1	1	1	0	0	0	0	0	0	0	0	PG	T	

"1" = 2.7V   "0" = GROUND

NOTE:
1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTHS FROM PACKAGE PINS.