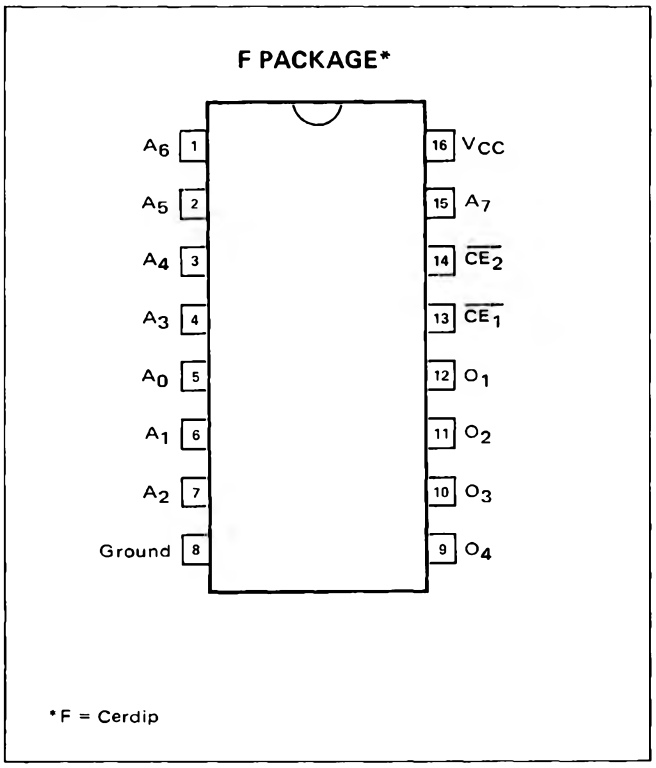
DESCRIPTION

The 82S27 is a Bipolar 1024-Bit Read Only Memory, organized as 256 words by 4 bits per word. It is Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S27 is supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S27 is fully TTL compatible, and includes on-chip decoding, two chip enable inputs, and open collector outputs for ease of memory expansion.

The 82S27 is available in the commercial temperature range. For the commercial temperature range (0°C to +75°C) specify N82S27, F.

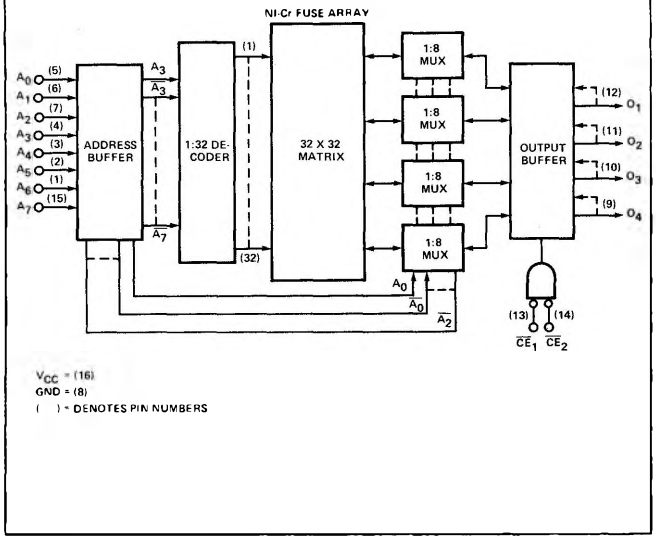
PIN CONFIGURATION



FEATURES

- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- POWER DISSIPATION – 0.6mW/BIT, TYPICAL
- INPUT LOADING – 1.6mA, MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

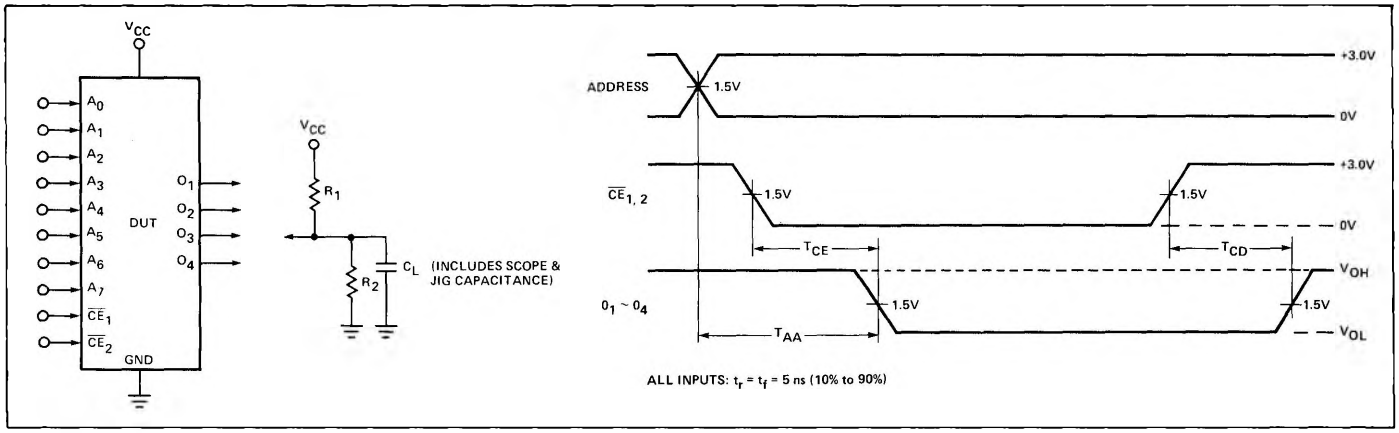
BLOCK DIAGRAM



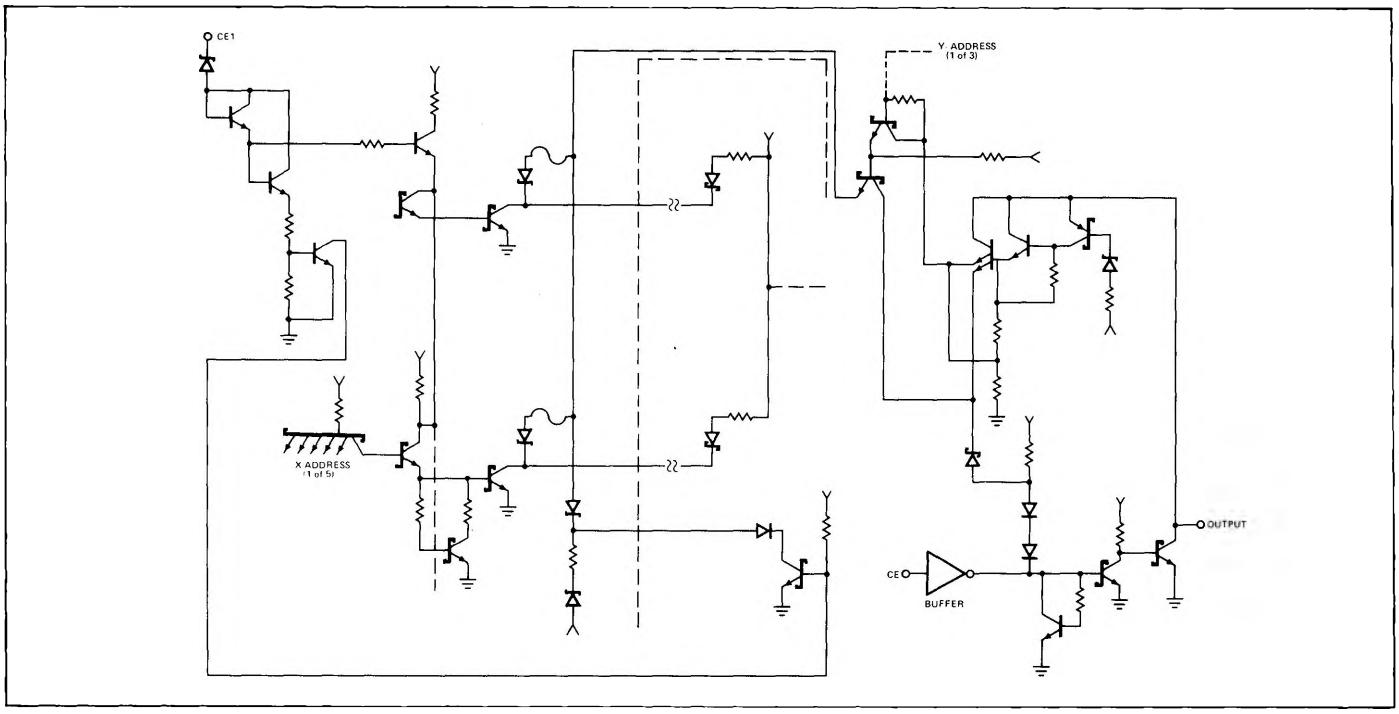
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

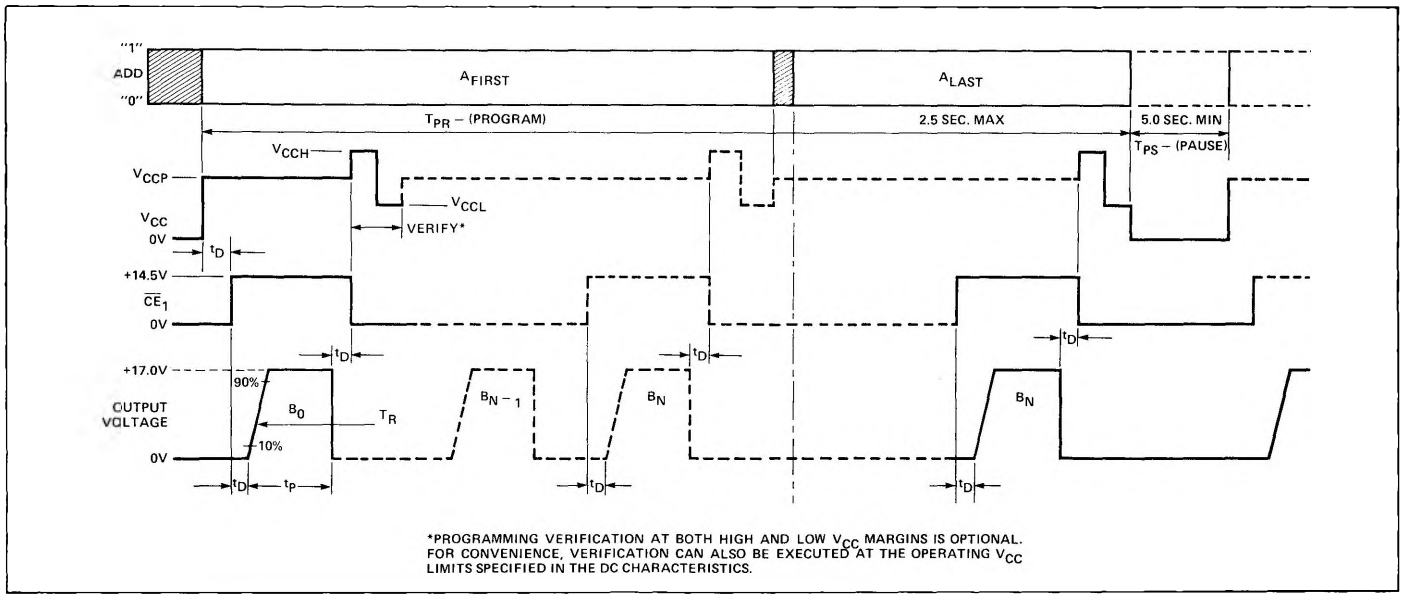
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

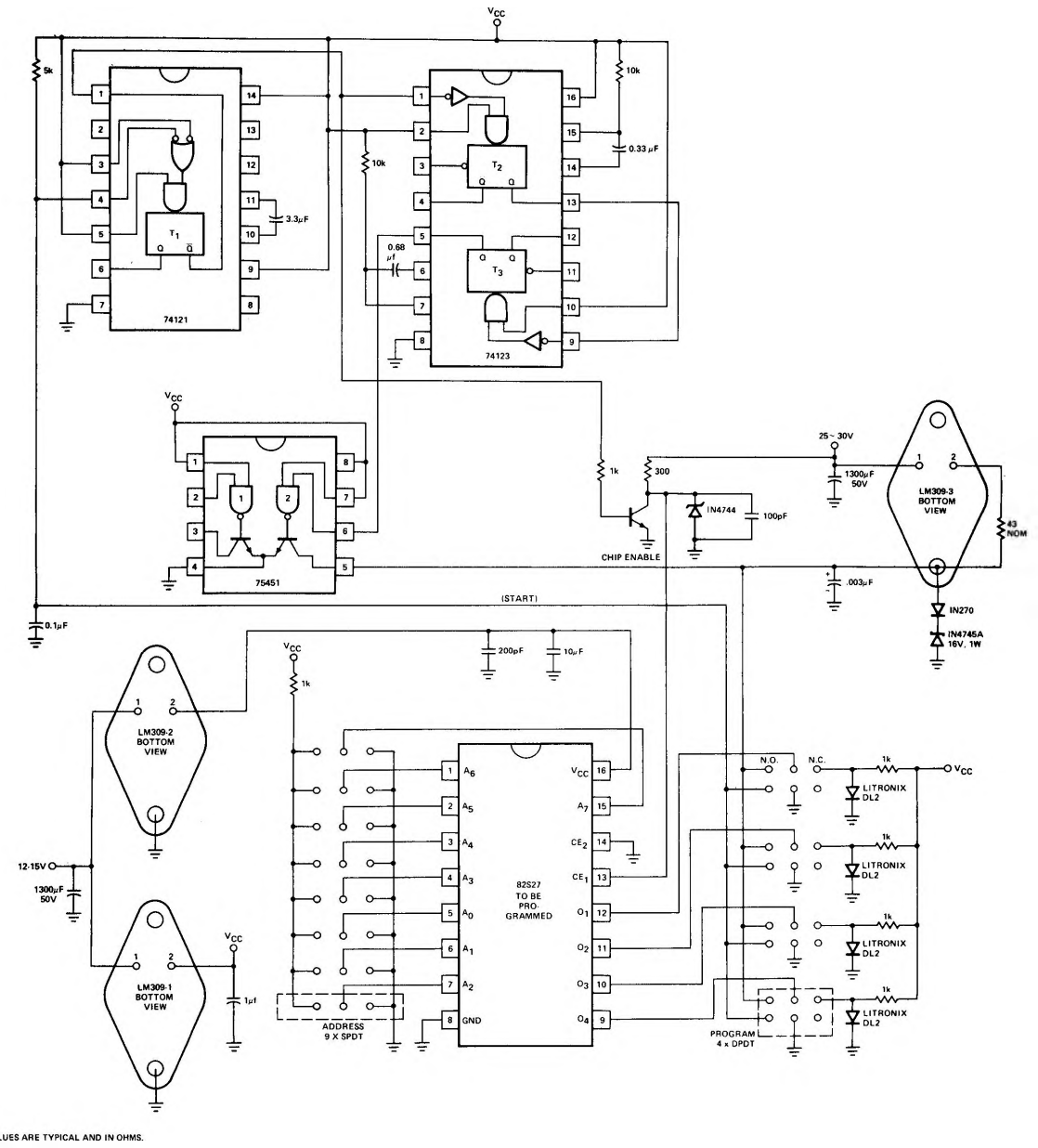
PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 32mA		0.45	0.50	V
I_{OLK}	Output Leakage Current	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{OUT} = 5.5V			100	μA
I_{IH}	"1" Input Current	V_{IN} = 2.4V			40	μA
		V_{IN} = 5.5V			1	mA
I_{IL}	"0" Input Current	V_{IN} = 0.50V			−1.6	mA
V_{IL}	"0" Level Input Voltage				.80	V
V_{IH}	"1" Level Input Voltage		2.0			V
I_{CC}	V_{CC} Supply Current			120	140	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA		−1.0	−1.5	V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE_1}$ or $\overline{CE_2}$ = "1"		8		pF

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{AA}	Address to Output	C_L = 30pF		30	40	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	20	ns

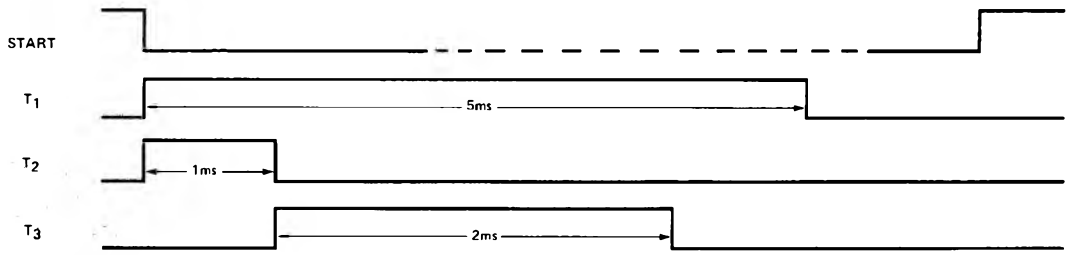
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

MANUAL PROGRAMMER



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TIMING SEQUENCE



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 300 ± 50mA (Transient or steady state)	5.0		5.25	V
V_{CCH}	Upper Verify Limit		5.0	5.25	5.5	V
V_{CCL}	Lower Verify Limit		4.5	4.75	5.0	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +5.0 ± 0.25V	250	300	350	mA
Input Voltage						
V_{IH}	Logical "1" (Except $\overline{CE_1}$)		3.0		5.0	V
V_{IN}	Program Level ($\overline{CE_1}$ Only)		14.0	14.5	15.0	V
V_{IL}	Logical "0"		0	0.4	0.5	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +3.0V			100	μA
I_{IL}	Logical "0"	V_{IL} = +0.5V			-1.6	mA
I_{IN}	Program Level ($\overline{CE_1}$ Only)	V_{IN} = +15.0V			15	mA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 115 ± 10mA (Transient or steady state)	16.5	17.0	17.5	V
I_{OUT}	Output Programming Current	V_{OUT} = +17.0 ± 0.5V	105	115	125	mA
T_R[5]	Output Pulse Rise Time		0.2		0.5	μs
t_P	Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	V_{CC} = V_{CCP}			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10kΩ resistor to V_{CC}.

c. Set $\overline{CE_2}$ to logic "0".

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to $\overline{CE_1}$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 0.5V to the output to be programmed. The source must have a current limit of 115mA. Program one output at the time.

Step 4 After 10μs delay, remove +17.0V supply from programmed output.

Step 5 To verify programming, after 10μs delay, return $\overline{CE_1}$ to 0V. Raise V_{CC} to V_{CCH} = +5.25 ± .25V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.75 ± .25V, and verify that the programmed output remains in the "1" state.

Step 6 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.

Step 7 Repeat steps 1 through 6 to program all other address locations.

NOTES:

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.
5. Measured with a 1k dummy load connected across the fusing source.