DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

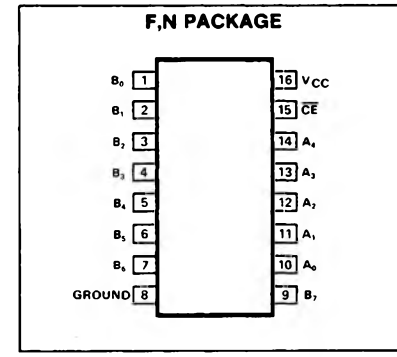
Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F only.

FEATURES

- **Address access time:**
  N82S23/123: 50ns max
  S82S23/123: 65ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S23/123: -100μA max
  S82S23/123: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S23: Open collector
  82S123: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION

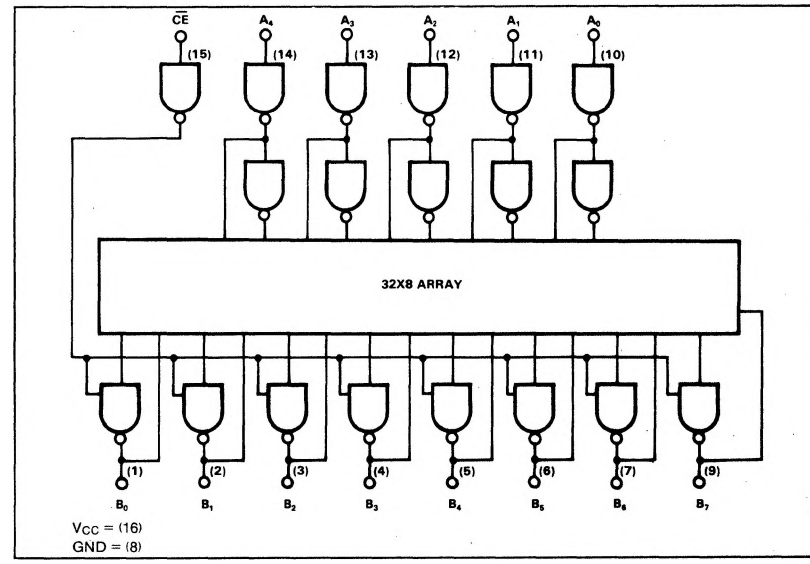
F,N PACKAGE



APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S23)	+5.5	
V_O	Off-state (82S123)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S23/123	0 to +75	
	S82S23/123	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S23/123			S82S23/123			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.85			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			50			50	
	Output current								
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
$I_{O(OFF)}$	Hi-Z state (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-50	
I_{OS}	Short circuit (82S123)	V_{OUT} = 0V	-20		-90	-20		-100	mA
I_{CC}	V_{CC} supply current			65	77		65	85	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[1]

N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

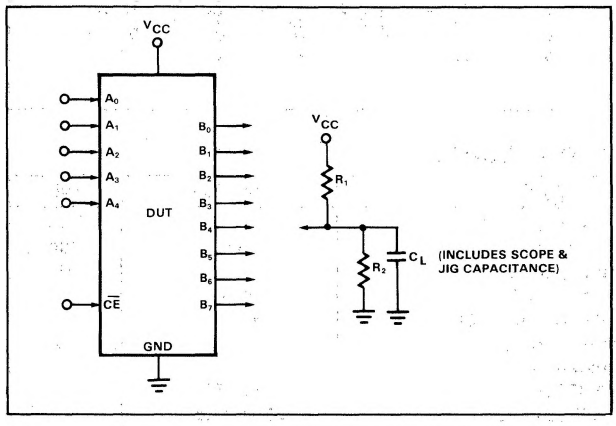
S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S23/123			S82S23/123			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		35	50		35	65	
T_{CE}	Output	Chip enable		25	35		25	40	
Disable time									ns
T_{CD}	Output	Chip disable		25	35		25	40	

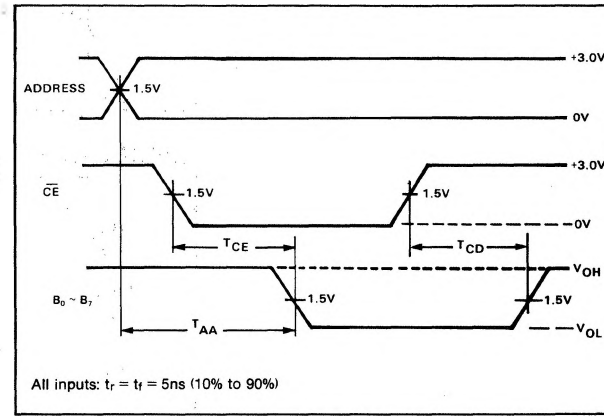
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f$ = 5ns (10% to 90%)

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 250 ± 50mA, Transient or steady state	9.5	10.0	10.5	
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	V_{CCP} = +10.0 ± 0.5V	200	250	300	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 65 ± 3mA, Transient or steady state	15.0	15.5	16.0	V
I_{OUT}	Output programming current	V_{OUT} = +15.5 ± 0.5V	60			mA
T_R	Output pulse rise time		10		50	μs
t_p	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_V	Verify delay		50			μs
t_D	Pulse sequence delay		10			
T_{PRI}	Initial programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

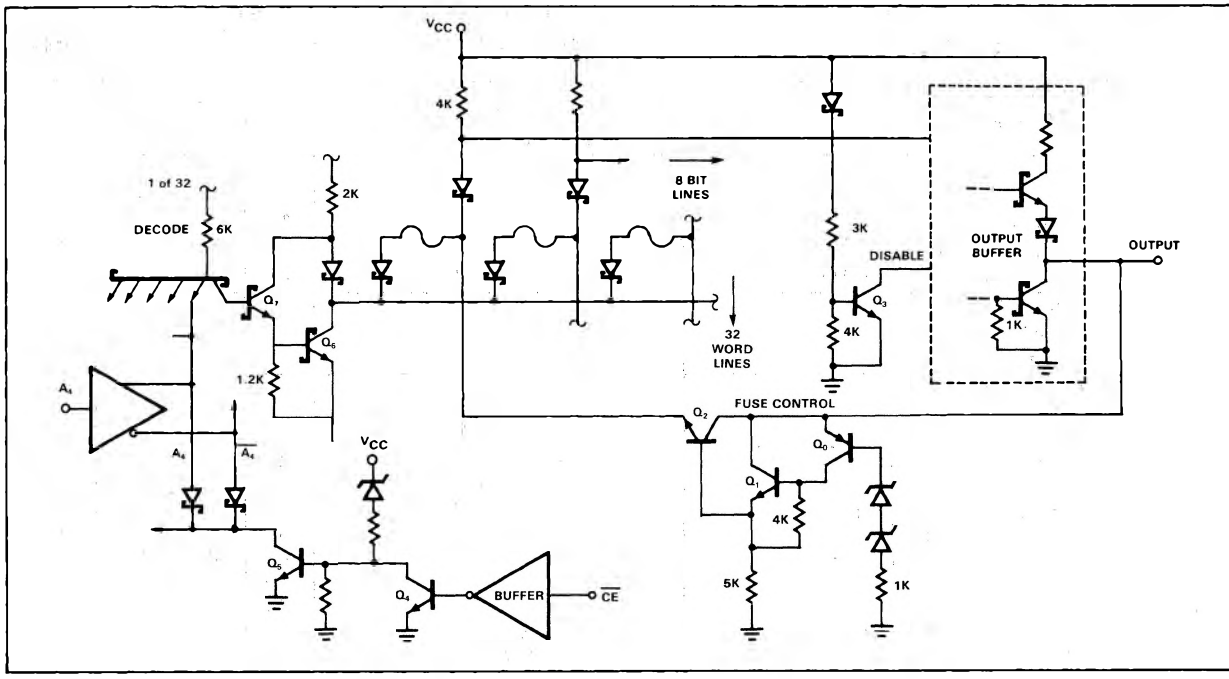
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure that +15.5 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Continuous fusing for an unlimited time is also allowed, provided that a 50% duty cycle is maintained. This may be accomplished by using a programming time and pauses of 6μs each.

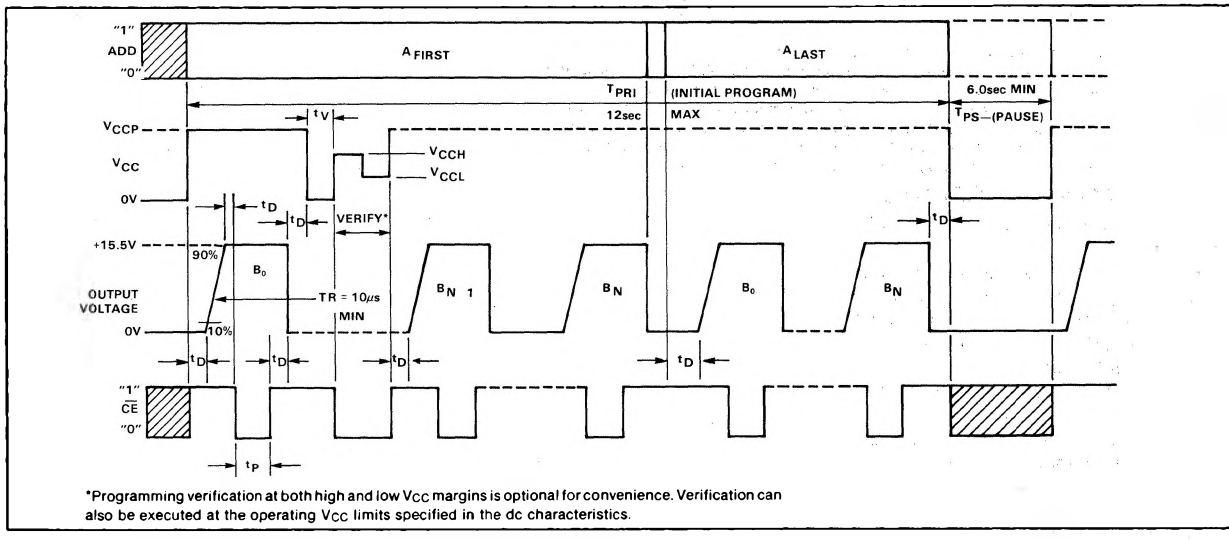
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the address to be programmed, and raise V_{CC} to V_{CCP} = +10 ± 0.5V.
3. After 10μs delay, apply I_{OUT} = 65 ± 3mA to the output to be programmed. Program one output at a time.
4. After 10μs delay, pulse the CE input to logic low for 0.3 to 0.5μs.
5. After 10μs delay, remove I_{OUT} from the programmed output.
6. After 10μs delay, return V_{CC} to 0V.
7. To verify programming, after 50μs delay, raise V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
8. Raise V_{CC} to V_{CCP} = +10 ± 0.5V and repeat steps 3 through 7 to program other bits at the same address.
9. After 10μs delay, repeat steps 2 through 8 to program all other address locations.

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional for convenience. Verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.