

DESCRIPTION

The 82S214 and 82S215 include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S214 and 82S215 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S214/215, F or N, and for the military temperature range (-55°C to +125°C) specify S82S214/215, F.

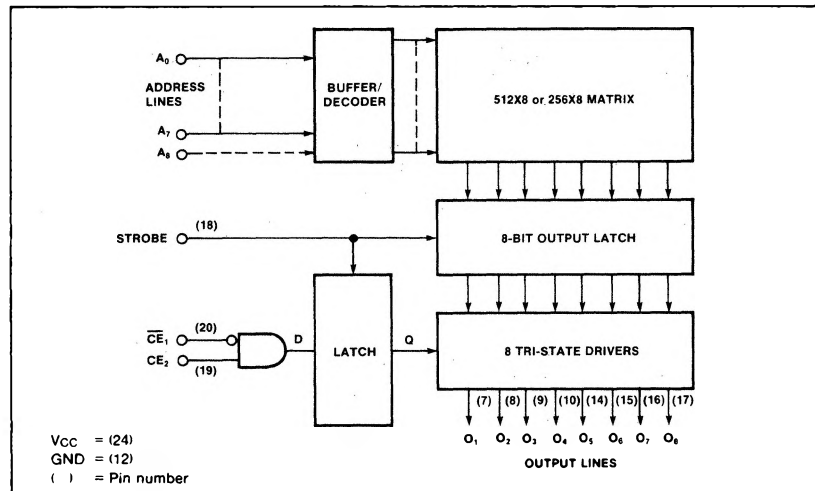
FEATURES

- Address access time:
N82S214/215: 60ns max
S82S214/215: 90ns max
- Power dissipation: 165 μ W/bit typ
- Input loading:
N82S214/215: -100 μ A max
S82S214/215: -150 μ A max
- On-chip data output registers
- On-chip storage latches
- Schottky clamped
- Fully compatible with Signetics 82S114/115 PROMs
- Fully TTL compatible

APPLICATIONS

- Microprogramming
- Hardwire algorithms
- Character generation
- Control store
- Sequential controllers

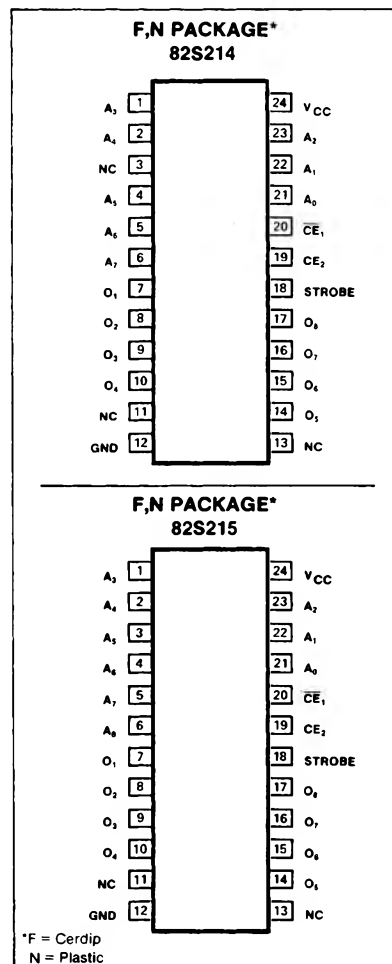
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VCC	+7	Vdc
VIN	+5.5	Vdc
TA	Operating	°C
	N82S214/215	0 to +75
	S82S214/215	-55 to +125
TSTG	Storage	-65 to +150

PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS N82S214/215: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
S82S214/215: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ¹	N82S214/215			S82S214/215			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp	2.0	-0.8	.85 -1.2	2.0	-0.8	.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High	2.7	3.3	0.5	2.4	3.3	0.5	V
I _{IL} I _{IH}	Input current Low High			-100 25			-150 50	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³	-20		40 -40 -70	-15		100 -100 -85	μA mA
I _{CC}	V _{CC} supply current		130	175		130	815	mA
C _{IN} C _{OUT}	Capacitance Input Output		5 8			5 8		pF

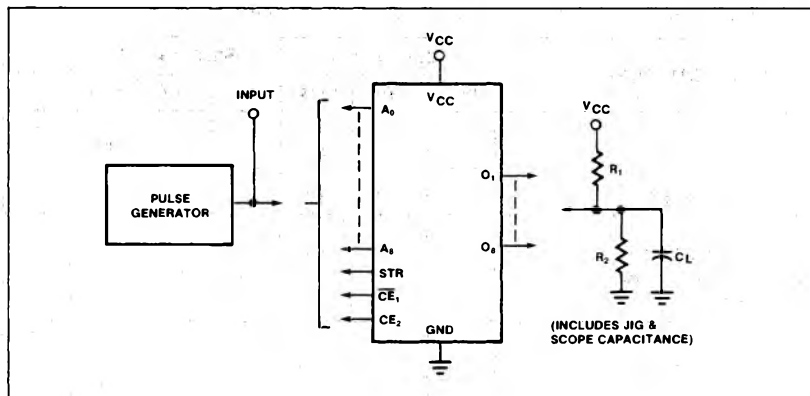
AC ELECTRICAL CHARACTERISTICS R₁ = 470 Ω , R₂ = 1k Ω , C_L = 30pF
N82S214/215: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
S82S214/215: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
				Min	Typ ²	Max	Min	Typ ²	Max	
T _{AA} T _{CE}	Access time ⁴ Output Output	Address Chip enable	Latched or transparent read		35 20	60 40		35 20	90 50	ns
T _{CD}	Disable time ⁴	Output	Chip disable		20	40		20	50	ns
T _{ADH} T _{CDH}	Setup and hold time ⁵ Hold time Setup time Hold time	Output Output	Address Chip enable	0 10	-10 0		5 10	-10 0		ns
T _{SW}	Pulse width ⁵ Strobe		Latched read only	30	20		40	20		ns
T _{SL}	Latch time ⁵ Strobe		Latched read only	60	35		90	35		ns
T _{DL}	Delatch time ⁵ Strobe		Latched read only			30			35	ns

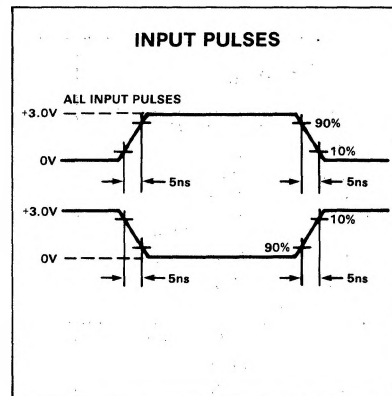
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

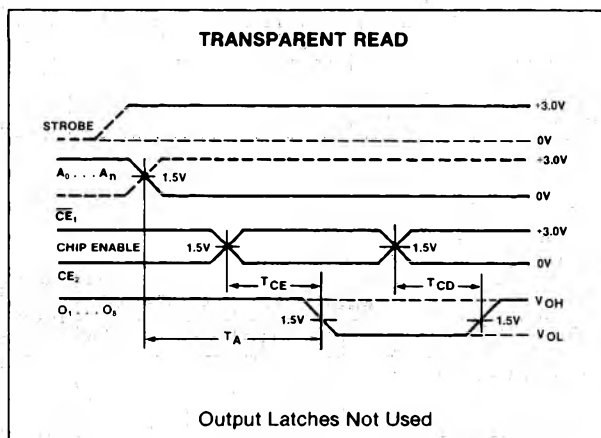
TEST LOAD CIRCUIT



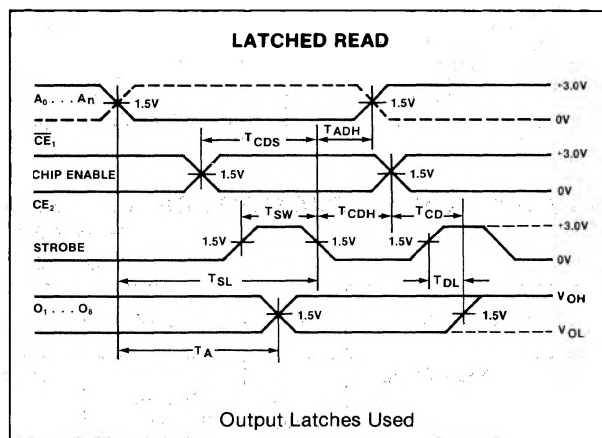
VOLTAGE WAVEFORM



TIMING DIAGRAMS



Output Latches Not Used



Output Latches Used