

DESCRIPTION

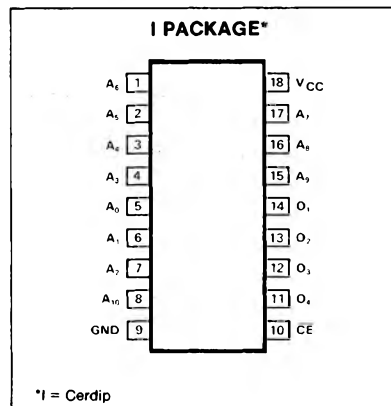
The 82S184 and 82S185 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S184 and 82S185 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

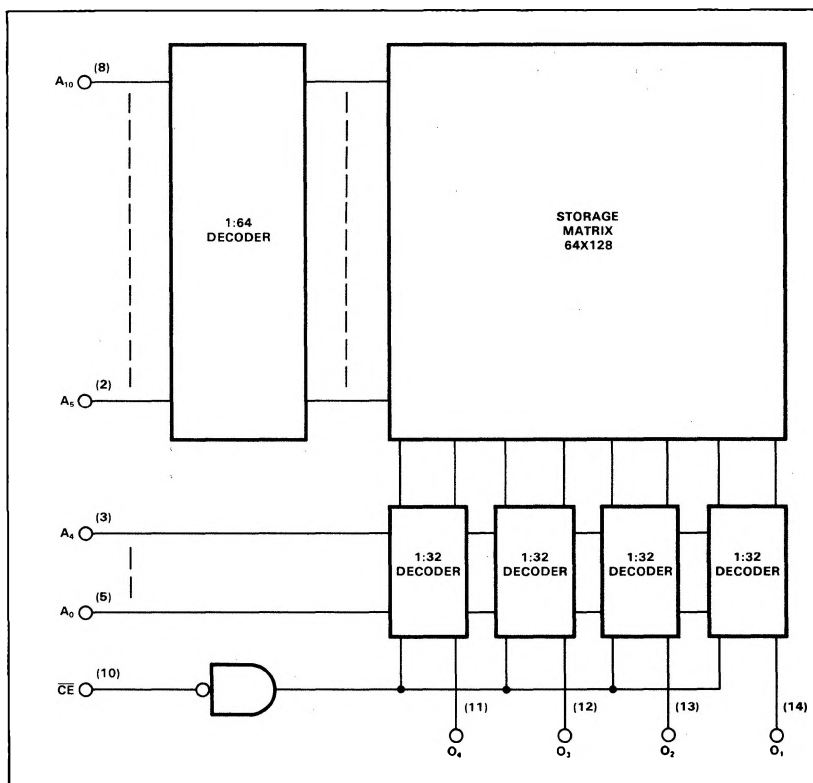
Both 82S184 and 82S185 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S184/185, I, and for the military temperature range (-55°C to +125°C) specify S82S184/185, I.

FEATURES

- **Low power dissipation:** 50µW/bit typ
- **Address access time:**
N82S184/185: 100ns max
S82S184/185: 150ns max
- **Input loading:**
N82S184/185: -100µA max
S82S184/185: -150µA max
- **On-chip address decoding**
- **Output options:**
82S184: Open collector
82S185: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage		V _{dc}
V _{OH} High (82S184)	+5.5	
V _O Off-state (82S185)	+5.5	
T _A Temperature range		°C
T _A Operating		
N82S184/185	0 to +75	
S82S184/185	-55 to +125	
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S184/185: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S184/185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ¹	N82S184/185			S82S184/185			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} Input voltage Low	I _{IN} = -18mA			.85			.80	V
V _{IH} Input voltage High		2.0			2.0			
V _{IC} Input voltage Clamp			-0.8	-1.2		-0.8	-1.2	
V _{OL} Output voltage Low	I _{OUT} = 16mA CE = Low, I _{OUT} = -2mA, High stored			0.45			0.5	V
V _{OH} Output voltage High (82S185)		2.4			2.4			
I _{IL} Input current Low	V _{IN} = 0.45V V _{IN} = 5.5V			-100			-150	μA
I _{IH} Input current High				40			50	
I _{OLK} Output current Leakage (82S184)	CE = High, V _{OUT} = 5.5V CE = High, V _{OUT} = 0.5V CE = High, V _{OUT} = 5.5V V _{OUT} = 0V			40			60	μA
I _O (OFF) Hi-Z state (82S185)				-40			-60	μA
I _{OS} Short circuit (82S185)		-20		40	-15		60	mA
I _{OS} Short circuit (82S185)				-70			-85	mA
I _{CC} V _{CC} supply current			80	120		80	130	mA
C _{IN} Capacitance Input	V _{CC} = 5.0V V _{IN} = 2.0V		5			5		pF
C _{OUT} Capacitance Output	V _{OUT} = 2.0V		8			8		

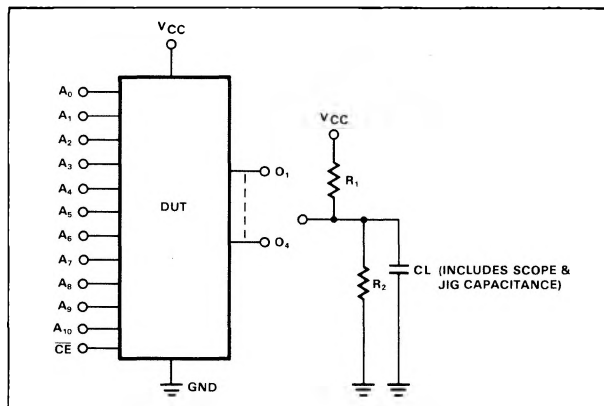
AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82S184/185: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S184/185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S184/185			S82S184/185			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T _{AA} Access time	Output	Address		70	100		70	125	ns
T _{CE} Chip enable				30	40		30	60	
T _{CD} Disable time	Output	Chip disable		30	40		30	60	ns

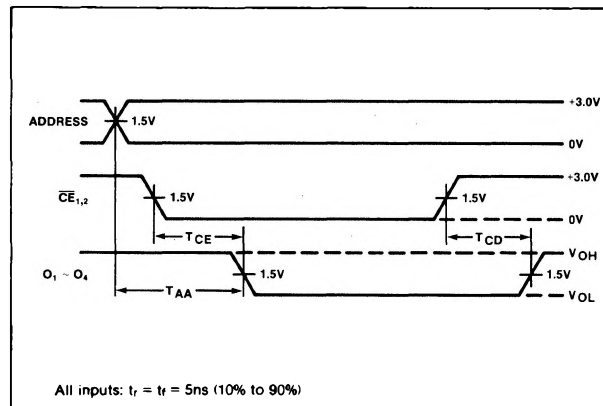
NOTES

- All voltage values are with respect to network ground terminal.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Positive current is defined as into the terminal referenced.
- Duration of the short circuit should not exceed 1 second.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 375 \pm 75\text{mA}$, Transient or steady state	8.5	8.75	9.0	V
V_{CCH} Verify limit Upper		5.3	5.5	5.7	V
V_{CCL} Lower		4.3	4.5	4.7	V
V_S Verify threshold ²		1.4	1.5	1.6	V
I_{CCP} Programming supply current	$V_{CCP} = +8.75 \pm .25\text{V}$	300		450	mA
V_{IH} Input voltage High		2.4		5.5	V
V_{IL} Low		0	0.4	0.8	V
I_{IH} Input current High	$V_{IH} = +5.5\text{V}$			50	μA
I_{IL} Low	$V_{IL} = +0.4\text{V}$			-500	μA
V_{OUT} Output programming voltage ³	$I_{OUT} = 200 \pm 20\text{mA}$, Transient or steady state	16.0	17.0	18.0	V
I_{OUT} Output programming current	$V_{OUT} = +17 \pm 1\text{V}$	180	200	220	mA
T_R Output pulse rise time		10		50	μs
t_p CE programming pulse width		0.3	0.4	0.5	ms
t_D Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI} Initial programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%
F_L Fusing attempts per link				2	cycle

NOTES

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10k\Omega$ resistor to V_{CC} . Apply $\overline{CE} = \text{High}$.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After $10\mu s$ delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After $10\mu s$ delay, pulse the $\overline{CE}$ input to logic low for 0.3 to 0.5ms.
5. After $10\mu s$ delay, remove $+17V$ from the programmed output.
6. To verify programming, after $10\mu s$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic low level to the $\overline{CE}$ input. The programmed output should remain in the high state. Again, low V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu s$ delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE