

DESCRIPTION

The 82S16/116 and 82S17/117 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors which reduce input loading to 25 μ A for a high level, and -100 μ A for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S16/116/17/117, F or N. The 82S16 and 82S17 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S16/17.

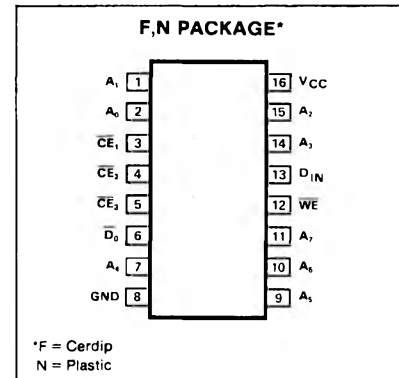
FEATURES

- Address access time:
82S116/117: 40ns max
- Write cycle time:
82S116/117: 25ns max
- Power dissipation: 1.5mW/bit typ
- Input loading:
N82S16/117: -100 μ A
- Output follows complement of data input during Write
- On-chip address decoding
- Output option:
82S16/116: Tri-state
82S17/117: Open collector
- Schottky clamped
- TTL compatible

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION

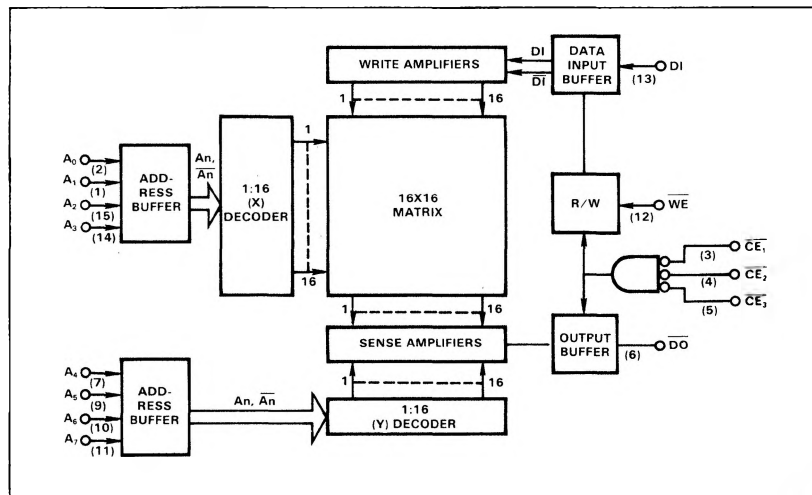


TRUTH TABLE

MODE	$\overline{CE}^*$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S16/116	82S17/117
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Disabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	V _{dc}
V _{IN}	Input voltage	+5.5	V _{dc}
V _{OUT}	Output voltage	+5.5	V _{dc}
V _O	High (82S17)		
V _O	Off-state (82S16)		
T _A	Temperature range		°C
	Operating		
	S82S16/17	-55 to +125	
	N82S16/17, N82S116/117	0 to +75	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S116/117, N82S16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S16/17: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S16/17/116/117			S82S16/17			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IH} V _{IL} V _{IC}	Input voltage ²								V
	High	V _{CC} = Max	2.0			2.0			
	Low	V _{CC} = Min			0.85			0.8	
	Clamp ³	V _{CC} = Min, I _{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
V _{OH} V _{OL}	Output voltage ²								V
	High (82S16/116) ⁴	V _{CC} = Min I _{OH} = -3.2mA	2.6			2.4			
	Low ⁵	I _{OL} = 16mA		0.35	0.45		0.35	0.5	
I _{IH} I _{IL}	Input current ³								mA
	High	V _{CC} = Max V _{IN} = 5.5V		1	25		1	25	
	Low	V _{IN} = 0.45V		-10	-100		-10	-250	
I _{OLK} I _{O(OFF)} I _{OS}	Output current								μA
	Leakage (82S17/117) ⁶	V _{OUT} = 5.5V		1	40		1	40	μA
	Hi-Z state (82S16/116) ⁶	V _{OUT} = 5.5V		1	40		1	50	μA
		V _{OUT} = 0.45V		-1	-40		-1	-50	μA
	Short-circuit (82S16/116) ⁷	V _{CC} = Max, V _O = 0V	-20		-70	-20		-70	μA
I _{CC}	V _{CC} supply current	V _{CC} = Max		80	115		80	120	mA
C _{IN} C _{OUT}	Capacitance								pF
	Input	V _{CC} = 5.0V V _{IN} = 2.0V		5			5		
	Output	V _{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

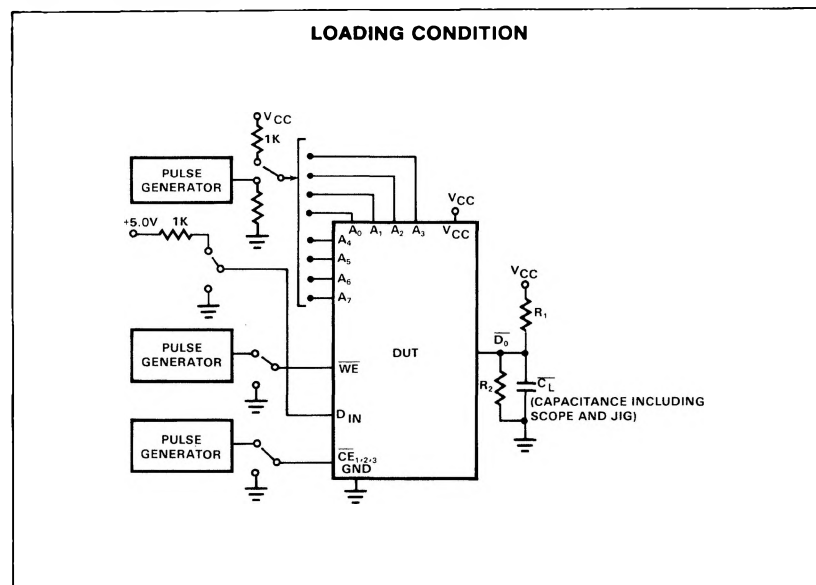
 $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$ N82S16/117, N82S16/17: $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ S82S16/17: $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S16/17			N82S116/117			S82S16/17			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	Min	Typ ¹	Max	
T_{AA} Access time				40	50		30	40		40	70	ns
T_{CE} Chip enable				30	40		15	25		30	40	ns
T_{CD} Disable time	Output	Chip enable		30	40		15	25		30	40	ns
T_{WD} Valid time	Output	Write enable		30	40		30	40		30	55	ns
T_{WSA} Setup and hold time												ns
Setup time	Write enable	Address	20	5		0	-5		20	5		
Hold time			5	0		0	-5		10	0		
T_{WSD} Setup time	Write enable	Data in	40	30		25	15		50	40		
Hold time			5	0		0	-5		10	0		
T_{WSC} Setup time	Write enable	$\overline{CE}$	10	0		0	-5		10	0		
Hold time			5	0		0	-5		10	0		
T_{WP} Pulse width												ns
Write enable ⁸			30	15		25	15		40	20		

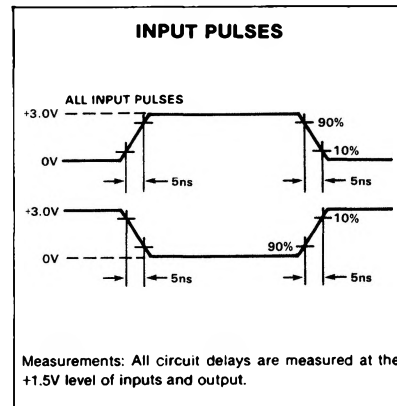
NOTES

1. All typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^\circ\text{C}$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at the time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC} .
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

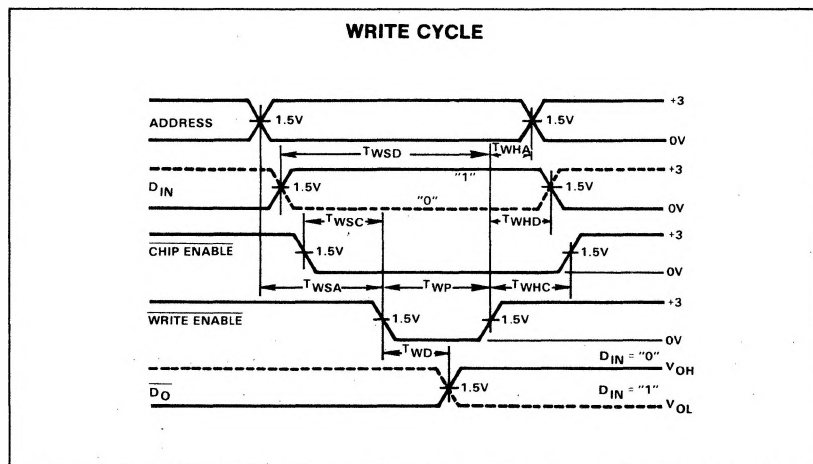
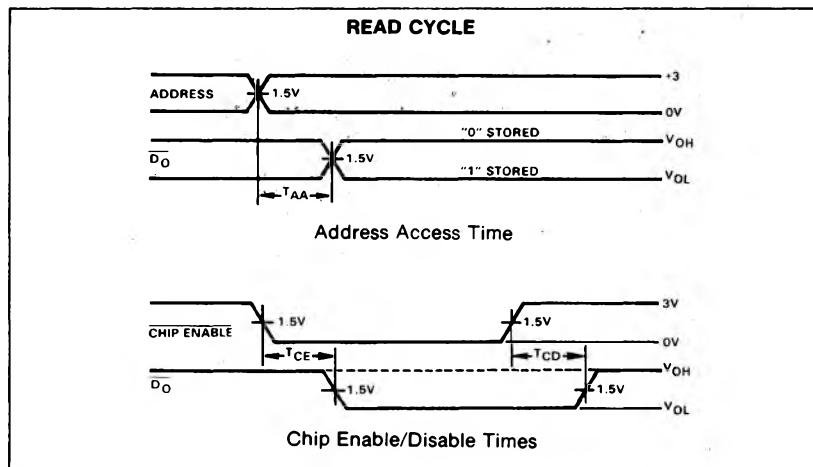
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD}** Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA}** Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC}** Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD}** Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP}** Width of Write Enable pulse.
- T_{WSA}** Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD}** Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD}** Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
- T_{WHC}** Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA}** Required delay between end of Write Enable pulse and end of valid Address.