

DESCRIPTION

The 82S10/11, with a typical access time of 30ns, is ideal for cache buffer applications and for systems requiring very high speed main memory.

The 82S10/11 family requires single +5V power supply and features very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S10/110/11/111. The 82S10 and 82S11 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S10/11.

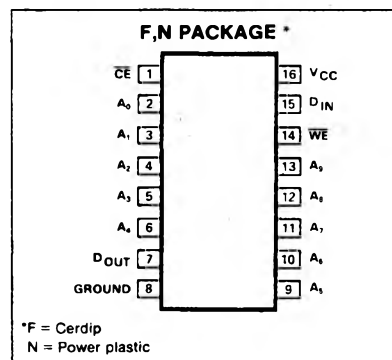
FEATURES

- **Address access time:**
N82S10/11: 45ns max
S82S10/11: 70ns max
N82S110/111: 35ns max
- **Write cycle time:**
N82S10/11: 45ns max
S82S10/11: 75ns max
N82S110/111: 40ns max
- **Power dissipation:** 0.5W/bit typ
- **Input loading:**
N82S10/11: -250μA max
S82S10/11: -250μA max
N82S110/111: -250μA max
- **Output options:**
82S10/110: Open collector
82S11/111: Tri-state
- **On-chip address decoding**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

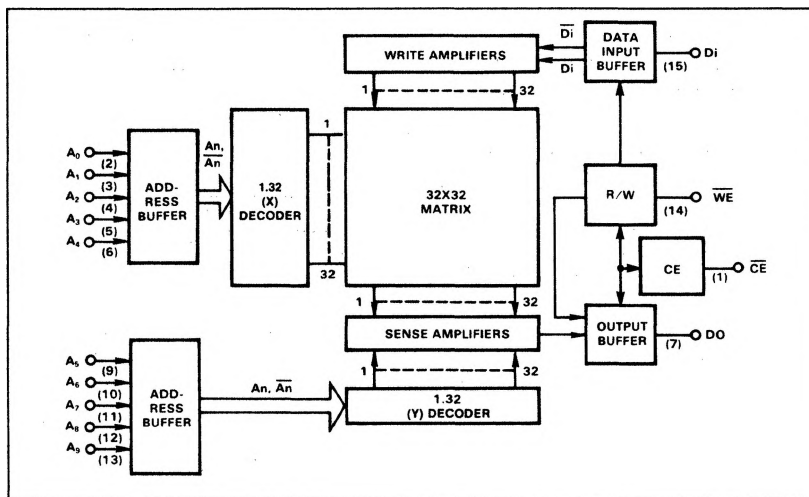


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D	D OUT	
				82S10/110	82S11/111
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹		RATING	UNIT
V _{CC}	Supply voltage	+7	V _{dc}
V _{IN}	Input voltage	+5.5	V _{dc}
	Output voltage		V _{dc}
V _{OH}	High (82S10/110)	+5.5	
V _O	Off-state (82S11/111)	+5.5	
	Temperature range		°C
T _A	Operating		
	N82S10/11/110/111	0 to +75	
	S82S10/11	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS²
N82S10/110/11/111: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S10/11: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N82S10/11/110/111			S82S10/11			UNIT
		Min	Typ ³	Max	Min	Typ ³	Max	
V _{IL}	Input voltage Low ¹			.85			.80	V
V _{IH}	Input voltage High ¹	2.1			2.1			V
V _{IC}	Clamp ^{1,4}		-1.0	-1.5		-1.0	-1.5	V
V _{OL}	Output voltage Low ^{1,5}		0.35	0.45		0.35	0.50	V
V _{OH}	Output voltage High (82S11/111) ^{1,6}	2.4			2.4			V
I _{IL}	Input current Low		-10	-250		-10	-250	μA
I _{IH}	Input current High		1	25		1	40	μA
I _{OLK}	Output current Leakage (82S10/110) ⁷		1	40		1	60	μA
I _{O(OFF)}	Output current Hi-Z state (82S11/111)		1	60		1	100	μA
I _{OS}	Output current Short circuit (82S11/111) ⁸		-1	-60		-1	-100	mA
I _{CC}	V _{CC} supply current ⁹			-100			-100	mA
			120	155		120	155	mA
			95	130		95	130	mA
				170			170	mA
C _{IN}	Capacitance Input		7			4		pF
C _{OUT}	Capacitance Output							pF

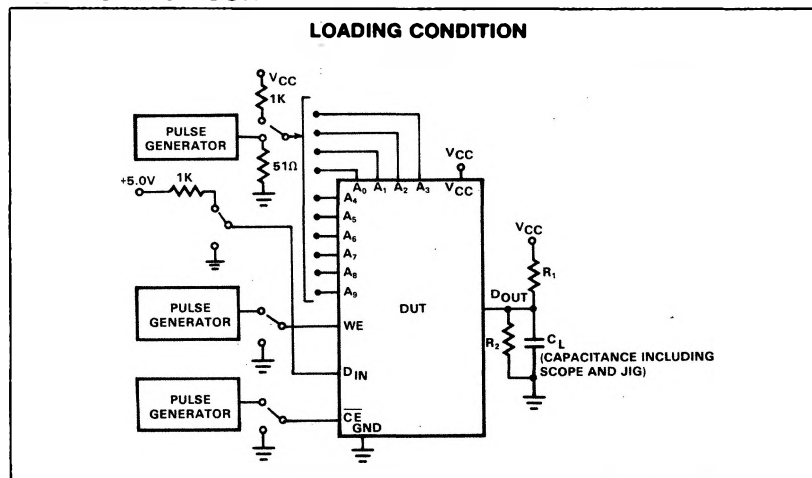
AC ELECTRICAL CHARACTERISTICS² $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$ N82S10/110/111/111: $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ S82S10/11: $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S10/11			N82S110/111			S82S10/11			UNIT
			Min	Typ ³	Max	Min	Typ	Max	Min	Typ ³	Max	
Access time T_{AA} Address T_{CE} Chip enable				30 15	45 30			35 25		30 15	70 45	ns
Disable time T_{CD} T_{WD}	Output Output	Chip enable Write enable		15 20	30 30			25 25		15 20	45 45	ns
T_{WR} Write recovery time				20	30			25		20	45	ns
Setup and hold time T_{WSA} Setup time T_{WHA} Hold time	Write enable	Address	5	0		5			15	0		ns
T_{WSD} Setup time T_{WHD} Hold time			5	0		10			10	0		
T_{WSD} Setup time T_{WHD} Hold time	Write enable	Data in	40	30		30			55	35		
T_{WSD} Setup time T_{WHD} Hold time			5	0		5			5	0		
T_{WSC} Setup time T_{WHC} Hold time	Write enable	$\overline{CE}$	5	0		5			5	0		ns
T_{WSC} Setup time T_{WHC} Hold time			5	0		5			5	0		
Pulse width T_{WP} Write enable ¹⁰			35	25		25			50	25		ns

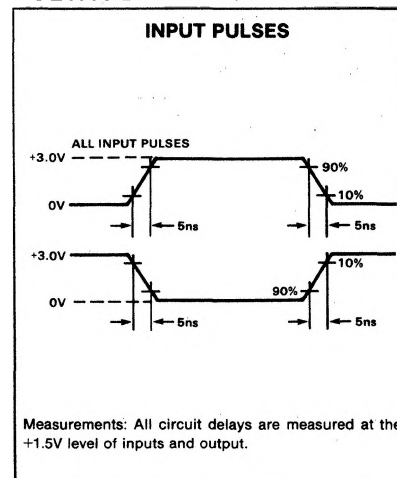
NOTES

- All voltage values are with respect to network ground terminal.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
Typical thermal resistance values of the package at maximum temperature are:
 θ_{JA} junction to ambient at 400lpm air flow - $50^\circ\text{C}/\text{watt}$
 θ_{JA} junction to ambient - still air - $90^\circ\text{C}/\text{watt}$
 θ_{JA} junction to case - $20^\circ\text{C}/\text{watt}$
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Test each input one at a time.
- Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
- Measured with V_{IH} applied to $\overline{CE}$.
- Duration of the short circuit should not exceed 1 second.
- I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

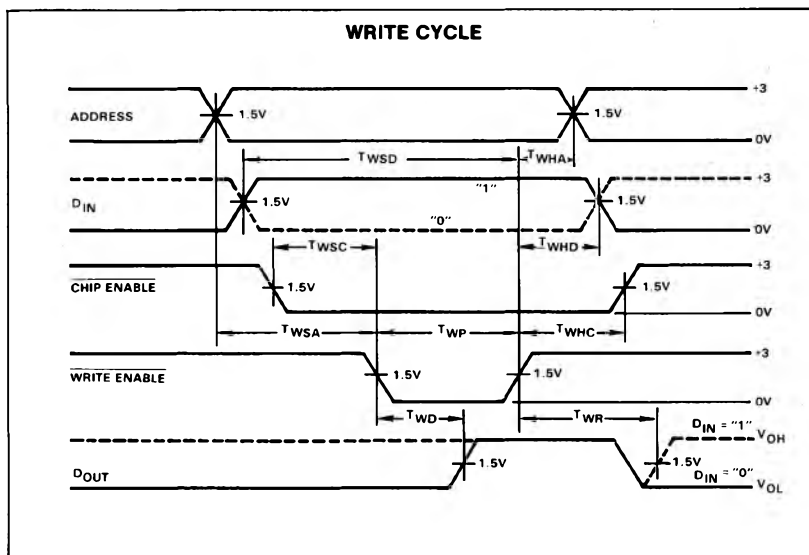
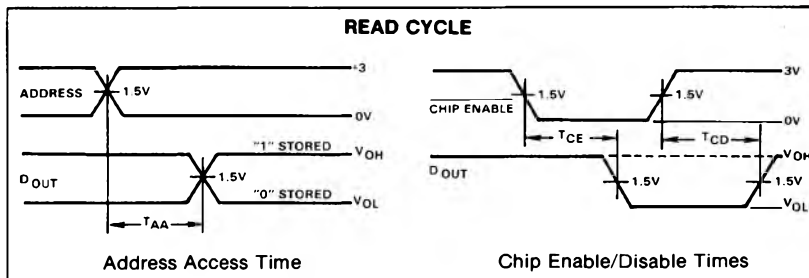
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{WR}** Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
- T_{CE}** Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD}** Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA}** Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC}** Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD}** Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP}** Width of Write Enable pulse.
- T_{WSA}** Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD}** Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD}** Delay between beginning of Write Enable pulse and when Data Output is in off state.
- T_{WHC}** Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA}** Required delay between end of Write Enable pulse and end of valid Address.